ECE65 Final, Spring 2014

For FETs, assume $V_{Tn} = |V_{Tp}| = 1 \text{ V}$, and $\mu_n C_{ox} W/L = \mu_p C_{ox} W/L = 2 \text{ mA/V}^2$, and $\lambda = 0.01 \text{V}^{-1}$.

For BJTs, assume $\beta = 100$, $V_{DD}=0.7 \text{V}$, $V_{sat}=0.2 \text{V}$, and $V_A=100 \text{V}$.

Assume $V_T=26 \text{ mV}$, and $n=1$ for all BJTs and diodes.

You may ignore the effect of $\lambda$ or $V_A$ for biasing, but not for small signal analysis.

1. **Design a peak detector circuit using a combination of diodes and 1 pF capacitors.**
   a) Draw the circuit.
   b) For a 5 Volt, 1 GHz sine wave input, draw the output as a function of time starting at $t=0$.
   c) Assume that the input has a DC voltage of 1 V, draw the small signal circuit.
   d) For the small signal circuit in part c, calculate the small signal transfer function $v_o/v_i$.
   e) Repeat part b assuming that the output is applied across a 1 k$\Omega$ load.
   f) For the circuit in part e, assume that the input has a DC voltage of 1 V, draw the small signal circuit.
   g) For the small signal circuit in part f, calculate the small signal transfer function $v_o/v_i$. For this last part you may ignore the effect of the capacitor on the impedance.

2. **Design a clipper circuit that is capable of limiting an input signal to $|V_{out}|=1.4 \text{ V}$ at the output using a combination of diodes and 1 k$\Omega$ resistors.**
   a) Draw the circuit.
   b) Plot the large-signal transfer function $V_o$ versus $V_i$.
   c) For a 5 Volt, 1 GHz sine wave input, draw the output signal as a function of time.
   d) Assuming that the input has a DC voltage of 1 V, draw the small signal circuit.
   e) For the small signal circuit in part d, calculate the small signal transfer function $v_o/v_i$.
   f) Assuming that the input has a DC voltage of 1.5 V, draw the small signal circuit.
   g) For the small signal circuit in part f, calculate the small signal transfer function $v_o/v_i$.
   h) Now assume that your diodes are replaced with Zener diodes with $V_Z=10 \text{ V}$. What is the change to the large signal transfer function $V_o$ versus $V_i$?

3. **Design a 2 mA current source using a current mirror based on PNP transistors. You have a 10 V source.**
   a) Draw the circuit.
   b) What value of resistor is needed to produce the required current?
   c) What is the maximum load impedance for the current mirror to work?
   d) Draw the small signal model.
   e) Calculate $g_m$ and $r_o$ for each of the transistors.
   f) What is the small signal output impedance of the current mirror?
   g) How much current would flow if this current mirror were applied in the forward direction across a diode.
   h) How much current would flow if this current mirror were applied in the reverse direction across a Zener diode with $V_Z=5 \text{V}$?
   i) How much current would flow if this current mirror were applied in the reverse direction across a Zener diode with $V_Z=10 \text{V}$?

4. **Design a common emitter amplifier based on an NPN transistor that is biased with a voltage divider at the base. You have a 10 V source and any resistors or capacitors you need. Your design should be stable for variations in $\beta$ of +/-20%, and for variations in $V_{DD}$ of 0.1 V. Your design target is $I_C=1 \text{ mA}$ and $V_{CE}=4 \text{V}$. You do not need a bypass capacitor at the emitter.**
Design a buffer circuit based on a p-channel FET with a gain of approximately unity, a high input resistance, and a low output resistance. You have a 10 V source and any resistors or capacitors you need. The transistor should have $I_D=5$ mA and $V_{DS}=5$ V.

a) What amplifier design do you choose? Draw the circuit.
b) What values of resistors do you use to properly bias the circuit and to have an input impedance of 10 kΩ?
   Note: there are 3 resistors, excluding source and load.
c) What is the output impedance of this amplifier?
d) What is the open circuit gain $A_{VO}$?
e) Assuming the amplifier is attached to a source with impedance of 1 kΩ, and a load with impedance of 5 Ω, what is the minimum coupling capacitance that can be used at the input and output to have a cutoff frequency of 20 Hz?
f) What would be the gain if a large capacitor is connected across the source resistor?

Design an amplifier based on a CMOS inverter that is biased using a resistive network so that the transistors have maximum DC drain current. It should be designed to have an input impedance of 10 kΩ. You have a 3 V source.

a) Draw the circuit including a resistive bias network.
b) What gate voltage produces the maximum drain current?
c) What is the value of the maximum drain current?
d) What is the value of the resistors at the gate to satisfy the requirements above?
e) At this bias point, what state is each transistor in?
f) What is the value of $g_m$ and $r_o$ for each transistor?
g) Draw the small signal model.
h) What is the output impedance?
i) What is the open circuit voltage gain $A_{VO}$?

Design a common source amplifier based on an n-channel FET using a self-bias approach. You have a 5 V source and any resistors or capacitors you need. The transistor should have $I_D=1$ mA.

a) Draw the circuit.
b) What values of resistors do you use to properly bias the circuit based only on the information above?
c) What is the value of $g_m$ and $r_o$ for this amplifier?
d) Draw the small signal circuit.
e) Assuming that the gate resistor is 30kΩ, find the open circuit gain $A_{VO}$.
f) Find the input and output impedance of this amplifier, assuming the source and load impedance are 50 Ω.
g) Find the cutoff frequency assuming that the input and output capacitors are each 1 nF, and the load and source impedance are each 50 Ω.