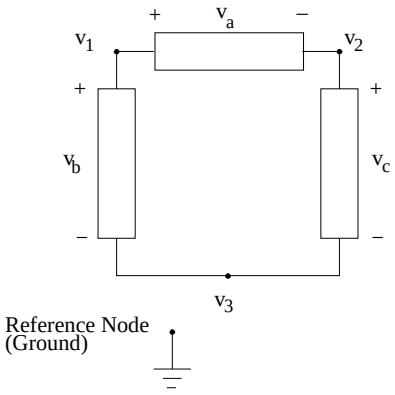
Circuit Analysis Techniques

We learned that KVLs, KCLs, and i-v characteristics equations results in a set of linear equations for the circuit variables (typically $2E$ equations in $2E$ circuit variables where E is number of elements). We learned that we can use i-v characteristics equations when we are marking the circuit variables and reduce the number of equation to be solved to E equations in E unknowns (which is the same as number of KCLs plus KVLs). In this section, we learn two methods, node-voltage and mesh-current, which reduce the number of equations to either number of KCLs or number of KVLs. These are node-voltage and mesh-current methods. They also form the basis to deduce certain properties of linear circuits.

Node-Voltage Method

The node-voltage method is based on following idea. Instead of solving for circuit variables, i and v of each element, we solve for a different set of parameters, node voltages in this case, which automatically satisfy KVLs. As such, we do not need to write KVLs and only need to solve KCLs.

Recall definition of potential. Potential was defined as the voltage between any point and the reference point (usually called ground or common). Take a circuit and identify the nodes on the circuit. Define the node voltage as the potential of that node (voltage between that node and the reference). In the circuit shown, the node voltages are denoted as v_1, v_2, and v_3. The voltage across each element is simply the voltage of the node attached to + terminal of the element minus the voltage of the node attached to − terminal of the element (see page 1 of notes):



$$\begin{aligned} v_a &= v_1 - v_2 \\ v_b &= v_1 - v_3 \\ v_c &= v_2 - v_3 \end{aligned}$$

Note that using node voltage definitions, KVLs will be automatically satisfied:

$$\text{KVL}: \quad -v_b + v_a + v_c = 0$$

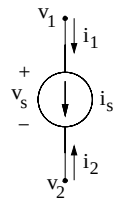
$$-(v_1 - v_3) + (v_1 - v_2) + (v_2 - v_3) = 0 \qquad \rightarrow \qquad 0 = 0$$

As the choice of the reference point (ground) is arbitrary, we can choose the reference point to be any node on the circuit. For example, we could choose node 3 in the above circuit as the reference mode ($v_3 = 0$). The, number of node voltages are reduced to 2. the voltage across the three elements are

$$\begin{aligned} v_a &= v_1 - v_2 \\ v_b &= v_1 \\ v_c &= v_2 \end{aligned}$$

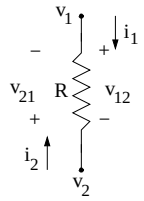
and KVL is still automatically satisfied. With this simplification, we have $N-1$ node voltages in each circuit where N is the number of nodes.

Recall that number of independent KCLs is $N-1$. If we can write the current in each element in terms of the node voltages, then the circuit reduced to $N-1$ KCLs in $N-1$ node voltages. This is straightforward for two of the three linear elements we have encountered up to now:



Current Source: The current flowing through current source is independent of voltage across it and, therefore, is independent of node voltages. From the figure, it is obvious that the current leaving node 1 is $i_1 = i_s$ and current leaving node 2 is $i_2 = -i_s$.

Voltage Source: The voltage across a voltage source is constant and is independent of current flowing through it. The i-v characteristics of the voltage source cannot be used to find the current flowing through it. Voltage sources should be treated in a special manner that will be discussed later.



Resistor: Resistors follow Ohm's Law. We need to calculate the voltage across the resistor first and find the current using the Ohm's Law. Care must be taken as we should use passive sign convention. For example, if we want to find current leaving node 1, i_1, we first find voltage v_{12}:

$$v_{12} = v_1 - v_2 \qquad \rightarrow \qquad i_1 = \frac{v_{12}}{R} = \frac{v_1 - v_2}{R}$$

Alternatively, if we want to find the current leaving node 2, i_2, we calculate v_{21} first:

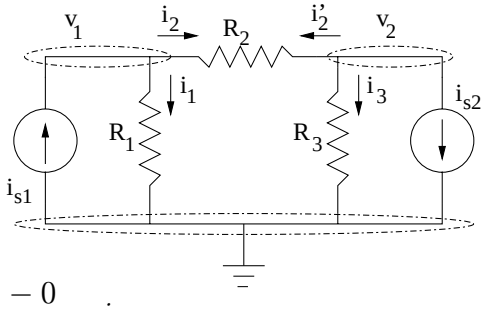
$$v_{21} = v_2 - v_1 \qquad \rightarrow \qquad i_2 = \frac{v_{21}}{R} = \frac{v_2 - v_1}{R}$$

Thus, if a resistor is connected between nodes 1 and 2, the current flowing from node 1 to 2 is $\dfrac{v_2 - v_1}{R}$ and the current flowing from node 2 to 1 is $\dfrac{v_1 - v_1}{R}$

In summary, we have found that we can define node voltages as circuit variables and:
1. Voltage across each element can be written in terms of node voltages.
2. Current through each element (resistor and ICS) can be written in terms of node voltages using the i-v characteristics of that element.
3. KVLs are automatically satisfied.

What is left is a set of KCLs. By using node voltages, we have reduced the number of variables to $N-1$ node voltages (one node is the reference node with zero voltage) and $N-1$ KCLs to solve.

Example:
The circuit has three nodes. We choose the node at the bottom as the reference (ground). The voltages at the other nodes are denoted by v_1 and v_2. We write KCL at these two nodes:



$$\text{KCL 1:} \quad i_2 + i_1 - i_{s1} = 0 \quad \rightarrow \quad \frac{v_1 - v_2}{R_2} + \frac{v_1 - 0}{R_1} = i_{s1}$$

$$\text{KCL 2:} \quad i_{s2} + i_3 + i_2' = 0 \quad \rightarrow \quad \frac{v_2 - 0}{R_3} + \frac{v_2 - v_1}{R_2} = -i_{s2}$$

The above are two equations in two unknowns (node voltages v_1 and v_2). Note that a circuit with 5 elements which, in principle, has 10 circuit variables and 10 equations to be solved is reduced to 2 equations in 2 unknowns.

The previous equations can be rearranged as:

$$v_1\left(\frac{1}{R_1} + \frac{1}{R_2}\right) - v_2\left(\frac{1}{R_2}\right) = i_{s1}$$
$$-v_1\left(\frac{1}{R_2}\right) + v_2\left(\frac{1}{R_2} + \frac{1}{R_3}\right) = -i_{s2}$$

or using the definition of conductance, $G = 1/R$, we have:

$$(G_1 + G_2)v_1 - G_2 v_2 = i_{s1}$$
$$-G_2 v_1 + (G_2 + G_3)v_2 = -i_{s2}$$

In the matrix form, the equations are:

$$\begin{bmatrix} G_1 + G_2 & -G_2 \\ -G_2 & G_2 + G_3 \end{bmatrix} \bullet \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} i_{s1} \\ -i_{s2} \end{bmatrix}$$

This can be generalized to any circuit with N nodes (let $n = N - 1$). The node-voltage equation can be written as

$$\mathbf{G} \bullet \mathbf{v} = \mathbf{i_s}$$

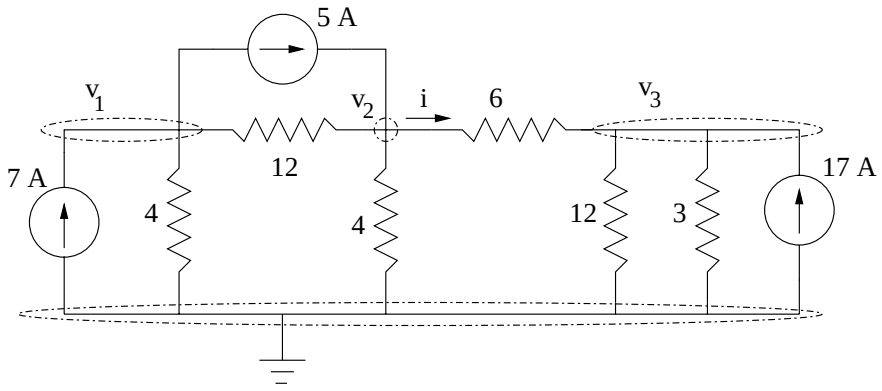
$$\mathbf{G} = \begin{bmatrix} G_{11} & -G_{12} & ... & -G_{1n} \\ -G_{21} & G_{22} & ... & -G_{nn} \\ ... & ... & ... & ... \\ -G_{n1} & -G_{n2} & ... & G_{nn} \end{bmatrix} \qquad \mathbf{v} = \begin{bmatrix} v_1 \\ v_2 \\ ... \\ v_n \end{bmatrix} \qquad \mathbf{i_s} = \begin{bmatrix} i_{s1} \\ i_{s2} \\ ... \\ i_{sn} \end{bmatrix}$$

Matrix $\mathbf{G}$ is called the conductance matrix. If the KCLs are written as sum of current exiting each node, the diagonal elements of this matrix will be positive and the off-diagonal elements will be negative. The diagonal elements G_{ii} are equal to the sum of all conductances connected to node i. The matrix is symmetric, *i.e.* $G_{ij} = G_{ji}$. These off-diagonal elements, G_{ij}, are sum of conductances directly connecting nodes i and j. Array $\mathbf{v}$ is the array of node voltages. Array $\mathbf{i_s}$ is the array of current sources. Element i_{si} is net equivalent of source currents entering the node.

Because of the above features of the node-voltage equations, it is possible to directly write the node voltage equations in the matrix form of $\mathbf{G} \bullet \mathbf{v} = \mathbf{i_s}$ and follow the above rules to construct matrix $\mathbf{G}$ and vectors $\mathbf{v}$ and $\mathbf{i_s}$. Node voltage method is a powerful and simple method. As such, all circuit simulation computer code such as PSpice use node-voltage method and use the above procedure to construct the conductance matrix and the node-voltage equations.

I personally have found that in solving circuits by hand, it is much better to forgo the above direct technique for writing matrix $\mathbf{G}$ and vector $\mathbf{i_s}$ and instead just write down the KCLs as sum of currents existing a node. The chances of mistakes is much reduced and is worth the price of one additional step of rearranging terms to arrive at the above matrix equation. Furthermore, the above procedure should be modified for circuits containing voltage sources. It is just not worth memorizing two additional procedures.

Example: In the circuit below, resistance are given in Ohms. Find i



The circuit has four nodes. Assigning the node at the bottom as the reference node, we write KCL at the three other nodes:

Node 1: $+5 + \dfrac{v_1 - v_2}{12} + \dfrac{v_1 - 0}{4} - 7 = 0$

$(v_1 - v_2) + 3v_1 - 24 = 0 \qquad \rightarrow \qquad 4v_1 - v_2 = 24$

Node 2: $\dfrac{v_2 - v_3}{6} + \dfrac{v_2 - 0}{4} + \dfrac{v_2 - v_1}{12} - 5 = 0$

$2(v_2 - v_3) + 3v_2 + (v_2 - v_1) - 60 = 0 \qquad \rightarrow \qquad -v_1 + 6v_2 - 2v_3 = 60$

Node 3: $-17 + \dfrac{v_3 - 0}{3} + \dfrac{v_3 - 0}{12} + \dfrac{v_3 - v_2}{6} = 0$

$-204 + 4v_3 + v_3 + 2(v_3 - v_2) = 0 \qquad \rightarrow \qquad -2v_2 + 7v_3 = 204$

or

$$\begin{cases} 4v_1 & -v_2 & & = 24 \\ -v_1 & +6v_2 & -2v_3 & = 60 \\ & -2v_2 & +7v_3 & = 204 \end{cases}$$

Note the structure of above matrix equations. The **G** matrix is symmetric. As we wrote the KCLs as the sum of currents exiting the nodes, the diagonal elements are positive and off-diagonal elements are negative. These are good points to check to see if we made a mistake in writing KCLs.

The above equations can be solved to get $v_1 = 12$ V, $v_2 = 24$ V, and $v_3 = 36$ V. We know need to find the problem unknown, i from the node voltages. Using Ohm's law, we get

$$i = \frac{v_2 - v_3}{6} = \frac{24 - 36}{6} = -2 \text{ A}$$

Notes:

1. The above circuit has 8 circuit elements. Node-voltage method results in only 3 equations in 3 unknown. You can try to solve the above circuit with KVL/KCL or circuit reduction techniques to appreciate the power and utility of the node-voltage method.

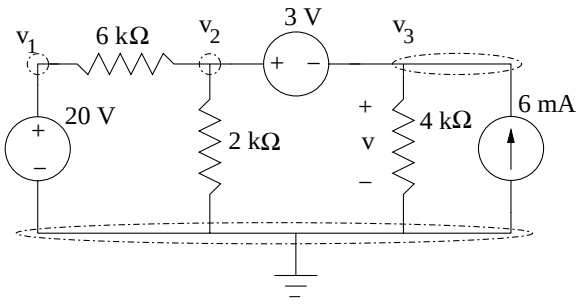
2. In the above circuit, the 12 and 3 Ω resistors are in parallel. The number of node-voltage equations would not have changed if we had replaced these two parallel resistors with their equivalent. So, as a matter of principle, there is no need to replace parallel elements if you are using node-voltage method. It pays, however, to reduce series element as this will eliminate the node between the series elements and reduces the number of equations.

Circuits with voltage sources

Node voltage method as outlined above has to be modified for circuits with voltage sources as the i-v characteristics of IVS does not specify the current through it. This modifications is best explained in the context of the example below:

Example: Find v.

The circuit has four nodes. We will assign the node at the bottom as the reference node and we have three node voltages as unknowns. If we did not have voltage sources, we would write 3 KCL at the 3 nodes to arrive at 3 equations in 3 unknowns. For this circuit, writing KCLs is not useful as the i-v characteristics of IVS does not specify the current through it. We note that there are two possible configuration for voltage sources:



a) Voltage source is connected to the reference node (such as the 20-V IVS in the circuit above). If we write the voltage across the IVS in terms of the node voltages:

$$v_1 - 0 = 20 \qquad \rightarrow \qquad v_1 = 20 \text{ V}$$

In this case, we do not need to write any KCL. The value of node voltage can be derived directly from the i-v characteristics of the IVS!

b) Voltage source is connected between two nodes that are not reference nodes (such as the 3-V IVS in the above circuit). We need to write 2 equations for nodes 2 and 3 (one for each). KCLs for those nodes (2 equations) cannot be used as both contain the current through IVS

that is unknown. One equation is the voltage across the IVS in terms of the node voltages:

$$v_2 - v_3 = 3$$

The second equation can be found by noting that as charge cannot be accumulated in any part in the circuit, KCL should apply to any portion of the circuit. Consider a portion of the circuit including nodes 2, 3 and the 3 V voltage source. We call this portion a supernode. KCL should be valid for a supernode. This gives

$$\text{KCL for super node 2\&3:} \quad -6\times10^{-3} + \frac{v_3}{4\times10^3} + \frac{v_2}{2\times10^3} + \frac{v_2 - v_1}{6^3} = 0$$

$$-72 + 3v_3 + 6v_2 + 2(v_2 - v_1) = 0$$

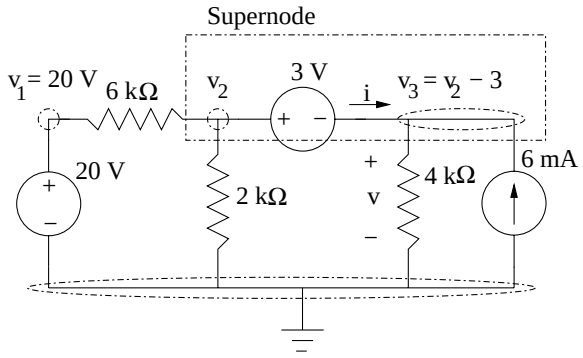
$$-2v_1 + 8v_2 + 3v_3 = 72$$

We now have three equations in three unknowns:

$$\begin{cases} v_1 & & & = 20 \\ & v_2 & -v_3 & = 3 \\ -2v_1 & +8v_2 & +3v_3 & 72 \end{cases}$$

Which gives $v_1 = 20$ V, $v_2 = 11$ V, and $v_3 = 8$ V. The problem unknown $v = v_3 - 0 = v_3 = 8$ V.

Note that most of the work outlined above could be done on the circuit diagram as shown. Noting $v_1 = 20$, we can write the value of the node voltage on the circuit. Also, using $v_2 - v_3 = 3$, we can arrive at $v_3 = v_2 - 3$ as shown in the circuit below.



Now, we only have one unknown, v_2, which can be found by writing KCL on the super node:

$$\text{KCL for super node 2\&3:} \quad -6\times10^{-3} + \frac{v_2 - 3}{4\times10^3} + \frac{v_2}{2\times10^3} + \frac{v_2 - 20}{6^3} = 0$$

The above is one equations in one unknown which can be solved rapidly.

Notes:

1. Voltage sources actually simplify the node voltage equations. By using the i-v characteristic equations of IVS on the circuit diagram, we can reduce the number of unknown node voltages (an, thus, number of equations to be solved) to $N - 1 - N_{IVS}$.

2. The situation is much simpler for voltage sources that are connected between a node and ground (such as 20-V source in the above circuit). As the location of the reference node is arbitrary, a good rule is: Choose the reference node as the node with maximum number of voltage sources attached to it!

3. While we do not need to write KCL at the nodes connected to a voltage node in order to find the node voltages, we need to use KCL if we want to find the current through a voltage source. For example, in the circuit above, current i can be found by writing KCL at node 3 (after we have found all node voltages):

$$-i - 6 \times 10^{-3} + \frac{v_2 - 3}{4 \times 10^3} = 0$$

$$i = -6 \times 10^{-3} + \frac{11 - 3}{4 \times 10^3} = -6 + 2 = -4 \text{ mA}$$

4. In writing Node voltage equations (KCLs), one should ignore the reference directions provided on the circuit for circuit variables (*e.g.* i and v in the above circuit). The node voltage equations are written in terms of node voltages following the above procedure and are independent of these reference directions.

Recipe for Node Voltage Method

1. Identify nodes and supernodes.
   a) Choose the reference node as the one with maximum number of voltage sources attached to it.
   b) Use i-v characteristic equations of IVS to find node voltage values and reduce the number of unknowns

2. Write KCL at each node or supernode.

3. Solve node-voltage equations.

4. Calculate problem unknowns from node voltages. If you need to calculate the current in a voltage source you may have to write KCL at a node connected to that voltage source.