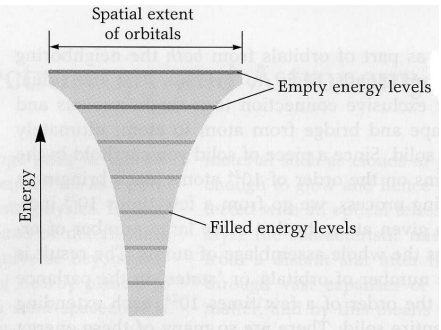
# II. Diodes

We start our study of nonlinear circuit elements. These elements (diodes and transistors) are made of semiconductors. A brief description of how semiconductor devices work is first given to understand their $iv$ characteristics. You will see a rigorous analysis of semiconductors in the breadth courses.

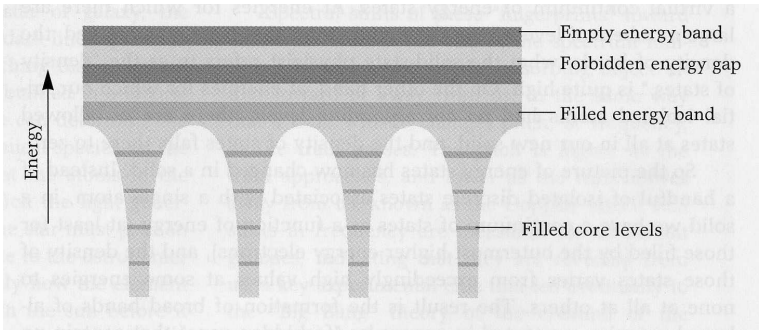
## 2.1 Energy Bands in Solids

In every atom, the nucleus (positively charged) is surrounded by a cloud of electrons. Initially scientists envisioned the atomic structure to be similar to the solar system: the nucleus in the center (similar to the sun), electrons revolving on orbits around the nucleus (similar to planets), and the electric attraction force between the nucleus and electrons being similar to the gravitational force between the sun and planets. However, according to Maxwell's equations, electrons that revolve around a nucleus should emit electromagnetic radiation. As such, the electrons should lose energy gradually and their orbit should decay (in a fraction of a second!). This means that there is a mechanism that would not allow the electrons to lose energy gradually and is one of main reasons that the quantum theory was developed.

According to quantum theory, electrons revolving around an atom can have only discrete levels of energy as is shown below. Electrons are not allowed to gradually lose or gain energy. They can only "jump" from one level to another (by absorbing or emitting a quanta of energy, usually a photon). Furthermore, there are only a finite number of electrons that are allowed in each state (Pauli's Principle). Therefore, both the energy levels for electrons and the number of electrons at each energy level are specified. Because any system would tend to be in a minimum energy state, electrons in an atom start by "filing" the lowest energy level. Once all allowable slots is filled, electrons start filling the next energy level and so on. Therefore, the electronic structure include "filled" energy levels (all slots are taken by electrons), "empty" energy levels (positions are available but no electron is present), and "partially filled" levels (there are some electrons but there is also room for more electrons).




Isolated Atoms

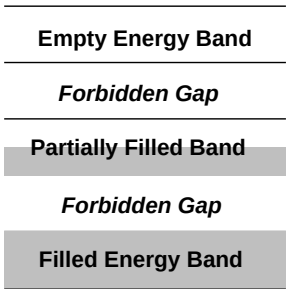



A Solid

When atoms are arranged in a solid, the inter-spacing between atoms can become comparable to the size of electron orbitals of each atom (electrons at each energy level are confined to a region in space called the orbital and the higher energy levels have larger orbital sizes). In this case, the outer orbitals merged into energy bands. Electrons in these bands are not tied to an atom, rather they are free to move around the solid (if space is available per Pauli's Principle). In addition, instead of discrete energy levels, these "shared" electrons can have continuous values of energy within a "band" of energy. As before, there are range of energies that no electron can occupy. These range of energies are called "Forbidden Gaps." (see the figure above).

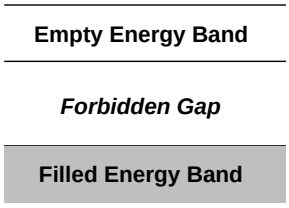
The electric properties of metals, semiconductors, and insulators are can be understood with this picture. As these properties are tied to energy bands and forbidden gaps, we only focus on these regions as are shown in the figure below.

In metals, one of the energy bands is only partially filled. Obviously, all energy bands below (*i.e.,* with lower energies) are completely filled and all energy bands above are completely empty. Electrons in the partially filled band can easily move around the solid with smallest amount of energy as there are lots of spaces available. As such, metals can conduct electricity (and heat) very well.




**Metals**

In a semiconductor, no partially filled band exists. In the filled energy band, there are a lot of electrons, but there are no available slot to move into. In the empty band, there are a lot of slots but no electrons. One would expect that semiconductors to be perfect insulators (for both electricity and heat). However, the size of the forbidden gap in a semiconductor is small. At room temperature, the thermal energy in the material is sufficient to provide sufficient energy to a select number of electrons to move from the filled energy band into the empty energy band.




**Semiconductors**

These electrons that are promoted to the empty energy band now can carry electricity and heat because there are a lot of slots available in this band. In addition, these electrons leave spaces (or "holes") in the originally filled energy band. As such, electrons in the originally filled energy band can also move around the solid by moving from one hole to another hole and participate in the conduction of electricity. Obviously it is easier to keep track of the small number of holes in the filled energy band as opposed to the large number of electrons in that band (it is much easier to find the attendance in a almost full class room by counting the number of empty seats rather the number of students!). In this picture, when electrons move for example to the left to fill a hole, it would look like the hole is moving to the right direction. So, in describing semiconductors we usually keep track of negatively charged

electrons (those that are promoted to the empty energy band) and positively charged holes (spaces left behind).

Since at room temperature the number of electrons that are promoted into the energy band ($\sim 10^{16}$ to $10^{19}$) is much smaller than number of electrons in the partially filled band of a metal ($\sim 10^{28}$ to $10^{29}$), semiconductor conduct electricity but have a much lower conductivity (thus, the name semiconductor). Overall, the properties of semiconductors are very sensitive to temperature as the number of electrons than can "jump" over the Forbidden gap increases exponentially. This is an important effect and should be taken into account in the design of electronic circuits.

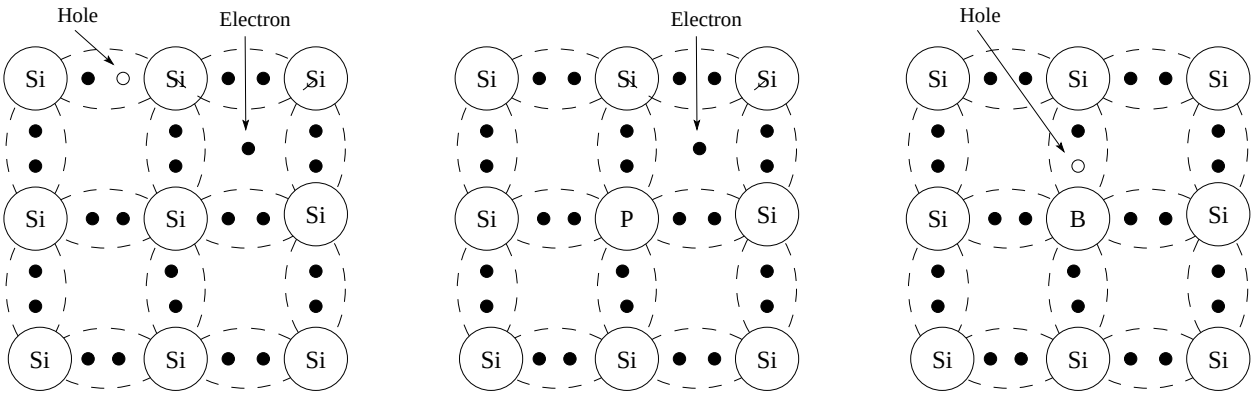
Lastly, insulator have a similar energy band structure as semiconductors (no partially filled band) with one exception. The size of the forbidden gap in an insulator is several time larger than that of a semiconductor. As such, the number of electrons that can be promoted to the energy band is very small ($\sim 10^7$ at room temperature). So, these material are very poor conductors.

## 2.2 Semiconductor Devices

Semiconductor material are mainly made of elements from group IVB of the periodic table like C (diamond), Si, Ge, SiC. These material have 4 electrons in their outer most electronic shell. Each atom can form a "covalent" bond with four of its neighbors sharing one electron with that atom. In this manner, each atom "sees" eight electrons in its outer most electronic shell (4 of its own, and one from each neighbor), completely filling that shell. It is also possible to form this type of covalent bond by combining elements from group IIIB (sharing three electrons) with element from group VB (sharing five electrons). Examples of these semiconductors are GaAs or AlGaAs and are usually called "3-5" semiconductors. We focus mostly on Si semiconductors in this class. Figure below shows this covalent bond structure for Si. A pair of electrons and holes are slow shown. Note that Si form a tetrahedron structure and an atom in the center of the tetrahedron share electrons with atoms on the each vertex. Figure below is a two-dimensional representation of such a structure. The left figure is for a pure Si semiconductor and an electron-hole pair is depicted. Both electrons and holes are called "mobile" carriers as they are responsible for carrying electric current.

If we add a small amount of an element from group VB, such as P, to the semiconductor, we create a n-type semiconductor and the impurity dopant is called a n-type dopant. Each of these new atoms also form a covalent bond with four of its neighbors. However, as a n-type dopant has 5 valance electron, the extra electron will be located in the "empty" energy band. As can be seen, there is no hole associated with this electron. In addition to electrons from the n-type dopant, there are electron-hair pair in the solid from the base semiconductor (Si in

the above figure) which are generated due to temperature effects. In a n-type semiconductor, the number of free electrons from the dopant is much larger than the number of electrons from electron-hole pairs. As such, a n-type semiconductor is considerably more conductive than the base semiconductor (in this respect, a n-type semiconductor is more like a "resistive" metal than a semiconductor).




Pure Semiconductor n-type semiconductor p-type semiconductor

In summary, in a n-type semiconductor there are two charge carriers: "holes" from the base semiconductor (called the "minority" carriers) and electrons from both the n-type dopant and electron-hole pairs (called the "majority" carrier).

Similarly, we can create a p-type semiconductor by adding an element from group IIIB, such as B, to the semiconductor. In this case, the p-type dopant generate holes. We will have two charge carriers: majority carriers are "holes" from the p-type dopant and electron-hole pairs and minority carriers are electrons from the base semiconductor (from electron-hole pairs).

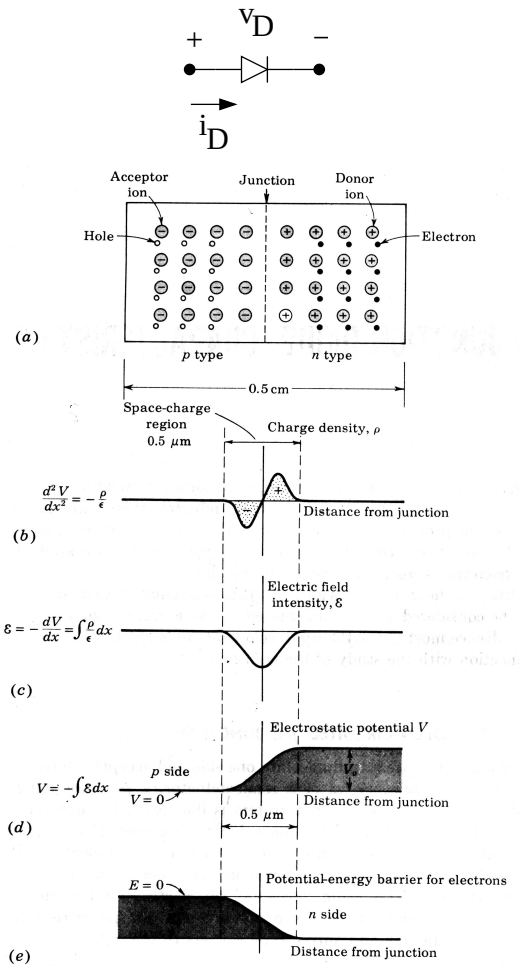
The charge carriers (electrons and holes) move in a semiconductor through two mechanisms: First, charge carriers would move from regions of higher concentration to lower concentration in order to achieve a uniform distribution throughout the semiconductor. This process is called "diffusion" and is characterized by the diffusion coefficient, $D$. Second, charge carriers move under the influence of an electric field. This motion is called the drift and is characterized by the mobility, $\mu$. The ratio of $D$ and $\mu$ is independent of the dopant or the base semiconductor material and is given by Einstein's Equation

$$\frac{D}{\mu} = \frac{kT}{q} \simeq \frac{T}{11,600} \approx V_T$$

where $k$ is the Boltzmann's constant, $T$ is temperature in Kelvin, and $q$ is the electron charge. Parameter $V_T$ is called the "volt-equivalent of temperature" and appears in most semiconductor formulas. At room temperature, $V_T \approx 25$ mV.

## 2.3 The Junction Diode

The simplest semiconductor device is a pn-junction diode as is shown in the figure with p-type material on the left and n-type material on the right and metal contacts are attached to both sides. Circuit symbol for the device is also shown with the "inward" arrow depicting the p-type material side. The convention for the direction of the diode current and the voltage across the diode are also shown.



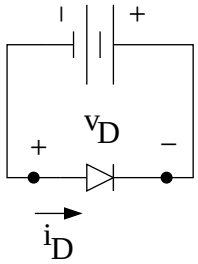

We see that in the n-type material side, there is a large concentration of free electrons. As such, these electrons would like to diffuse to the p-side where there are few electrons. Similarly there is a large concentration of holes in the p-type material and they would like to diffuse to the n-type material side. When these electrons and holes meet in the vicinity of the junction, they combine and are neutralized. Since this region is "depleted" of mobile carriers, it is called the "depletion" region (also referred to as the "transition" or "space-charge" region). The width of this region is small, typically $\sim 0.5\mu$m.

Since the n-type material has lost electrons, it becomes positively charged. Similarly the p-type material becomes negatively charged. As a result, an electric potential and an electric field appears across the depletion region. This electric field (or the voltage barrier) impedes the flow of electrons from the n-type material and flow of holes from the p-type material. The height of this voltage barriers is related to the forbidden gap of the base semiconductor material (and not the amount of dopant).

### *iv* Characteristics

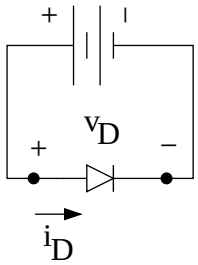
Let us attach a voltage source to this junction diode such that the positive terminal of the voltage source is attached to the n-type material. This configuration is called reverse bias. In this case, some of the free electrons from the n-type material will travel to the voltage sources making the n-type material side more positively charged. Similarly, some of the holes from the p-type material would go the voltage source, making the p-type material more negatively charged. As a result, the depletion region becomes wider and the height of the potential barrier increases and no majority carriers can cross the depletion region.

A small current however, flows in the circuit because of the minority carriers. On the n-type material side, electron-hole pair are created due to thermal energy. Electrons move to the voltage source and holes move to the depletion region. Similarly, on the p-type material side, electron-hole pairs are created, holes are neutralized by electrons from the voltage source and electrons move to the depletion region. These electrons from the p-type material and holes from the n-type material (minority carriers) combine in the depletion region leading to the flow of a net current which is called the reverse saturation current, $I_s$. In the circuit above, $i_D = -I_s$. $I_s$ is very small: at room temperature it is about several nA ($10^{-9}$A) for Si semiconductors. Value of $I_s$ strongly depends on the temperature (as it is related to the electron-hole production rate) – $I_s$ doubles for every increase of $\sim 7$°C in temperature.



Reverse Bias

Now, let us attach the voltage source to the diode such that the positive terminal is attached to the p-type material. This configuration is called forward bias.



Forward Bias

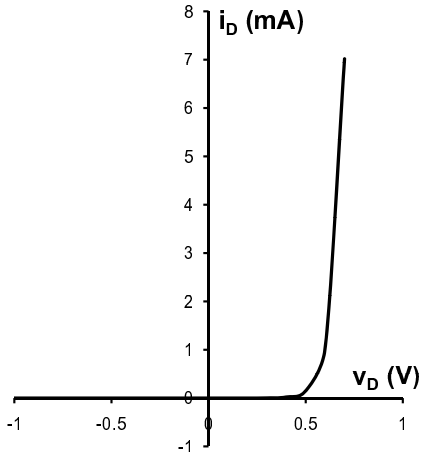
Electrons are injected into the p-type material making that region less positively charged while electrons are taken from the n-type material making it less negatively charged. As a result, the depletion region become thinner and the height of the potential barrier decreases. In this case the diffusion process can gradually overcome the force of the electric field and some of majority carriers can cross the junction and a positive current flows through the diode. As the voltage source voltage is increased, the potential barrier height become smaller leading to larger and larger currents (diode current increases exponentially with the applied voltage).

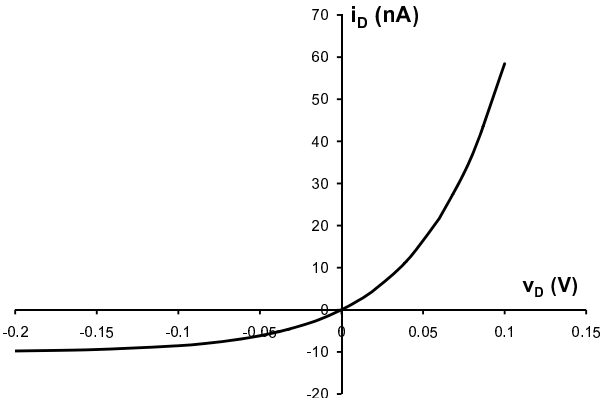
The *iv* characteristics of a junction diode is given by:

$$i_D = I_s \left( e^{v_D/nV_T} - 1 \right)$$

where the constant $n$ is called the "emission coefficient" (For Si, $n = 2$ for discrete diodes and $1 \leq n \leq 2$ in ICs). Figure below (left) shows the plot of $i_D$ versus $v_D$ for a typical Si diode. Note that because $I_s$ is very small (nA range), $v_D$ should become large enough such that large value of $exp(v_D/0.05)$ compensate for the small value of $I_s$. As can be seen, the diode current sharply rises when $v_D$ is in the range of 0.6 to 0.7 V.

While, the above model indicates that a current of $-I_s$ flows in the diode that is reversed biased, typically the diode current is much larger (*e.g.,* $\mu$A versus 10s of nA) because of "leakage" currents (*e.g.,* current flowing through an oxide layer covering both p and n semiconductors). This reversed-bias current, however, is still small and is usually ignored.




**Diode Limitations:** In the forward bias region, the power $P = i_D v_D$ is dissipated in the diode in the form of heat. The diode packaging provides for the conduction of this heat to the outside and diode is cooled by the air. If we increase $v_D$ (or $i_D$) diode is heated more. At some point, the generated heat is more than capability of the diode package to conduct it away and diode temperature rises dramatically and diode burns out. As $v_D$ changes slowly, this point is usually characterized by the current $i_{D,max}$, maximum forward current, and is specified by the manufacturer.

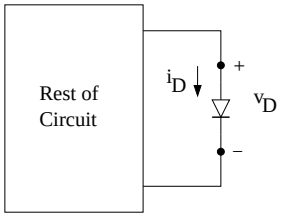
Heat generation is not a problem in the revers bias as $i_D \simeq 0$ (and, thus, $P \simeq 0$). However, if we increase the reverse bias voltage, at some voltage, a large current can flow through the diode. This voltage is called the reverse breakdown voltage or the Zener voltage.

This large reverse current is produced through two processes. First, in the reverse bias, minority carriers enter the depletion region. These minority carriers are accelerated by the voltage across the depletion region. If the reverse bias voltage is high enough, these minority carrier can accelerate to a sufficiently high energy, impact an atom, and disrupt a covalent band, thereby generating new electron-hole pairs. The new electron-hole pairs can accelerate, impact other atoms and generate new electron-hair pairs. In this manner, the number of minority carriers increases exponentially (an avalanches process), leading to a large reverse current. This is called the avalanche breakdown. Second, when the strength of the electric field across the junction becomes too large, electrons can be pulled out of the covalent bonds directly, generating a large number of electron-hole pairs and a large reverse current. This is known as the Zener effect or Zener breakdown.

Regular diodes are usually destroyed when operated in the Zener or reverse breakdown regions. These diode should be operated such that $v_D > -V_Z$. A special type of diodes, Zener diodes, are manufactured specifically to operate in the Zener region. We will discuss these diodes later. In Zener diodes, heat generation sets a maximum for the allowable diode current in the Zener region.

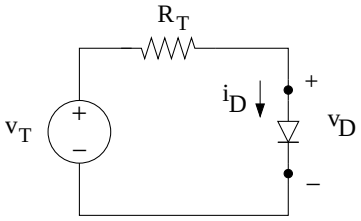
## 2.4 Solving Diode Circuits

With diode $iv$ characteristic in hand, we now attempt to solve diode circuits. Consider any linear circuit with a diode. The box labeled "the rest of the circuit" in the figure can be replaced by its Thevenin equivalent, giving the simple diode circuit below.




Because the three elements are in series, current $i_D$ flows through all elements. Writing KVL around the loop we have:

$$v_T = i_D R_T + v_D$$




This is an equation with two unknowns ($i_D$ and $v_D$) as $v_T$ and $R_T$ are known. The second needed equation (to get two equations in the two unknown) is the diode characteristic equation:

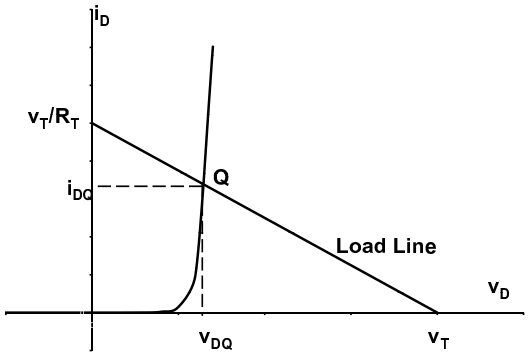
$$i_D = I_s \left( e^{v_D / n V_T} - 1 \right)$$

The above two equations in two unknown cannot be solved analytically as the diode $iv$ equation is non-linear. PSpice solves these equations numerically. As analytical solutions can provide insight in the circuit behavior and may be also needed for circuit design, we develop two methods to solve diode circuits without numerical analysis.

### 2.4.1 Load Line

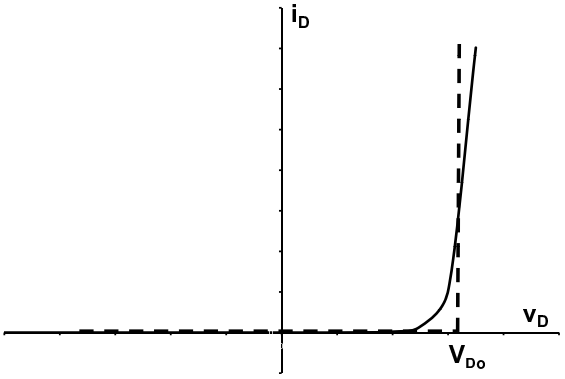
The $iv$ characteristic of the diode is plotted in the figure. The $i_D$ and $v_D$ values of any point on the curve satisfies the diode equation above. Also plotted is the line representing $V_T = i_D R_T + v_D$. This line is called the "load line." The $i_D$ and $v_D$ values of any point on the load line satisfies the first equation above. Since the solution to the above two equations in two unknowns is a pair of $i_D$ and $v_D$ that satisfies both equations, such a point should be both on the $i_v$ plot of the diode and on the load line, *i.e.,* at the intersection of the two. This point is called the Q-point or the Quiescent point (or the operating point) of the diode.

The load line technique is not accurate in finding numerical values of $i_D$ and $v_D$. However, it is a powerful tool to get qualitative measures of the circuit behavior *e.g.,* ensuring that the diode operating point is safety away from the maximum forward current.



### 2.4.2 Piecewise Linear Model

The problem in arriving at an analytical solution to the diode circuit is that the diode $iv$ equation is nonlinear. An approach would be to try to "approximate" the diode $iv$ equation by a linear equation (*i.e.,* the diode $iv$ characteristics curve with a line).




As can be seen from the figure, it is NOT possible to approximate the $iv$ characteristics curve with ONE line. However, it is possible to do so with TWO (or more) lines. This type of approximation is called a piecewise linear model, *i.e.,* pieces of the curve are replaced by lines. One such model for diodes is shown in the figure with equations:

**Diode ON:** $v_D = V_{D0}$ and $i_D \geq 0$

**Diode OFF:** $i_D = 0$ and $v_D < V_{D0}$

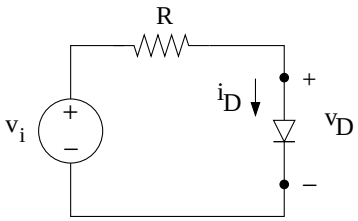
Parameter $V_{D0}$ is called the "cut-in" voltage and it is related to the forbidden gap of the base semiconductor (not what dopant is used and how much). For Si, $V_{D0} \approx 0.6 - 0.7$ V. For GaAs, $V_{D0} \approx 1.7 - 1.9$ V. Each equation is valid for a range of parameters (*e.g.,* "Diode ON" equation is valid only if $i_D > 0$). Also, the point with $v_D = V_{D0}$ and $i_D = 0$ is located on both Diode ON and Diode OFF lines (in the above equations, that point is added to the diode ON case).

An issue that arises in solving circuits with diodes is that we do not know *a priori* the state of the diode (ON or OFF) and so we do not which equation to use. The following "recipe" can be used to solve diode equations:

*Recipe for solving diode circuits:*

1. Write down all circuit equation with $i_D$ and $v_D$ as parameters and simplify as much as possible.
2. Assume diode is in one state (either ON or OFF). Use the diode equation for that state to solve the circuit equations and find $i_D$ and $v_D$.
3. Check the range of validity inequality with the values of $i_D$ and $v_D$ that was found. If $i_D$ and $v_D$ values satisfy the range of validity, the assumption was correct. Otherwise, the assumed diode state is incorrect. Go to step 2 above and assume that the diode is in the other state.

Let's use this method for the Si diode ($V_{D0} = 0.7$ V) circuit shown with $v_i = 5\ V$ and $R = 1$ k$\Omega$.




*Step 1:* KCL tells that current $i_D$ flow in all elements and by KVL:

$$v_i = i_D R + v_D \quad \rightarrow \quad 5 = 10^3 i_D + v_D$$

*Step 2:* Assume diode is OFF, $i_D = 0$ and $v_D < V_{D0}$. Substituting for $i_D = 0$ in the circuit equation, we get:

$$5 = 10^3 \times 0 + v_D \quad \rightarrow \quad v_D = 5 \text{ V}$$

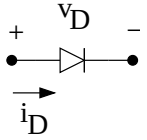
*Step 3:* Since $v_D = 5 > 0.7 = V_{D0}$, diode $v_D$ does NOT satisfy range of validity and the assumed diode state is incorrect.

*Step 2:* Assume diode is ON, $v_D = V_{D0}$ and $i_D \geq 0$. Substituting for $v_D = V_{D0} = 0.7$ V in the circuit equation, we get:

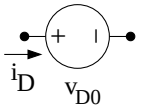
$$5 = 10^3 \times i_D + 0.7 \quad \rightarrow \quad i_D = 4.3 \text{ mA}$$

*Step 3:* Although we know that since diode was not OFF, it should be ON, it is a good practice to check in case we might have made a math mistake. For this case, $i_D > 0$ and satisfies the range of validity. So diode is ON and $v_D = 0.7$ V and $i_D = 4.3$ mA.

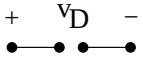
**Diode circuit Model:** The above method can become cumbersome if we have a complicated circuit and/or several diodes as it is not straightforward to use advanced circuit solution methods (node-voltage, mesh current). Another approach would be to use circuit models (instead of equation) for the diode as is shown below:




**Diode ON:** $i_D \geq 0$




**Diode OFF:** $v_D < V_{D0}$,

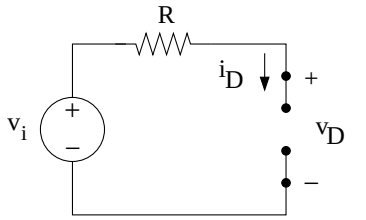



If you use the above circuit models, we need to modify our recipe for solving diode circuits accordingly:

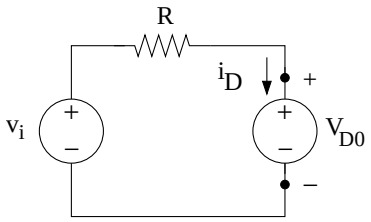
*Recipe for solving diode circuits with diode circuit models:*

1. Draw a circuit for each state of the diode (If more than one diode, you should draw circuits to all possible combinations of states of diodes).
2. Solve each diode circuit and find $i_D$ and $v_D$.
3. Check the range of validity inequality with the values of $i_D$ and $v_D$ that was found. If $i_D$ and $v_D$ values satisfy the range of validity, the assumption was correct. Otherwise, the assumed diode state is incorrect. Go to step 2 above and start with another circuit.

As an example, let's solve the diode circuit of the previous page ($v_i = 5\ V$ and $R = 1$ k$\Omega$) with this method:




**Diode OFF:** from the circuit by KVL, $v_D = v_i = 5$ V. Since $v_D > V_{D0} = 0.7$ V, our assumption is not correct.



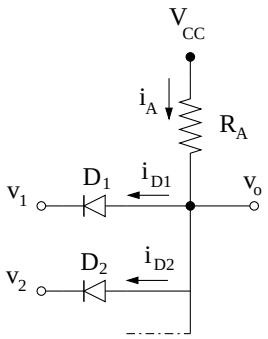

**Diode ON:** from the circuit by Ohm's Law, $i_D = (v_i - V_{D0})/R = 4.3$ mA. Since $i_D > 0$, our assumption is correct.

Therefore, the diode is ON with $v_D = 0.7$ V and $i_D = 4.3$ mA.

## 2.5 Diode Logic Gates

You have seen binary mathematics and logic gates in ECE25. We will explore some electronic logic gates in this course. Binary mathematics is built upon two states: 0, and 1. We need to relate the binary states to currents or voltages as these are parameters that we can manipulate in electronic circuits. Similar to our discussion of analog circuits, it is advantageous (from power point of view) to relate these the binary states to voltages. As such, we "choose" two voltages to represent the binary states: $V_L$ for state 0 or Low state and $V_H$ for state 1 or High state (for example, 0 V to represent state 0 and 5 V to represent state 1). These voltages are quite arbitrary and can be chosen to have any value. We have to be careful as it is extremely difficult, if not impossible, to design an electronic circuit to give exactly a voltage like 5 V (what if the input voltage was 4.99 V?). So, we need to define a range of voltages (instead of one value) to represent high and low states. We will discuss logic gates more thoroughly in the transistor section. Here, we consider a simpler diode logic gate.

**Diode AND Gate:** To study the behavior of the gate we will consider the state of the circuit with $V_{CC} = 5$ V and $R_A = 1$ kΩ for different values of $v_1$ and $v_2$ (either 0 or 5 V corresponding to low and high states). We also assume that in the output any voltage $< 1$ V would be considered a low state and any voltage $> 4$ V is considered a high state. We note that by KCL, $i_A = i_{D1} + i_{D2}$ (assuming that there is no current drawn from the circuit).




Case 1, $v_1 = v_2 = 0$:

Since the 5-V supply ($V_{cc}$) will tend to forward bias both $D_1$ and $D_2$, let's assume that both diodes are forward biased. Thus, $v_{D1} = v_{D2} = V_{D0} = 0.7$ V and $i_{D1} \geq 0$, $i_{D2} \geq 0$. Then,

$$v_o = v_1 + v_{D1} = v_2 + v_{D2} = 0.7 \text{ V}$$
$$i_A = \frac{V_{CC} - v_o}{R_A} = \frac{5 - 0.7}{1,000} = 4.3 \text{ mA}$$

Current $i_A$ will be divided between two diodes by KCL, each carrying one half of $i_A$ (because of symmetry). Thus, $i_{D1} = i_{D2} = 2.1$ mA. Since diode currents are positive, our assumption of both diode being forward biased is justified and, therefore, $v_o = 0.7$ V.

So, when $v_1$ and $v_2$ are low, $D_1$ and $D_2$ are ON and $v_o$ is low.

Case 2, $v_1 = 0, v_2 = 5$ V:

Again, we note that the 5-V supply ($V_{cc}$) will tend to forward bias $D_1$. Assume $D_1$ is ON: $v_{D1} = V_{D0} = 0.7$ V and $i_{D1} \geq 0$. Then:

$$v_o = v_1 + v_{D1} = 0.7 \text{ V}$$
$$v_o = v_2 + v_{D2} \quad \rightarrow \quad v_{D2} = -4.3 \text{ V} < V_{D0}$$

and $D_2$ will be OFF ($i_{D2} = 0$). Then:

$$i_A = \frac{V_{CC} - v_o}{R_A} = \frac{5 - 0.7}{1,000} = 4.3 \text{ mA}$$
$$i_{D1} = i_A - i_{D2} = 4.3 - 0 = 4.3 \text{ mA}$$

Since $i_{D1} > 0$, our assumption of $D_1$ forward biased is justified and, therefore, $v_o = 0.7$ V.

So, when $v_1$ is low and $v_2$ is high, $D_1$ is ON and $D_2$ is OFF and $v_o$ is low.

Case 3, $v_1 = 5$ V, $v_2 = 0$ V:

Because of the symmetry in the circuit, this is exactly the same as case 2 with roles of $D_1$ and $D_2$ reversed.

So, when $v_1$ is high and $v_2$ is low, $D_1$ is OFF and $D_2$ is ON and $v_o$ is low.

Case 4, $v_1 = v_2 = 5$ V:

Examining the circuit, it appears that the 5-V supply ($V_{cc}$) will NOT be able to forward bias $D_1$ and $D_2$. Assume $D_1$ and $D_2$ are OFF: $i_{D1} = i_{D2} = 0$, $v_{D1} < V_{D0}$ and $v_{D2} < V_{D0}$. Then:

$$i_A = i_{D1} + i_{D2} = 0$$
$$v_o = V_{CC} - i_{D1}R_A = 5 - 0 = 5 \text{ V}$$
$$v_{D1} = v_o - v_1 = 5 - 5 = 0 < V_{D0} \qquad \text{and} \qquad v_{D2} = v_o - v_2 = 5 - 5 = 0 < V_{D0}$$

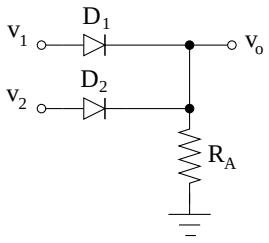
Thus, our assumption of both diodes being OFF are justified.

So, when $v_1$ and $v_2$ are high, $D_1$ and $D_2$ are OFF and $v_o$ is high.

Overall, the output of this circuit is high only if both inputs are high (Case 4) and the output is low in all other cases (Cases 1 to 3). Thus, this is an AND gate. This analysis can be easily extended to cases with three or more diode inputs.

This is actually not a good gate as for input we used low states of 0 V and the output low state was 0.7 V. We need to make sure that the input low state voltage is similar to the output low state voltage so that we can put these gates back to back. (You can easily show that if we had assumed low states of 0.7 V for input, the output low state would have been 1.4 V.) This gate is not usually used by itself but as part of diode-transistor logic gates that we will discuss in the BJT section.

**Exercise:** Show that this is an OR gate.




## 2.6 Parametric solution of diode circuits

In the diode circuits above, we need to know the value of all of the elements in order to find the state of the diode and currents and voltages in the circuit. This is cumbersome as, for example if in the simple diode circuit of page 2-10, if the input voltage $v_i$ was changing in time, we need to solve the diode circuit for ALL values of $v_i$.

It is very useful if we can derive the circuit solution parametrically, *i.e.,* with values of various circuit elements, in particular, the input voltage as parameters. This approach would allows us to solve the circuit ONCE. The problem is that diode can be either of its two states which, in principle, depend on the values of circuit parameters ($v_i$ and $R$ in the example above).

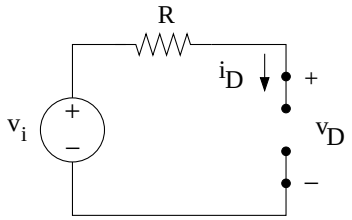
The approach to do this is to assume that the diode is one specific state and find the range of circuit parameters (*e.g.,* range of $v_i$) that would result in the diode being in that state. In this manner, we will have multiple solutions for $v_o$, each valid for range of $v_i$.

*Recipe for solving diode circuits parametrically:*

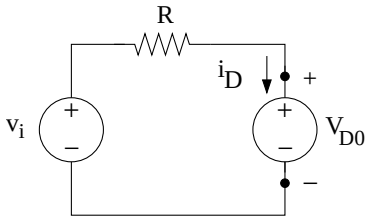
1. Draw circuits covering all possible diode states ($2^n$ states, where $n$ is the number of diodes)
2. Solve each circuit and find currents and voltages.
3. Use the range of validity of the diode states for that circuit to find the range of circuit parameters which leads to that state.

For example, consider the diode circuit discussed before with $v_i$ as a parameter. Following our recipe we get:

**Diode OFF:** from the circuit by KVL, $v_D = v_i$.
For diode OFF, we need $v_D < V_{D0}$ or $v_i < V_{D0}$. Therefore, when $v_i < V_{D0}$, diode will be OFF and $v_D = v_i$.




**Diode ON:** from the circuit by Ohm's Law, $i_D = (v_i - V_{D0})/R$.
For diode ON, we need $i_D \geq 0 \rightarrow (v_i - V_{D0})/R \geq 0$ or as $R$ is positive, $v_i - V_{D0} \geq 0$.




Therefore, the parametric solution of the circuit can be summarized as:

$$\text{When} \quad v_i \geq V_{D0} \quad \rightarrow \quad \text{Diode is ON} \quad \rightarrow \quad v_D = V_{D0} \quad \text{and} \quad i_D = \frac{v_i - V_{D0}}{R}$$

$$\text{When} \quad v_i < V_{D0} \quad \rightarrow \quad \text{Diode is OFF} \quad \rightarrow \quad v_D = v_i \quad \text{and} \quad i_D = 0$$

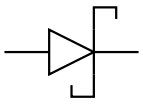
Note that if we had solved the circuit parametrically first, we could get the answer for the case $v_i = 5$ V and $R = 1$ kΩ immediately: $v_i = 5$ V $> V_{D0} = 0.7$ V, therefore, diode is ON, $v_D = V_{D0} = 0.7$ V and $i_D = (5 - 0.7)/10^3 = 4.3$ mA.

We will use the above method to explore some diode circuits later.

## 2.7 Other Types of Diodes

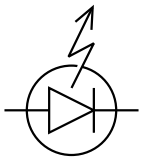
Three other types of diodes are in wide use. They include:

**Schottky Barrier Diode**: Schottky barrier diodes are formed by putting a metallic surface in contact with n-type semiconductors. This type of diode has a much larger $I_s$ and, therefore, will go into forward-bias at $V_{D0} \approx 0.3$ V. Because majority carriers do not have to diffuse toward the contact point, Schottky diodes have a much faster switching speed and are used in digital circuits like transistor-transistor logic (TTL). The circuit symbol for a Schottky diode is similar to a junction diode but with the cathode vertical line modified to resembled an S.



Schottky Diode

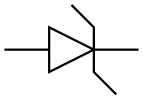
**Light-Emitting Diode (LED)**: This type of diode emits light when it is forward biased. In order to have a visible light output, the band gap of the semiconductor should be larger then Si. Thus, these diodes are typically made of types III-V semiconductors (*e.g., GaAs*). As such, they have a much larger $V_{D0}$ between 1.7 to 1.9 V.



LED

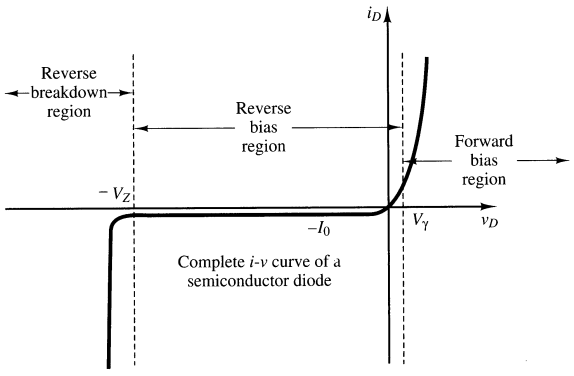
Both Schottky diodes and LEDs are similar to regular junction diodes (with the exemption of $V_{D0}$ value) and the pierce linear model and analysis tools developed above can be applied.

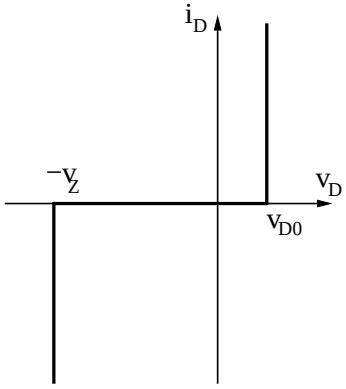
**Zener Diodes:** Zener diodes are specially manufactured to operate in the Zener region. In these diode, heavily doped regions are manufactured near the metal contacts to the semiconductor. The high density of charge carriers allows a substantial reverse breakdown current to be sustained. These diodes are useful in applications where a constant value of voltage is necessary, for example, in voltage regulators.



Zener Diode

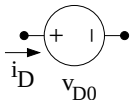
The *iv* characteristics of Zener diodes and their piecewise linear model are shown below:



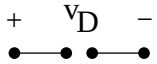



The piecewise linear characteristics equations are:

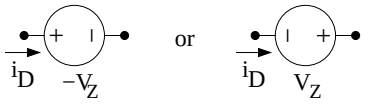
**ON:** $v_D = V_{D0}$ and $i_D \geq 0$




**OFF:** $-V_z < v_D < V_{D0}$ and $i_D = 0$




**Zener Region:** $v_D = -V_Z$ and $i_D \leq 0$



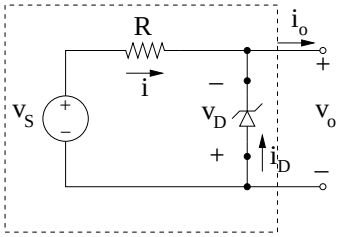

Circuit solution techniques for junction diodes can be applied to Zener diodes. The only change is that Zener diodes has three states (instead of two for regular diodes).

### 2.7.1 A simple Power Supply

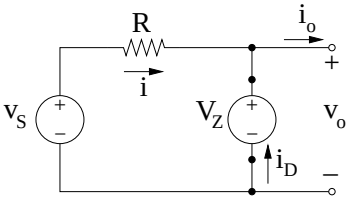
An independent voltage source is a circuit in which the output voltage is constant regardless of the current drawn from the circuit. In some cases, we have a voltage source and its voltage changes like a battery as battery ages or the output voltage of the rectifier circuit (discussed later) which even with a capacitor exhibit some "ripple".

This circuit makes such a "slightly" varying DC voltage source (denoted by $v_s$) into an independent voltage source, *i.e.,* the output voltage, $v_o$, is constant for a range of $i_o$'s.

Circuits like this are two-terminal networks or circuits that we discussed in Sec. 1. In principle, we are interested to compute $v_o$ in terms of $i_o$ (or vice versa) as such information will allow us to compute $i_o$ and $v_o$ for any "load" that it is attached to the circuit without solving the circuit in the box again. We will use the parametric method to analyze this circuit.




*Case 1: Diode is in the Zener region.* The equivalent circuit is shown and we need to have $i_D < 0$. KVL in the right loop gives:




KVL: $v_o = V_Z = const$

So as long as the diode is in the Zener region, the output voltage will be constant regardless of the value of $i_o$. Therefore, this circuit will act as an independent voltage source.

To find the range of parameters for which the diode remains in the Zener region ($i_D \leq 0$), we note:

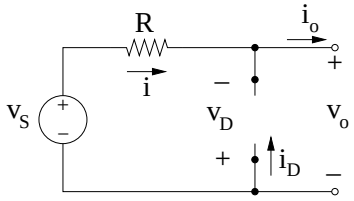
$$\text{KCL:} \quad i_D = i_o - i$$

$$\text{KVL:} \quad v_s = Ri + V_Z$$

$$i_D = i_0 - \frac{v_s - V_Z}{R} \leq 0 \qquad \rightarrow \qquad i_o \leq \frac{v_s - V_Z}{R}$$

Therefore, as long as $i_o$ is smaller than the value $i_{o,max} = (v_s - V_Z)/R$, the diode would remain in the Zener region and the circuit would act as an independent voltage source.

*Case 2: Diode is in the reverse bias region.* The equivalent circuit is shown and we need to have $-V_Z < v_D < V_{D0}$. Because $i_D = 0$, KCL gives $i = i_o$. Then, KVL in the outer loop gives:




$$\text{KVL:} \quad v_s = Ri_o + v_o \qquad \rightarrow \qquad v_o = v_s - Ri_o$$

Therefore, the output voltage drops as more current is drawn from the circuit.

To find the range of parameters for which the diode remains in the reverse bias region ($-V_Z < v_D < V_{D0}$), we note: $v_o = -v_D$. Thus:

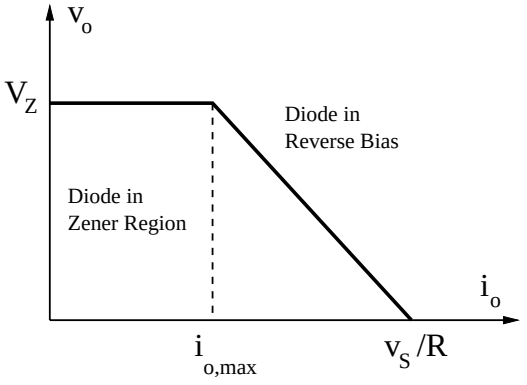
$$-V_Z < -v_o < V_{D0}$$

$$-V_Z < -(v_s - Ri_o) < V_{D0} \qquad \rightarrow \qquad \frac{v_s - V_Z}{R} < i_o < \frac{v_s + V_{D0}}{R}$$

**Exercise:** Show that if $v_s > 0$, $i_{o,max} < i_o \leq v_s/R$ (Hint: $v_o$ cannot become negative).

*Case 3: Diode is in the forward bias region.* Since $v_s > 0$, the diode CANNOT be in the forward bias region.

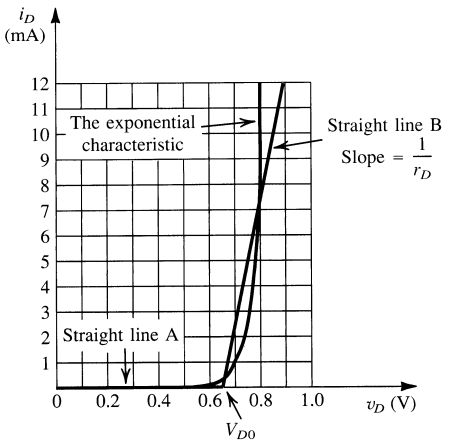
The $i_o v_o$ characteristics of this circuit is shown in the figure. The circuit resembles an independent voltage source with a strength of $V_Z$ as long as the diode remains in the Zener region (*i.e.,* $i_o < (v_s - V_Z)/R = i_{o,max}$). In practice, because $V_Z$ changes slightly when the diode current changes, the output voltage of circuit ($V_Z$) changes slightly. Much better power supply circuits can be build by addition of a transistor or OpAmps to the circuit



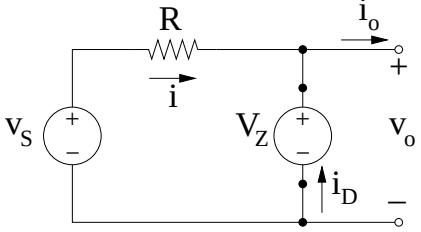
## 2.8 Other Diode Models

In this section, we introduced a piecewise linear model for the diode in order to facilitate circuit analysis and specially circuit design. This was done by approximating the diode $iv$ characteristics by two lines: one for ON state and one for OFF state. Many choices for these model "lines" are possible. The piecewise linear model developed and used before is sometimes referred to as "the constant voltage" model to differentiate it from other piecewise linear models.

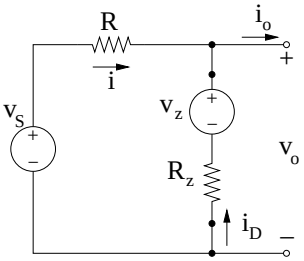
Figure shows another model in which the ON region is approximated with a "sloped" line. In this case, two parameters, $V_{D0}$ and $R_D$, are necessary: $v_D = V_{D0} + i_D R_D$. The corresponding circuit model is a voltage source $V_{D0}$ in series with a resistor $R_D$ with $R_D$ typically a few to tens of Ohm. This model is not often used as a) a large set of $V_{D0}$ and $R_D$ can be chosen and best choice actually depends on the operating point of the diode (which is not known a priori), and b) the increase in the amount of work for analyzing the circuit does not usually justify any improvement in the accuracy. This model, however, is useful in understanding certain features of the circuits as discussed below. Note that $R_D$ is typically 10's $\Omega$




Similarly for a Zener diode, the Zener region can be modeled with a combination of a voltage source $(-V_{Z0})$ and a resistor $R_Z$. We will analyze the simple Zener-diode power supply circuit page 39 to show how this model is utilized. Note that we are still using the same model for the reverse-bias region ($i_D = 0$ and $-V_{Z0} < v_D < V_{D0}$). Thus, the analysis of page 40 for this region remains valid and is not repeated here.




*Case 1: Diode is in the Zener region.* The equivalent circuit is shown and we need to have $i_D < 0$. KCL and KVL in the left loop give:




KCL: $\quad i_D + i = i_o$

KVL : $\quad v_s = Ri + V_{Z0} - R_Z i_D$

Since we want to find $v_o$ in terms of $i_o$ ($i_o$, $R$, $V_{Z0}$, and $R_Z$ are known), above are two equations in two unknowns ($i_D$ and $i$) and can be solved to get:

$$i_D = -\frac{v_s - V_{Z0} - Ri_o}{R + R_Z}$$
$$i = \frac{v_s - V_{Z0} + R_Z i_o}{R + R_Z}$$

Condition of Zener diode being in the Zener region ($i_D < 0$) leads to $i_o < (v_s - V_{Z0})/R$ which is the same as the result from our constant-voltage model of page 39. We can find $v_o$ by KVL in the right loop:

$$v_o = V_{Z0} + R_Z \times \frac{v_s - V_{Z0} - Ri_o}{R + R_Z}$$
$$v_o = \frac{RV_{Z0} + R_Z v_s}{R + R_Z} - \frac{RR_Z}{R + R_Z}\, i_o$$
$$v_o = \hat{V}_Z - (R \parallel R_Z)\, i_o$$

with $\hat{V}_Z = (RV_{Z0} + R_Z v_s)/(R + R_Z)$. The expression above can be simplified greatly by assuming $R_Z \ll R$ (*i.e.*, $R \parallel R_Z \approx R_Z$ and $\hat{V}_Z$ is "slightly larger than $V_{Z0}$):

$$v_o = \hat{V}_Z - R_Z i_o$$

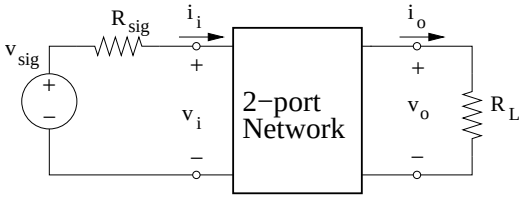
which means that the output voltage is slowly decreasing with the value of $i_o$ and in fact the circuit resembles a combination of an independent voltage source $\hat{V}_Z$ and a resistor $R_Z$. As can be seen, the more complicated model for the Zener diode and longer analysis has illuminated slight changes in the circuit behavior.

Final notes: 1) PSpice uses full diode expression as it is far easier and more accurate to solve non-linear equations with the computer as opposed to consider different states (and solve multiple circuits) with approximate models. 2) We will consider the concept of dynamic resistance of the diode in the transistor amplifier section.

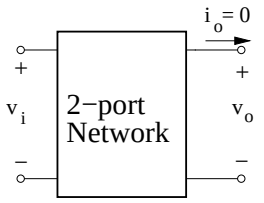
## 2.9 Wave-form Shaping Circuits

In this section, we examine several popular diode circuits. These circuit are generally called wave-form shaping circuits as the diode is utilized to "modify" the input voltage wave-form. Circuits like these are two-port networks that we discussed in Sec. 1. As discussed in Sec. 1, we only need to solve the circuit below for two-port networks if the circuit is linear. (Note: the circuit below is correct even if the two-port network itself can contain non-linear elements as long as the rest of the circuit is linear)

We are interested to compute $v_o$ as a function of $v_i$ as such a function allows us to compute $v_o$ for any value of $v_i$ without analyzing the circuit for each $v_i$ value (for example for a time-dependent $v_i$). The relationship between $v_o$ and $v_i$ is usually referred to as the transfer function of the circuit.

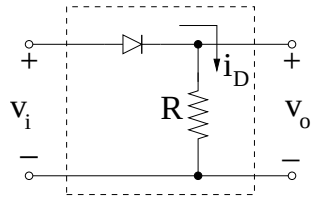



Circuit analysis is greatly simplified if $R_L \to \infty$ (or $i_o = 0$). This case is called the "open-loop" transfer function. We will show in Sec. 5 how to find the transfer function for a given $R_L$ from the open-loop transfer function for linear two-port networks. For simplicity, we will calculate the "open-loop" transfer function for the "non-linear" diode circuit discussed below. Furthermore, we assume $R_{sig} \to 0$ to arrive at the simplest circuit shown. Impact of loading ($R_L$) and $R_{sig}$ are left as exercise problems.




### 2.9.1 Rectifier Circuits

Since we are interested in the "open-loop" transfer function ($i_o = 0$), current $i_D$ flows through $R$ (by KCL) and




$$\text{KVL} \qquad v_i = v_D + Ri_D$$
$$v_o = Ri_D$$

*Diode OFF:* $i_D = 0$, $v_D < V_{D0}$

$$v_o = Ri_D \qquad \to \qquad v_o = 0$$
$$v_i = v_D + Ri_D \qquad \to \qquad v_i = v_D < V_{D0}$$

Thus, when $v_i < V_{D0}$, diode will be OFF and $v_o = 0$.

*Diode ON:* $v_D = V_{D0}$, $i_D \geq 0$,

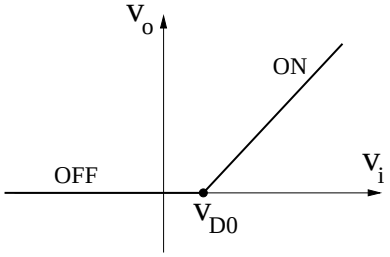
$$v_i = v_D + Ri_D \qquad \rightarrow \qquad v_o = Ri_D = v_i - v_D = v_i - V_{D0}$$
$$i_D = \frac{v_i - V_{D0}}{R} \geq 0 \qquad \rightarrow \qquad v_i \geq V_{D0}$$

Thus, when $v_i \geq V_{D0}$, diode will be ON and $v_o = v_i - V_{D0}$.

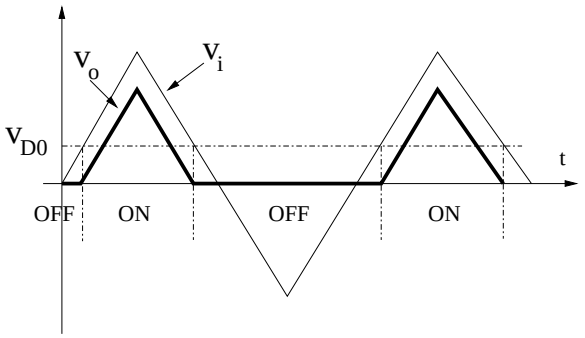
Transfer function of the circuit is:

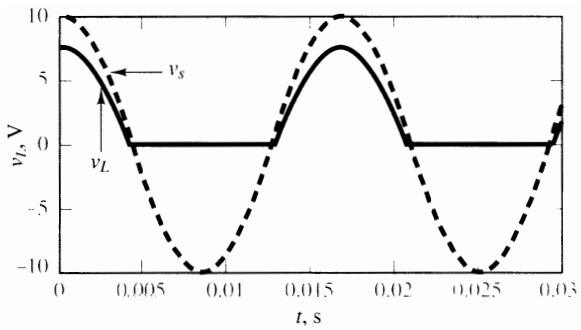
$v_i < V_{D0} \quad \rightarrow \quad$ Diode is OFF: and $v_o = 0$

$v_i \geq V_{D0} \quad \rightarrow \quad$ Diode is ON: and $v_o = v_i - V_{D0}$



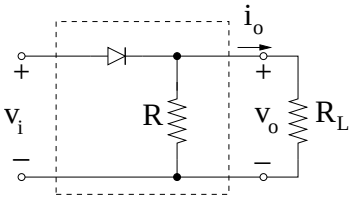

The figure to left below shows how $v_o$ can be found for a time dependent $v_i$ (triangular wave in this case). We find "time intervals" in which $v_i < V_{D0}$ and $v_i \geq V_{D0}$ (vertical dashed lines) and identify the time slices in which diode is ON or OFF (see figure). We can then construct the output wave-form by plotting $v_o = 0$ when diode is OFF and $v_o = v_i - V_{D0}$ when diode is ON as is shown below. Similarly, the response to a sinusoidal input waveform is shown to the right (this is a scope trace with $v_L = v_o$ and $v_s = v_i$).

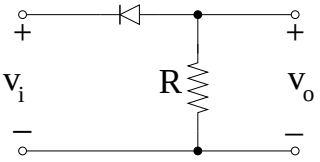



*Exercise:* Explain why the above scope trace for a sinusoidal input wave-form is NOT EXACTLY $v_o = v_i - V_{D0}$ at every point.

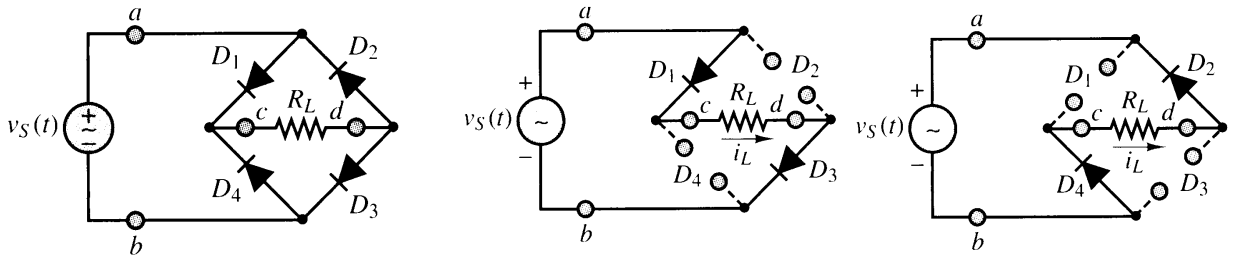
*Exercise:* A) Show that the transfer function does not change if a load $R_L$ is attached to the circuit. B) What happens if the diode terminals are reversed (Answer: circuit work as a rectifier but the output voltage will be negative)

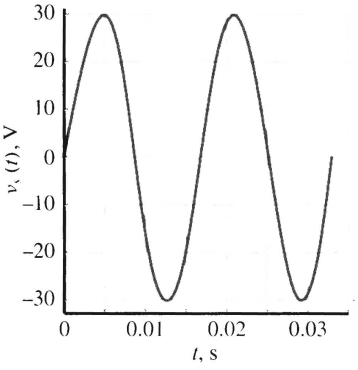


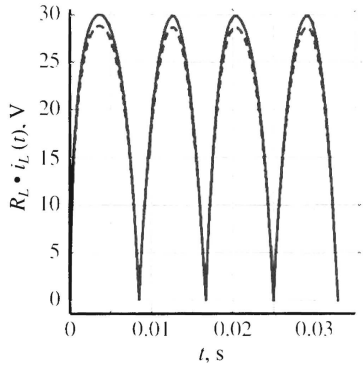



The above circuit is a simple method to convert AC input voltages to a "DC" output voltage and is used in AC to DC converter part of power supplies. Such circuits are called "rectifier" circuits. Because the output of the circuit above is only one half of the input waveform, this circuit is called a "half-wave" rectifier circuit.

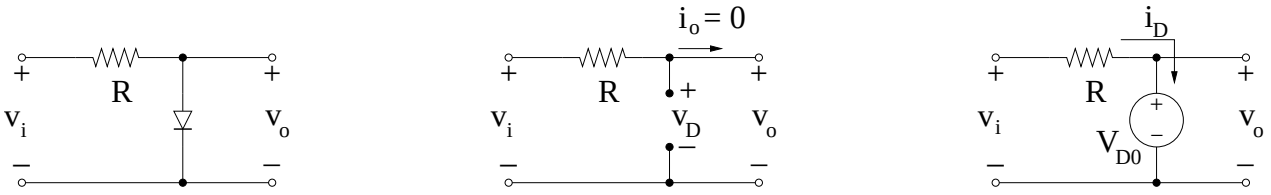
A better circuit would be a "full-wave" rectifier in which both portion of the AC input waveform is turned into a DC output (so that we do not "throw" away half of the input). An example of such a full-wave rectifier is the bridge rectifier shown below with four diodes. We can see that in the portion of the input period in which $v_s > 2V_{D0}$, diodes D1 and D3 are ON and a positive voltage appear across $R_L$. Diodes D2 and D4 are OFF. In the portion of the waveform in which $v_s < -2V_{D0}$, Diode D2 and D4 are ON and diodes D1 and D3 are OFF and again a positive voltage appears on $R_L$. The resulting voltage across $R_L$ is shown below.



### 2.9.2 Clipper Circuit




"Diode OFF, $v_D < V_{D0}$" "Diode ON, $i_D \geq 0$"

KVL $\quad v_i = Ri_D + v_D \quad$ and $\quad v_o = v_D$

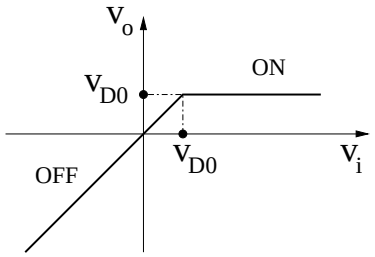
Diode OFF: $\quad v_o = v_i \quad$ and $\quad v_D = v_o = v_i < V_{D0}$

Diode ON: $\quad v_o = V_{D0} \quad$ and $\quad i_D = \dfrac{v_i - V_{D0}}{R} \geq 0 \quad \rightarrow \quad v_i \geq V_{D0}$

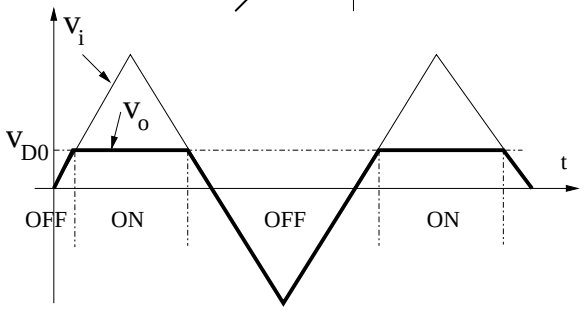
Transfer function of this circuit is shown with

$v_i < V_{D0} \quad \rightarrow \quad$ Diode is OFF: and $v_o = v_i$

$v_i \geq V_{D0} \quad \rightarrow \quad$ Diode is ON: and $v_o = V_{D0}$

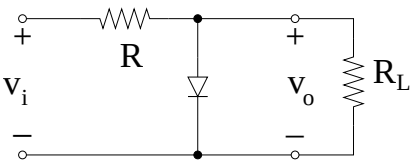



The figure shows $v_o$ for a time dependent $v_i$ (triangular wave in this case). As can be seen, $v_o$ is similar to $v_i$ when $v_i < V_{D0}$. When $v_i \geq V_{D0}$, the output voltage has remained fixed at $V_{D0}$, as if the wave-form is "clipped" for values larger than $V_{D0}$.

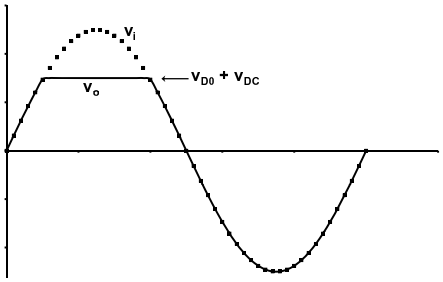


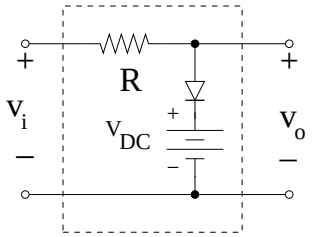

It is of interest to compare the clipper circuit with the half-wave rectifier. As can be seen circuits are the same with the exception of $v_o$ being taken across the resistor for the half-wave rectifier while $v_o$ is taken across the diode for the clipper circuit. Note that since $v_i = v_D + v_R$, this circuit (combination of a diode and a resistor) divides the input signal into two parts, the "rectified" part appears across the resistor and "clipped" part appears across the diode.

*Exercise:* A) Show that the transfer function does not change if a load $R_L$ is attached to the circuit as long as $R_L \gg R$. B) What happens if $R_L$ is not large.



It is of interest to build circuits which can "clip" the input signal at values different than $V_{D0}$. These circuits can be realized by inspecting the clipper circuit. We see that the signal is clipped when the diode is ON and the diode appears as an independent voltage source in the circuit with $v_o = V_{D0}$. As such, we can change the clipping voltage by adding a voltage source in series with the diode as is shown below.



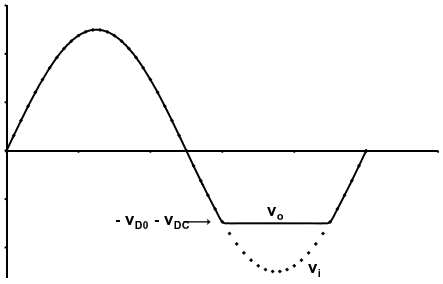

KVL $\quad v_o = v_D + v_{DC} \qquad$ and $\qquad v_i = Ri_D + v_D + v_{DC} = Ri_D + v_o$

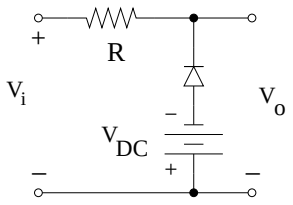
Diode ON: $\quad v_o = V_{D0} + v_{DC} \quad$ and $\quad i_D = \dfrac{v_i - V_{D0} - v_{DC}}{R} \geq 0 \rightarrow v_i \geq V_{D0} + v_{DC}$

Diode OFF: $\quad v_o = v_i - 0 \times R = v_i \quad$ and $\quad v_D = v_i - Ri_D - v_{DC} < V_{D0} \rightarrow v_i < V_{D0} + v_{DC}$

Therefore, this circuit clips input voltages larger than $v_{DC} + V_{D0}$. (The shape of the output signal for a sinusoidal input signal is shown above.) Note that we can choose $v_{DC}$ to be negative and make the clipping voltage to be negative. (However, always the "top" part of the wave form is clipped.)

Similarly, by switching the diode terminals, we can arrive at a circuit that clip the input voltages smaller than $-v_{DC} - V_{D0}$ (the "bottom" part of the wave form is clipped.) Note that $v_{DC}$ terminals are also switched:



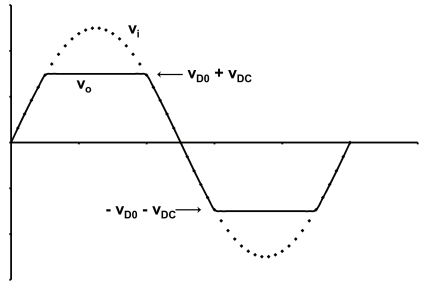



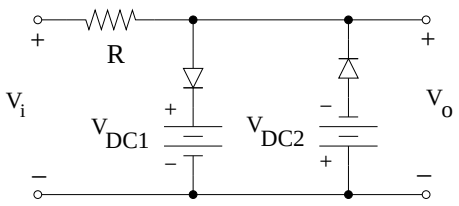

KVL $\quad v_i = -Ri_D - v_D - v_{DC} \qquad$ and $\qquad v_o = -v_D - v_{DC}$

Diode ON: $\quad v_o = -V_{D0} - v_{DC} \quad$ and $\quad i_D = \ fracv_i + V_{D0} + v_{DC}R \geq 0 \rightarrow v_i \leq -V_{D0} - v_{DC}$

Diode OFF: $\quad v_o = \quad$ and $\quad v_D = -v_i - v_{DC} < V_{D0} \rightarrow v_i > -V_{D0} - v_{DC}$

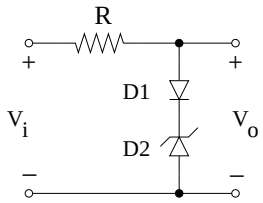
The above two circuits above can be combined to clip both voltages larger than $v_{DC1} + V_{D0}$ and voltages smaller than $-v_{DC2} - V_{D0}$.



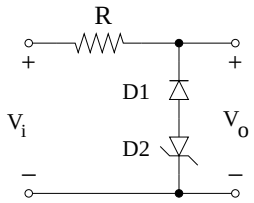




**Exercise:** Prove that the circuit above clips both both voltages larger than $v_{DC1} + V_{D0}$ and voltages smaller than $-v_{DC2} - V_{D0}$. Plot the transfer function of the circuit.

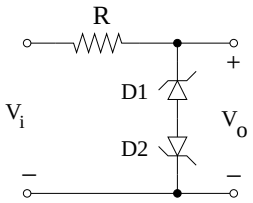
As power supplies are bulky, the above clipper circuits with $v_{DC}$ is only utilized when $v_{DC}$ voltages are available. Otherwise, voltage sources are replaced with Zener diodes as a Zener diode in the Zener region is modeled as a voltage source. The resulting circuits are shown below:




Clips voltages larger than $V_{Z2} + V_{D0}$




Clips voltages Smaller than $-V_{Z,2} - V_{D0,1}$



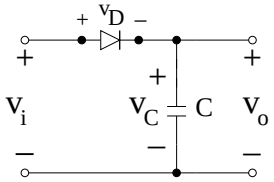

Clips voltages larger than $V_{Z,1} + V_{D0,2}$ and smaller than $-V_{Z,2} - V_{D0,1}$

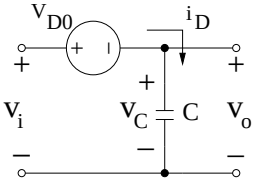
*Exercise:* A) Prove that circuits above clip the input voltage at the values given.

The draw back of the clipper circuit with Zener diodes is that $V_Z$ is always positive as opposed to clipper circuit with voltage sources in which $v_{DC}$ can be both positive or negative. For example for the clipper circuit in which the signal is clipped for voltages above a certain value ($V_{D0} + v_{DC}$ or $V_{D0} + V_Z$), we can clip voltages above a negative voltage by choosing $v_{DC}$ to be negative. The clipper circuit with the Zener diode, however, can only clip voltages larger than a positive value.

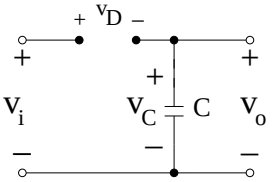
### 2.9.3 Peak Detector

Another simple diode circuit includes a diode and a capacitor. Note that $v_o = v_C$.




Diode is ON
$i_D \geq 0$



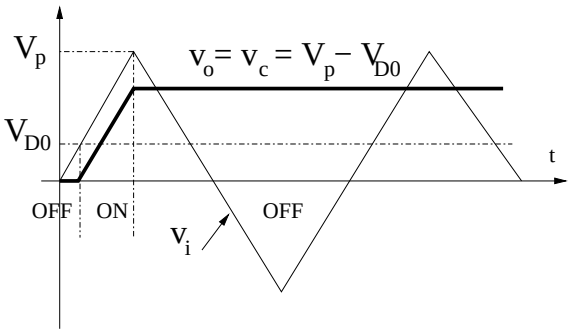

Diode is OFF
$v_D < V_{D0}$

*Case 1: Diode is ON.* In this case $v_o = v_C = v_i - V_{D0}$. Since $i_D = i_C = Cdv_C/dt = Cd(v_i - V_{D0})/dt$, condition of $i_D \geq 0$ requires $v_i$ to be increasing.

*Case 2: Diode is OFF.* In this case $v_o = v_C = constant$. Diode remains off as long as $v_D = v_i - v_C \leq V_{D0}$ or $v_i < v_C + V_{D0}$.

It is important to note that the state of the diode depends not only on $v_i$ but also on $v_C = v_o$.

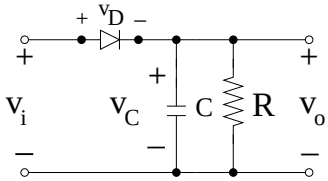
Assume the input signal is a triangular wave with a peak value of $V_p$. At $t = 0$, $v_i = 0$ and $v_C = v_{C,0} = 0$. Since $v_i = 0 < v_C + V_{D0}$, diode is OFF. The diode remains OFF as $v_i$ increases as long as $v_i < V_{D0}$ (see figure). In this interval, $v_o = v_C = 0$ as $v_{C,0} = 0$. When $v_i$ reaches $V_{D0}$, diode turns ON and $v_o = v_C = v_i - V_{D0}$ starts to increase until $v_i$ reaches its peak and starts decreasing.



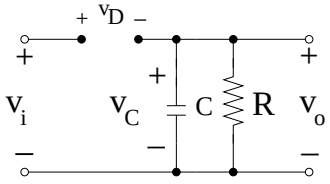

At that point the diode turns OFF as $v_i$ is decreasing. The voltage across the capacitor at this point is $v_o = v_C = V_p - V_{D0}$ and remains at this value. For the following cycles, the diode remains OFF as $v_D$ only reaches $V_{D0}$ at the peak of the cycle.

As can be seen from this discussion that the capacitor charges up to a value of $V_p - V_{D0}$ in the first cycle and its voltage remain constant from then on. Note that $V_p$ is the peak value of the input signal and the shape of the input signal is not important. As the output voltage is the same as the peak of the input voltage (minus $V_{D0}$) this circuit is called a peak detector.

A practical peak-detector circuit includes a load (modeled as a resistor) and we need to include the effect of this resistor on the circuit behavior.



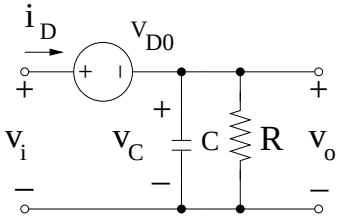
*Case 1: Diode is OFF.* In this case we have an RC circuit with capacitor discharging in the resistor with a time constant $\tau = RC$ according to $v_o(t) = v_C(t) = v_{C,0}\exp[-(t-t_0)/\tau]$ where $v_{C,0}$ denote the voltage across the capacitor when diode is switched to OFF position (at $t_0$). Diode is in OFF state when:




$$v_D = v_i - v_o = v_i - v_C < V_{D0} \quad \rightarrow \quad v_i < v_C + V_{D0}$$

Note that in an ideal peak detector, the voltage across the capacitor does not change. So, to approach the ideal condition, we need to have a "large" $\tau$ (we will show later how large).

*Case 2: Diode is ON.* In this case $v_o = v_C = v_i - V_{D0}$. Exact computation of condition for diode ON ($i_D \geq 0$) is cumbersome and depends on the rate of change of $v_i$ as the current $i_D$ is divided between current in the capacitor $i_c$, and the current in the resistor $i_R$:




$$i_D = i_c + i_R = C\,\frac{d(v_i - V_{D0})}{dT} + \frac{v_i - V_{D0}}{R} = C\left\{\frac{d(v_i - V_{D0})}{dT} + \frac{v_i - V_{D0}}{\tau}\right\}$$

If the change in $v_i - V_{D0}$ occurs much slower than $\tau = RC$ (*i.e.,* if $v_i$ is a sin wave with the period $T$ and $T \gg \tau$), then the first term in the above equation (capacitor current) would be much smaller than the second term (resistor current). As such the capacitor does not play any role (circuit acts as a rectifier) and $i_D \geq 0$ as long as $v_i \geq V_{D0}$.

On the other hand, if the change in $v_i - V_{D0}$ occurs much faster than $\tau$ (*i.e.,* if $v_i$ is a sin wave with the period $T$ and $T \ll \tau$), then the capacitor current dominates (approaching ideal peak detector circuit). In that case, $i_D \geq 0$ if $v_i$ is increasing ($dv_i/dt > 0$) and diode is ON. On other hand if $v_i$ is decreasing, $i_D < 0$ and diode turns OFF.

As can be seen, the circuit behaves differently depending on if $T \gg \tau$ or if $\tau \gg T$ and approaches the ideal peak detector for $\tau = RC \gg T$.

If $T \gg \tau$, we have:

$$\text{Diode ON:} \quad v_i \geq V_{D0} \quad \rightarrow \quad v_o = v_i - V_{D0}$$

$$\text{Diode OFF:} \quad v_i < v_C + V_{D0} \quad \rightarrow \quad v_o = v_C = v_{C,0}\exp[-(t-t_0)/\tau]$$

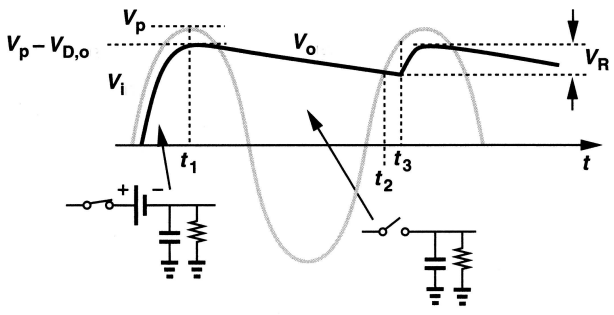
Assume the input signal is a triangular wave. At $t = 0$, $v_i = 0$ and $v_C = v_{C,0} = 0$. Since $v_i = 0 < v_C + V_{D0}$, diode is OFF. The diode remains OFF as $v_i$ increases as long as $v_i < V_{D0}$ (see figure below). In this interval, $v_o = v_C = 0$ as $v_{C,0} = 0$. When $v_i$ reaches $V_{D0}$, diode turns ON and $v_o = v_C = v_i - V_{D0}$. Diode remains ON until $v_i$ reaches its peak value, decreases, and reaches $v_i = V_{D0}$ again. At this point diode turns OFF. In addition, at this point $v_C = v_i - V_{D0} = 0$ which is $v_{C,0}$ for the next interval. As such, during the diode OFF time, $v_o = v_C = 0$ as $v_{C,0} = 0$. The circuit behaves like a half-wave rectifier.

If $\tau \gg T$ (this is the circuit of interest), we have:

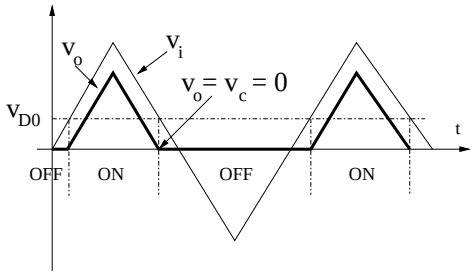
$$\text{Diode ON:} \quad v_i \text{ increasing} \quad \rightarrow \quad v_o = v_i - V_{D0}$$

$$\text{Diode OFF:} \quad v_i < v_C + V_{D0} \quad \text{or} \quad v_i \text{ decreasing} \quad \rightarrow \quad v_o = v_C = v_{C,0}\exp[-(t-t_0)/\tau]$$

We assume that $v_i$ is a sin wave, $v_i = V_p \sin(\omega t)$ and is applied to the circuit at $t = 0$ and at that time $v_C = 0$ ($V_p$ is the peak value of $v_i$). At $t = 0$, $v_i = 0$ and $v_C = v_{C,0} = 0$ and diode is OFF ($v_i < v_C + V_{D0}$). The diode remains OFF as $v_i$ increases as long as $v_i < V_{D0}$. In this interval, $v_o = v_C = 0$ as $v_{C,0} = 0$. When $v_i$ reaches $V_{D0}$, diode turns ON and $v_o = v_C = v_i - V_{D0}$ starts to increase until $v_i$ reaches its peak and starts decreasing. At that point the diode turns OFF ($v_i$ decreasing) and the capacitor starts to discharge and $v_o$ drops slowly. $v_i$ decreases until it reaches its minimum values ($-V_p$) and then it starts to increase. However, as $v_i \leq v_C + V_{D0}$, the diode does NOT turn ON and remains off until $v_i$ reaches $v_i = v_C + V_{D0}$ (and $v_i$ is still increasing). At that point diode turns ON, capacitor starts to charge and its voltage increases according to $v_C = v_o = v_i - V_{D0}$. This continues until $V_i$ reaches its peak $+V_p$ and starts to decrease which turns the diode OFF as is shown below. As can be seen, with the exception of the first quarter of period, the output voltage is roughly constant, $v_o \approx V_p - V_{D0}$, and is $V_{D0}$ below the peak value of the input signal.




($\tau \gg T$)




($T \gg \tau$)

The changes in the output voltage, $V_R$, (see figure) is called the "ripple." To calculate $V_R$, we note that the length of the diode OFF interval (when capacitor is discharging, $t_3 - t_1$ in the figure) is very close to the the period of the input wave. Noting (see figure) $t_0 = t_1$, $v_{C,0} = V_P - V_{D0}$ and $v_C(t = t_3) = V_P - V_{D0} - V_R$:

$$v_o = v_C = v_{C,0}\, e^{-(t - t_0)/\tau}$$

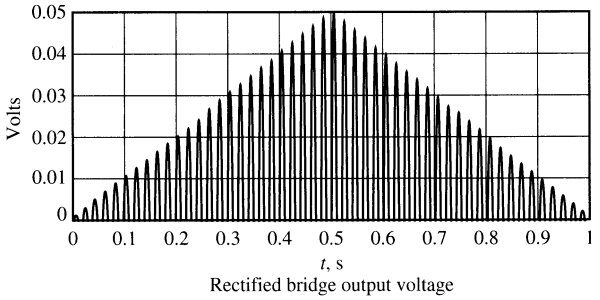
$$v_C(t = t_3) = V_P - V_{D0} - V_R = (V_P - V_{D0})e^{-T/\tau} \approx (V_P - V_{D0})(1 - \frac{T}{\tau})$$

$$\left|\frac{V_R}{V_P - V_{D0}}\right| = \frac{T}{\tau}$$

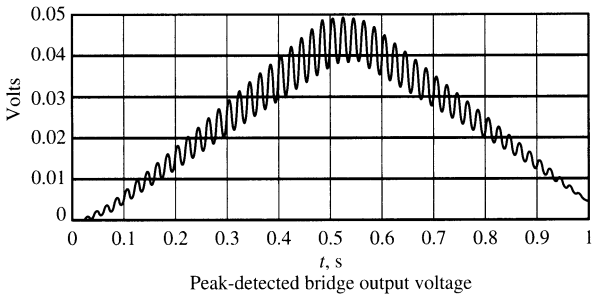
Thus, the "relative" magnitude of the ripple only depends on $T/\tau$. Typically a ripple value of 1%-5% is required.

This circuit has two applications. First, by adding a large capacitor ($RC \gg T$) to our rectifier circuit, we get a relatively smooth DC output. Similarly such a capacitor can be added to a full-wave rectifier circuit.

Second, it can be used as to the "detect" the peak voltage of the input signal. For example, consider the signal transmitted from an AM station. The amplitude of the carrier wave (radio station frequency) is modulated according the sound signal. An example of such a signal is shown below (assuming that the sound signal is a triangular wave). If we apply this modulated voltage to our "peak-detector" circuit above and choose the value of capacitor such that $\tau = RC \gg T_{rf}$ where $T_{rf}$ is the period of radio-frequency carrier wave but $\tau = RC \ll T_{so}$ where $T_{so}$ is the period of the sound wave, the output of the circuit would be an approximation of the the initial sound wave as is shown below. Note that the output voltage is the envelope of the peak amplitudes of the input signal.



Rectified bridge output voltage



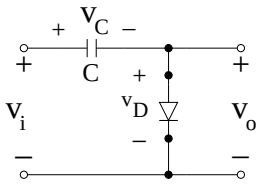
Peak-detected bridge output voltage

*Exercise:* What happens if the input voltage was $v_i = v_{DC} + V_i \sin(\omega t)$? (Answer, the output voltage is roughly constant $v_o \approx V_p - V_{D0}$ with $V_p = v_{DC} + V_i$, *i.e.,* $V_p$ is the maximum value of the input waveform.)

*Exercise:* What happens if the diode terminals are reversed? (See similar exercise for the rectifier circuit.)

### 2.9.4 Clamp Circuit

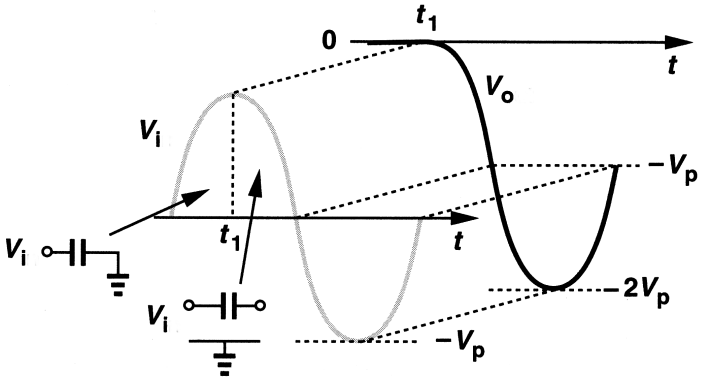
We saw that in the "ideal" peak detector circuit, the capacitor charges to a value of $v_C = V_p - V_{D0}$ in the first cycle and remains at this constant voltage after-wards. In this case,



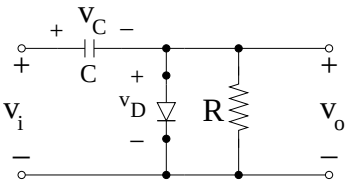

$$v_i = v_C + v_D$$

$$v_i = V_p - V_{D0} + v_D \qquad \rightarrow \qquad v_o = v_D = -(V_p - V_{D0}) + v_i$$

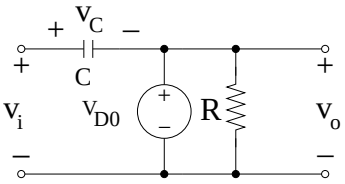
Therefore, the voltage across the diode is equal to the input voltage "shifted" by a DC value of $-(V_p - V_{D0})$. Note that the shape of the input signal is not important (as long $V_p$ is the "peak" value). The input and output signals are shown for the case of $V_{D0} = 0$



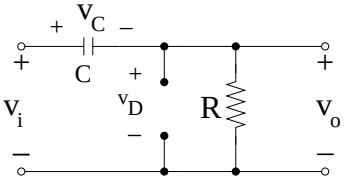

Such a wave-form shaping circuit is called a "clamp" circuit. Typically a resistor $R$ is added across the diode to simulate the impact of the load ($R$ is large enough such that $\tau = RC \gg T$ and, therefore, the voltage across the capacitor drops by $\approx V_R$, similar to a peak detector circuit). Detailed analysis is not performed here as the circuit behaves similar to the peak detector



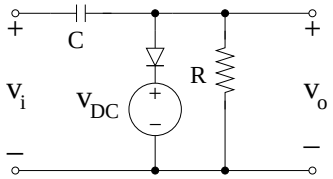

*Case 1: Diode is ON.* We noted that during the first cycle, diode remains ON and charges the capacitor to a voltage $v_C = V_p - V_{D0}$ where $V_p$ is the "peak" value of the input signal.



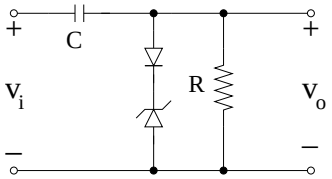

*Case 2: Diode is OFF.* After the first cycle, diode remains OFF almost all of the time (except for brief intervals near the peak of the input voltage to charge up the capacitor again). In this case $v_o = v_i - v_C = v_i - (V_p - V_{D0})$



Since the capacitor is fully charged in the first half cycle when the diode is ON (see diode ON circuit), different values of downward shift (corresponding to different capacitor charged-up voltages) can be produced by the addition of a DC voltage source in series with the diode or using Zener diodes (similar to clipper circuits).

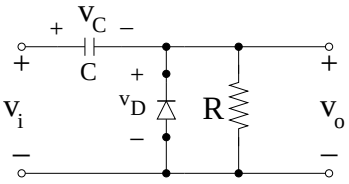



down-shift by
$V_p - V_{D0} - v_{DC}$




down-shift by
$V_p - V_{D0} - V_Z$

If we switch the terminals of the diode (see circuit), it is easy to show that the capacitor will chage to a value of $v_C = -V_p + V_{D0})$ in the first cycle and remains at this constant voltage after-wards. Here $-V_p$ is the lowest voltage of the input signal and $V_p > 0$. Then,

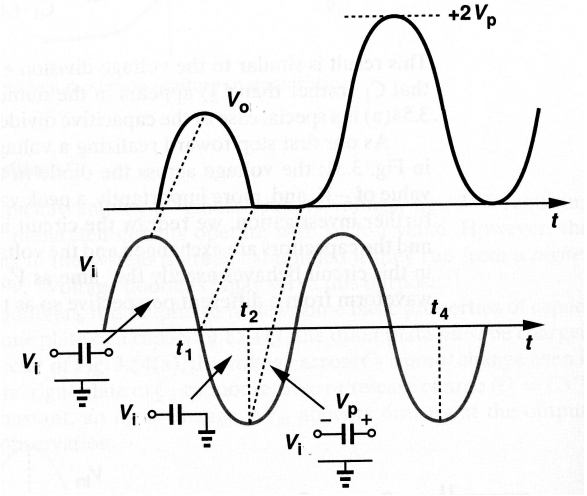



$$v_i = +v_C - v_D$$

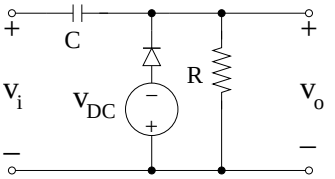
$$v_i = -V_p + V_{D0} - v_D$$

$$v_o = -v_D = v_i + V_p - V_{D0}$$

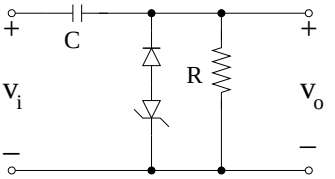
Therefore, the voltage across the diode is equal to the input voltage shifted up by a DC value of $(V_p - V_{D0})$. Note that the shape of the input signal is not important (as long $V_p$ is the "peak" value). The input and output signals are shown for the case of $V_{D0} = 0$




Different values of upward shift (corresponding to different capacitor charged-up voltages) can be produced by the adding a DC voltage source or a Zener diode in series with the diode.




up-shift by
$V_p - V_{D0} - V_{DC}$

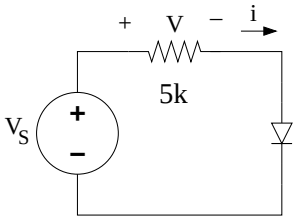



up-shift by
$V_p - V_{D0} - V_Z$

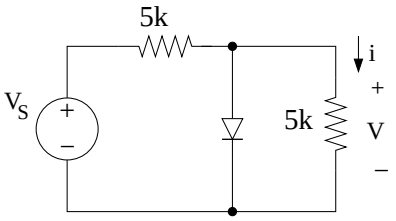
## 2.10 Exercise Problems

In circuit design, use commercial resistor values (1, 1.1, 1.2, 1.3, 1.5, 1.6, 1.8, 2, 2.2, 2.4, 2.7, 3., 3.3, 3.6, 3.9, 4.3, 4.7, 5.1, 5.6, 6.2, 6.8, 7.5, 8.2, 9.1) and commercial capacitor values (1, 1.5, 1.8, 2. or 2.2, 3.3, 4.7, and 6.8) values. You can also use Zener diodes with any Zener voltage.

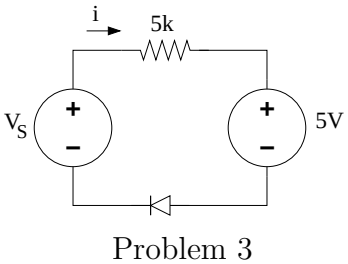
**Problems 1 to 9.** In circuits below with Si diodes ($V_{D0} = 0.7$ V) and $V_Z = 5$ V for Zener diodes, A) Find $v$ and/or $i$ for $v_s = 10$ V, B) Find $v$ and/or $i$ for $v_s$ ranging from $-20$ to $+20$ V.



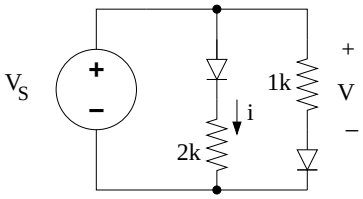

Problem 1



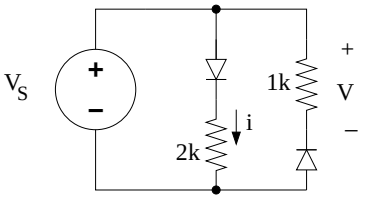

Problem 2



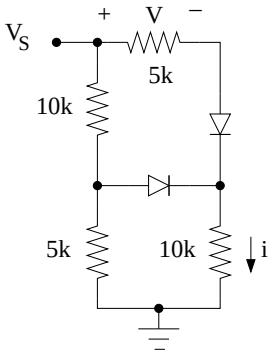

Problem 3



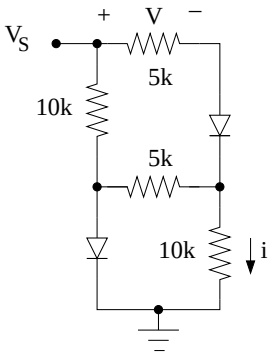

Problem 4



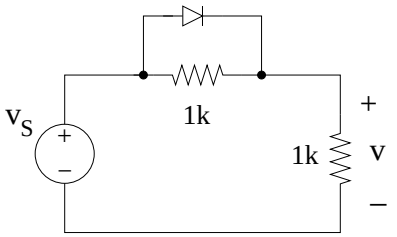

Problem 5



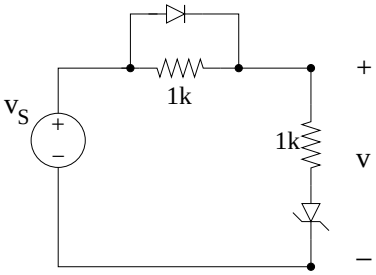

Problem 6




Problem 7

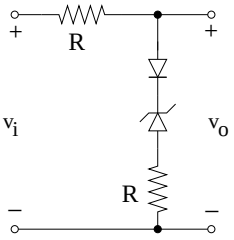



Problem 8

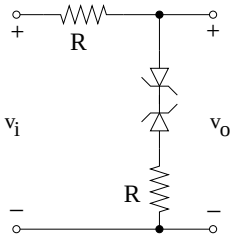



Problem 9

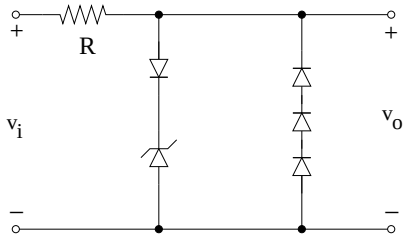
**Problems 10 to 12.** Find transfer functions of circuits below (Si diodes with $V_{D0}$=0.7 V and $V_Z = 5$ V for Zener diodes).




Problem 10




Problem 11




Problem 12

**Problem 13.** Design a clipper circuit that clips voltages above 5 V using a) DC power supplies only, b) Zener diodes only.

**Problem 14.** Design a clipper circuit that clips voltages above 5 V and below −3 V using a) DC power supplies only, b) Zener diodes only.

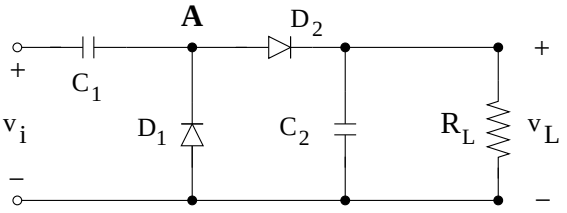
**Problem 15.** Design a clipper circuit that clips voltages above 5 V and below +3 V using a) DC power supplies only, b) Zener diodes only.

**Problem 16.** Consider a sinusoidal source with $v_i = 15\sin(\omega t)$ V. Design a clamp circuit that adds a DC offset of +5 to the input voltage using a) DC power supplies only, b) Zener diodes only.

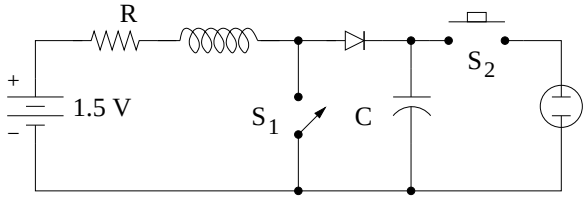
**Problem 17.** Consider a sinusoidal source with $v_i = 15\sin(\omega t)$ V. Design a clamp circuit that adds a DC offset of −5 to the input voltage using a) DC power supplies only, b) Zener diodes only.

**Problem 18.** Circuit below is a "voltage doubler." Show that if $v_i = V_p\sin(\omega t)$, $v_o = 2V_p$ (Assume that capacitor C is large such that it discharge very little per cycle and $V_p \gg V_{D0}$.)

**Problem 19.** Circuit below is a simplified version of an electronic flash for cameras. Switch S2 is controlled by the shutter and is closed to operate the flash bulb. Normally switch S2 is open. The circuit to the left of switch S2 charges the capacitor to about 100 V using a 1.5 V battery. Switch $S1$ is an electronic switch that is opened and closed at about 10 kHz. As a result, the capacitor is charged to about 100 V using a 1.5 V battery. Explain how the charge-up circuit works.



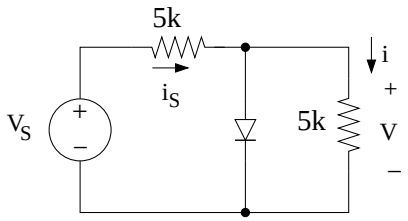

Problem 18




Problem 19

## 2.11 Solution to Selected Exercise Problems

**Problem 2.** In circuit below with Si diodes ($V_{D0} = 0.7$ V) and $V_Z = 5$ V for Zener diodes, A) Find $v$ and/or $i$ for $v_s = 10$ V, B) Find $v$ and/or $i$ for $v_s$ ranging from $-20$ to $+20$ V.




Circuit equations:

KCL: $i_s = i_D + i$

KVL: $v_s = 5 \times 10^3 i_s + v_D$

KVL: $v = v_D = 5 \times 10^3 i$

**Part A:** $v_s = 10$ V.

Assume diode is ON: $v_D = V_{D0} = 0.7$ V, $i_D \geq 0$. Substituting in the above equations we get:

$$v_s = 5 \times 10^3 i_s + v_D \quad \rightarrow \quad 10 = 5 \times 10^3 i_s + 0.7 \quad \rightarrow \quad i_s = 1.86 \text{ mA}$$

$$v = v_D = 0.7 \text{ V}$$

$$v = v_D = 5 \times 10^3 i \quad \rightarrow \quad 0.7 = 5 \times 10^3 i \quad \rightarrow \quad i = 0.14 \text{ mA}$$

$$i_s = i_D + i \quad \rightarrow \quad 1.86 \times 10^{-3} = i_D + 0.14 \times 10^{-3} \quad \rightarrow \quad i_D = 1.72 \text{ mA}$$

Since $i_D = 1.72$ mA $> 0$, our assumption of diode being ON is correct and $i = 0.14$ mA and $v = 0.7$ V.

**Part B:** Parametric Solution:

For diode being ON: $v_D = V_{D0} = 0.7$ V, $i_D \geq 0$. Substituting in the circuit equations we get:

$$v_s = 5 \times 10^3 i_s + v_D \quad \rightarrow \quad v_s = 5 \times 10^3 i_s + 0.7 \quad \rightarrow \quad i_s = 2 \times 10^{-4}(v_s - 0.7) \text{ A}$$

$$v = v_D = 0.7 \text{ V}$$

$$v = v_D = 5 \times 10^3 i \quad \rightarrow \quad 0.7 = 5 \times 10^3 i \quad \rightarrow \quad i = 0.14 \text{ mA}$$

$$i_s = i_D + i \quad \rightarrow \quad i_D = i_s - 0.14 \times 10^{-3} = 2 \times 10^{-4}(v_s - 0.7) - 1.4 \times 10^{-4}$$

$$i_D \geq 0 \quad \rightarrow \quad 2 \times 10^{-4}(v_s - 0.7) - 1.4 \times 10^{-4} \geq 0 \quad \rightarrow \quad v_s \geq 1.4 \text{ V}$$

For diode being OFF: $i_D = 0$ and $v_D < V_{D0} = 0.7$ V. From circuit equations, we get:

$$i_s = i_D + i \quad \rightarrow \quad i_s = i$$

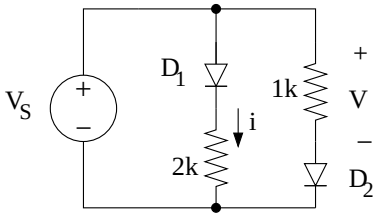
$$v_s = 5\times 10^3 i_s + v_D = 5\times 10^3 i_s + 5\times 10^3 i = 1\times 10^4 i \quad \rightarrow \quad i = 10^{-4} v_s$$

$$v = v_D = 5\times 10^3 i \quad \rightarrow \quad v = v_D = 0.5 v_s$$

$$v_D < V_{D0} = 0.7 \quad \rightarrow \quad 0.5 v_s < 0.7 \quad \rightarrow \quad v_s < 1.4 \text{ V}$$

Therefore, for $v_s < 1.4$ V, diode is OFF $v = 0.5 v_s$ and $i = 10^{-4} v_s$.
For $v_s \geq 1.4$ V, diode is ON, $v = 0.7$ V, and $i = 0.14$ mA.

**Problem 4.** In circuit below with Si diodes ($V_{D0} = 0.7$ V) and $V_Z = 5$ V for Zener diodes, A) Find $v$ and/or $i$ for $v_s = 10$ V, B) Find $v$ and/or $i$ for $v_s$ ranging from $-20$ to $+20$ V.




Circuit equations:

KVL: $v_s = v_{D1} + 2\times 10^3 i_{D1}$

KVL: $v_s = 10^3 i_{D2} + v_{D2}$

$v = 10^3 i_{D2}$ and $i = i_{D1}$

**Part A:** $v_s = 10$ V.

Assume both diodes are ON: $v_{D1} = v_{D2} = V_{D0} = 0.7$ V, $i_{D1} \geq 0$, and $i_{D2} \geq 0$. Substituting in the above equations we get:

KVL: $v_s = v_{D1} + 2\times 10^3 i_{D1} \rightarrow 10 = 0.7 + 2\times 10^3 i_{D1} \rightarrow i_{D1} = 4.65\times 10^{-3} = 4.65$ mA

KVL: $v_s = 10^3 i_{D2} + v_{D2} \quad \rightarrow \quad 10 = 0.7 + 10^3 i_{D2} \quad \rightarrow \quad i_{D2} = 9.3\times 10^{-3} = 9.3$ mA

$v = 10^3 i_{D2} \quad \rightarrow \quad v = 9.3$ V

Since both $i_{D1}$ and $i_{D1}$ are positive, our assumption of both diodes being ON is correct and $v = 9.3$ V and $i = i_{D1} = 4.65$ mA.

**Part B:** Parametric Solution: Here, we have to consider four cases.

*Case 1:* D1 and D2 are both ON: $v_{D1} = v_{D2} = V_{D0} = 0.7$ V, $i_{D1} \geq 0$, and $i_{D2} \geq 0$.

KVL: $v_s = v_{D1} + 2\times 10^3 i_{D1} \rightarrow v_s = 0.7 + 2\times 10^3 i_{D1} \rightarrow i_{D1} = 5\times 10^{-4}(v_s - 0.7)$

KVL: $v_s = 10^3 i_{D2} + v_{D2} \quad \rightarrow \quad v_s = 0.7 + 10^3 i_{D2} \quad \rightarrow \quad i_{D2} = 10^{-3}(v_s - 0.7)$

$v = 10^3 i_{D2} \quad \rightarrow \quad v = v_s - 0.7$

$i_{D1} \geq 0 \quad \rightarrow \quad 5\times 10^{-4}(v_s - 0.7) \geq 0 \quad \rightarrow \quad v_s \geq 0.7$ V

$i_{D2} \geq 0 \quad \rightarrow \quad 10^{-3}(v_s - 0.7) \geq 0 \quad \rightarrow \quad v_s \geq 0.7$ V

So, for $v_s > 0.7$ V, both diodes will be ON with $v = v_s - 0.7$ V and $i = i_{D1} = 5 \times 10^{-4}(v_s - 0.7) = 0.5(v_s - 0.7)$ mA.

*Case 2:* D1 and D2 are both OFF: $i_{D1} = i_{D2} = 0$, $v_{D1} < V_{D0} = 0.7$ V, and $v_{D2} < V_{D0} = 0.7$ V.

KVL: $v_s = v_{D1} + 2 \times 10^3 i_{D1} \quad \rightarrow \quad v_{D1} = v_s$

KVL: $v_s = 10^3 i_{D2} + v_{D2} \quad \rightarrow \quad v_{D2} = v_s$

$v = 10^3 i_{D2} \quad \rightarrow \quad v = 0$

$v_{D1} < V_{D0} = 0.7 \quad \rightarrow \quad v_s < 0.7$ V

$v_{D2} < V_{D0} = 0.7 \quad \rightarrow \quad v_s < 0.7$ V

So, for $v_s < 0.7$ V, both diodes will be OFF with $v = 0$ and $i = i_{D1} = 0$

Note that since for $v_s > 0.7$ V, both diodes will be ON and for $v_s < 0.7$ V, both diodes will be OFF, one would expect that it would not be possible for one diode to be ON and one to be OFF. We will demonstrate this below.

*Case 3:* D1 is ON: $v_{D1} = V_{D0} = 0.7$ V, and $i_{D1} \geq 0$ while D2 is OFF: $i_{D2} = 0$ and $v_{D2} < V_{D0} = 0.7$ V.

KVL: $v_s = v_{D1} + 2 \times 10^3 i_{D1} \rightarrow v_s = 0.7 + 2 \times 10^3 i_{D1} \rightarrow i_{D1} = 5 \times 10^{-4}(v_s - 0.7)$

KVL: $v_s = 10^3 i_{D2} + v_{D2} \quad \rightarrow \quad v_{D2} = v_s$

$v = 10^3 i_{D2} \quad \rightarrow \quad v = v_s - 0.7$

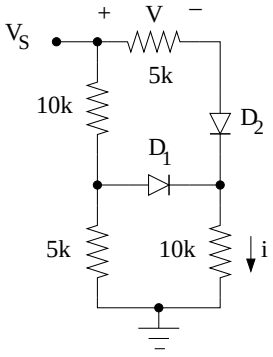
$i_{D1} \geq 0 \quad \rightarrow \quad 5 \times 10^{-4}(v_s - 0.7) \geq 0 \quad \rightarrow \quad v_s \geq 0.7$ V

$v_{D2} < V_{D0} = 0.7 \quad \rightarrow \quad v_s < 0.7$ V

We see that for D1 to be ON ($i_{D1} \geq 0$), we need $v_s \geq 0.7$ V and for D2 to be OFF ($v_{D2} < V_{D0}$) we need $v_s < 0.7$ V. These cases are mutually exclusive so we cannot have simultaneously D1 ON and D2 OFF.

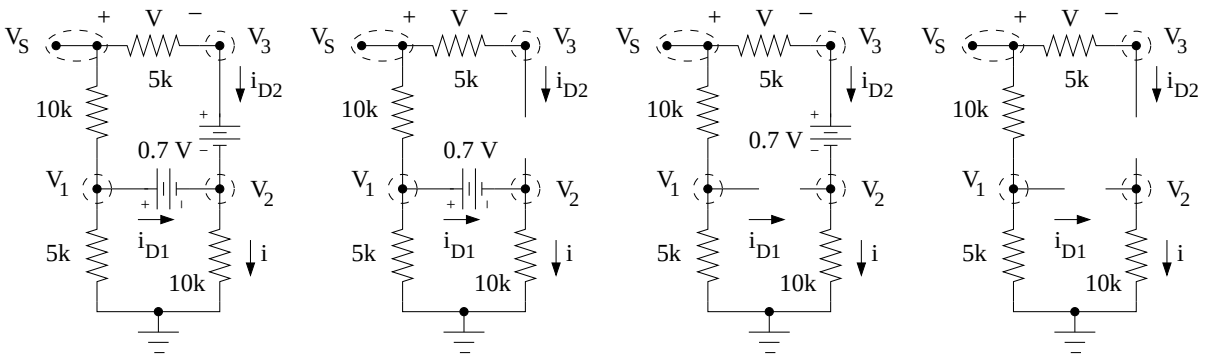
Similarly, we can find D1 is OFF and D2 ON case is not possible.

**Problem 6.** In circuit below with Si diodes ($V_{D0} = 0.7$ V) and $V_Z = 5$ V for Zener diodes, A) Find $v$ and/or $i$ for $v_s = 10$ V, B) Find $v$ and/or $i$ for $v_s$ ranging from $-20$ to $+20$ V.




**Part A:** $v_s = 10$ V.

With the exception of simple circuits, it is usually more useful to redraw the circuit based on the state of the diodes as this can simplify the circuit considerably. Note that when a diode is ON, $v_D = V_{D0}$ for $i_D > 0$ and the diode resembles an ideal voltage source with the strength of $V_{D0}$. When the diode is OFF, $i_D = 0$ and the diode resembles an open circuit. This can be seen in circuits below:




D1 ON, D2 ON | D1 ON, D2 OFF | D1 OFF, D2 ON | D1 OFF, D2 OFF

Case 1: Assume D1 is ON and D2 is ON. The above circuit can be solved by node voltage method. This circuit has four nodes, $v_1$, $v_2$, $v_3$, and $v_s = 10$ V. All nodes are supernodes as they are attached to a voltage source. So we have only we KCL containing nodes $v_1$, $v_2$, and $v_3$:

$$\text{Supernode:} \quad v_1 - v_2 = 0.7$$

$$\text{Supernode:} \quad v_3 - v_2 = 0.7$$

$$\text{KCL at } v_1, v_2, v_3: \quad \frac{v_1 - v_s}{10 \times 10^3} + \frac{v_3 - v_s}{5 \times 10^3} + \frac{v_1 - 0}{5 \times 10^3} + \frac{v_2 - 0}{10 \times 10^3} = 0$$

$$v_1 - v_s + 2(v_3 - v_s) + 2v_1 + v_2 = 0$$

$$3v_1 + v_2 + 2v_3 = 3v_s = 30 \text{ V}$$

We substitute for $v_1$ and $v_3$ from the first two equations in the last equation to get:

$$3(v_2 + 0.7) + v_2 + 2(v_2 + 0.7) = 30 \quad \rightarrow \quad v_2 = 4.42 \text{ V} \quad \text{and} \quad v_1 = v_3 = 5.12 \text{ V}$$

To check the validity of our assumption of D1 and D2 ON, we need to compute $i_{D1}$ and $i_{D2}$. $i_{D2}$ is the same as the current in the 5 k resistor on the top of the circuit and $i_{D2}$ can be found by KCL at node $v_1$:

$$i_{D1} = \frac{v_s - v_1}{10 \times 10^3} + \frac{0 - v_1}{5 \times 10^3} = \frac{10 - 5.12}{10 \times 10^3} + \frac{-5.12}{5 \times 10^3} = -0.54 \text{ mA} < 0$$
$$i_{D2} = \frac{v_s - v_3}{5 \times 10^3} = \frac{10 - 5.12}{5 \times 10^3} = 0.98 \text{ mA} > 0$$

Since $i_{D1} < 0$, our assumption is incorrect and we should consider other cases.

Case 2: Assume D1 is ON and D2 is OFF. The above circuit can be solved by node voltage method. This circuit has three nodes, $v_1$, $v_2$, and $v_s = 10$ V ($v_3 = v_s = 10$ V as $i_{D2} = 0$). All nodes are supernodes as they are attached to a voltage source. So:

$$\text{Supernode:} \quad v_1 - v_2 = 0.7$$
$$\text{KCL at } v_1, v_2: \quad \frac{v_1 - v_s}{10 \times 10^3} + \frac{v_1 - 0}{5 \times 10^3} + \frac{v_2 - 0}{10 \times 10^3} = 0$$
$$v_1 - v_s + 2v_1 + v_2 = 0 \quad \rightarrow \quad 3v_1 + v_2 = v_s = 10 \text{ V}$$

We substitute for $v_1$ from the first equation in the second equation to get:

$$3(v_2 + 0.7) + v_2 = 10 \quad \rightarrow \quad v_2 = 1.98 \text{ V} \quad \text{and} \quad v_1 = 2.68 \text{ V}$$

To check the validity of our assumption of D1 ON and D2 OFF, we need to compute $i_{D1}$ (KCL at node $v_1$) and $v_{D2}$.

$$i_{D1} = \frac{v_s - v_1}{10 \times 10^3} + \frac{0 - v_1}{5 \times 10^3} = \frac{10 - 1.98}{10 \times 10^3} - \frac{1.98}{5 \times 10^3} = 4.06 \text{ mA} > 0$$
$$v_{D2} = v_3 - v_2 = 10 - 1.98 = 8.02 > 0.7 \text{ V}$$

Since $v_{D2} > 0.7$, our assumption is incorrect and we should consider other cases.

Case 3: Assume D1 is OFF and D2 is ON. The above circuit can be solved by node voltage method. This circuit has four nodes, $v_1$, $v_2$, $v_3$, and $v_s = 10$ V. All nodes except $v_1$ are supernodes as they are attached to a voltage source. So:

$$\text{Supernode:} \quad v_3 - v_2 = 0.7$$
$$\text{KCL at } v_2, v_3: \quad \frac{v_3 - v_s}{5 \times 10^3} + \frac{v_2 - 0}{10 \times 10^3} = 0 \quad \rightarrow \quad 2v_3 - 20 + v_2 = 0$$
$$\text{KCL at } v_1: \quad \frac{v_1 - v_s}{10 \times 10^3} + \frac{v_1 - 0}{5 \times 10^3} = 0 \quad \rightarrow \quad v_1 - 10 + 2v_1 = 0 \quad \rightarrow \quad v_1 = 3.33 \text{ V}$$

The first two equations can be solved to find $v_2$ and $v_3$:

$$2(v_2 + 0.7) + v_2 = 20 \quad \rightarrow \quad v_2 = 6.2 \text{ V} \quad \rightarrow \quad v_3 = 6.9 \text{ V}$$

To check the validity of our assumption of D1 OFF and D2 ON, we need to compute $v_{D1}$ and $i_{D2}$.

$$v_{D1} = v_1 - v_2 = 3.33 - 6.2 = -2.87 < 0.7 \text{ V}$$
$$i_{D2} = \frac{v_s - v_3}{5 \times 10^3} = \frac{10 - 6.9}{5 \times 10^3} = 0.62 \text{ mA} > 0$$

Since $v_{D1} < 0.7$ and $i_{D2} > 0$, our assumption is correct. So D1 is OFF, D2 is ON and $i = i_{D2} = 0.62$mA and $v = v_s - v_3 = 10 - 6.9 = 3.1$ V.

This case could have been solved more simply by noting that when D1 is OFF, the two branches of the circuit become independent (we have two separate circuits) and $v_1$ and $v_2$ can be directly calculated:

$$v_1 = \frac{5 \times 10^3}{10 \times 10^3 + 5 \times 10^3} \times 10 = 3.33 \text{ V}$$
$$i = i_{D2} = \frac{v_s - 0.7}{10 \times 10^3 + 5 \times 10^3} = 0.62 \text{ mA}$$

and proceed to compute $v_{D1} < 0.7$ to show that our assumption was valid.

Case 4: Assume D1 is OFF and D2 is OFF.

While we proved that D1 is OFF and D2 is ON, let's proceed to solve this case. Again, we see that two branches of the circuit are independent. In addition, since $i = 0$, $v_2 = 0$ and $v_3 = v_s = 10$ V. From voltage divider, we have $v_1 = 3.33$ V (similar to case 3).

To check our assumption, we note $v_{D1} = v_1 - v_2 = 3.33 - 0 = 3.33 > 0.7$ V so D1 cannot be OFF and assumption was incorrect.

As can be seen, the simplest circuit is when diodes are OFF as the circuit usually divides into several simpler circuits. As such, if one cannot make an educated guess regarding the state of the diodes, it is usually best to start the analysis with diodes being OFF.

**Part B:** Parametric Solution: Here, we have to consider four cases. As discussed above, we will start with simplest cases (diodes OFF).

*Case 1:* D1 and D2 are both OFF: we see that two branches of the circuit are independent. In addition, since $i = 0$, $v_2 = 0$ and $v_3 = v_s$. From voltage divider, we have $v_1 = v_s/3$.

To find the range of validity of this solution,

$$v_{D1} = v_s/3 < V_{D0} \quad \rightarrow \quad v_s < 2.1 \text{ V}$$
$$v_{D2} = v_3 - v_2 < V_{D0} \quad \rightarrow \quad v_s < 0.7 \text{ V}$$

For both diodes to be OFF, we need $v_s < 0.7$ V (the most restrictive of both conditions).

So, for $v_s < 0.7$ V, both diodes will be OFF, $i = 0$ and $v = 0$

*Case 2:* D1 OFF and D2 ON: we see that two branches of the circuit are independent. From voltage divider, we have $v_1 = v_s/3$ V.

$$i = i_{D2} = \frac{v_s - 0.7}{10 \times 10^3 + 5 \times 10^3} = 6.67 \times 10^{-5}(v_s - 0.7)$$
$$v = 5 \times 10^3 i = 0.33(v_s - 0.7)$$

To find the range of validity of this solution,

$$i_{D2} = 6.67 \times 10^{-5}(v_s - 0.7) \geq 0 \quad \rightarrow \quad v_s \geq 0.7 \text{ V}$$
$$v_{D1} = v_1 - v_2 < V_{D0} \quad \rightarrow \quad \frac{v_s}{3} - 10 \times 10^3 i < 0.7$$
$$0.33 v_s - 0.67(v_s - 0.7) < 0.7 \quad \rightarrow \quad v_s > -0.7 \text{ V}$$

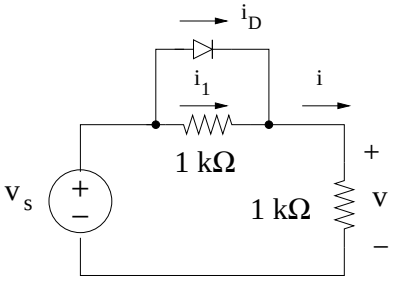
For D1 OFF and D2 ON, we need $v_s \geq 0.7$ V (the most restrictive of both conditions).

So, for $v_s \geq 0.7$ V, D1 OFF and D2 ON, $i = 6.67 \times 10^{-5}(v_s - 0.7)$ and $v = 0.33(v_s - 0.7)$.

Since for $v_s < 0.7$ V, both diodes will be OFF and for $v_s > 0.7$ V, D1 is OFF and D2 is ON, there is no range of values for $v_s$ when other cases (D1 ON and D2 OFF or both ON) are possible.

*Exercise:* Solve circuit equations directly to show that D1 ON and D2 OFF Case or both diodes ON Cases are not physically possible.

**Problem 8.** In circuit below with Si diodes ($V_{D0} = 0.7$ V) and $V_Z = 5$ V for Zener diodes, A) Find $v$ and/or $i$ for $v_s = 10$ V, B) Find $v$ and/or $i$ for $v_s$ ranging from $-20$ to $+20$ V.




**Part A:** $v_s = 10$ V.

Assume diode is OFF: $i_D = 0$ and $v_D < V_{D0} = 0.7$ V. Then $i_1 = i = v_s/(10^3+10^3) = 5$ mA and $v = 10^3 i = 5$ V.

To check the our assumption, we note $v_D = 10^3 i_1 = 5 > 0.7$ V, so the assumption is incorrect.

Assume diode is ON: $v_D = V_{D0} = 0.7$ V and $i_D \geq 0$ Then by KVL: $v = v_s - v_D = 9.3$ V and $i = v/10^3 = 9.3$ mA.

To check the our assumption, we note $i_1 = v_D/10^3 = 0.7$ mA and by KCL $i_D = i - i_1 = 8.6$ mA. Since $i_D > 0$, our assumption is correct.

Therefore, diode is ON and $i = 9.3$ mA and $v = 9.3$ V.

**Part B:** Parametric Solution:

*Case 1:* Assume diode is ON: $v_D = V_{D0} = 0.7$ V and $i_D \geq 0$.

KVL: $\quad v = v_s - v_D = v_s - 0.7$

To check the region of validity of our assumption we need to calculate $i_D$:

$$i_1 = \frac{v_D}{10^3} = 0.7 \times 10^{-3} \text{ A} = 0.7 \text{ mA} \quad \text{and} \quad i = \frac{v}{10^3} = 10^{-3} \times (v_i - 0.7)$$

$$i_D = i - i_1 \geq 0 \quad \rightarrow \quad 10^{-3} \times (v_s - 0.7) - 0.7 \times 10^{-3} \geq 0 \quad \rightarrow \quad v_s \geq 1.4 \text{ V}$$

So, if $v_s \geq 1.4$ V, the diode will be ON and $v = v_s - 0.7$ V.

*Case 2:* Assume diode is OFF: $i_D = 0$ and $v_D < V_{D0} = 0.7$ V.

KCL: $\quad i = i_1 + i_D = i_1$

KVL: $\quad v_s = 10^3 i_1 + 10^3 i = 2 \times 10^3 i \quad \rightarrow \quad i = i_1 = 0.5 \times 10^{-3} v_s$

$\qquad v = 10^3 i = 0.5 v_s$

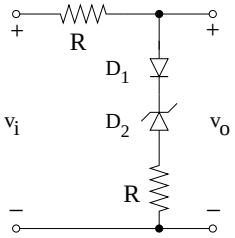
To check the region of validity of our assumption we need to calculate $v_D$:

$$v_D = v_s - v = v_s - 0.5 v_s = 0.5 v_s$$

$$v_D < V_{D0} \quad \rightarrow \quad 0.5 v_s < 0.7 \quad \rightarrow \quad v_s < 1.4 \text{ V}$$

So, if $v_s < 1.4$ V, the diode will be OFF and $v = 0.5 v_s$.

**Problem 10.** Find transfer function of the circuit below (Si diodes with $V_{D0}$=0.7 V and $V_Z = 5$ V for Zener diodes).




The regular diode can have two states (ON and OFF) and the Zener diode has three states (ON, OFF, and Zener). So, it appears that we need to consider $2 \times 3 = 6$ possible cases. However, an examination of the circuit shows that only two of these six combinations are possible by nothing $i_{D1} = -i_{D2}$.

If D1 is ON, $i_{D1} \geq 0$. This means that $i_{D2} < 0$ and D2 diode has to be in Zener state.

If D2 is OFF, $i_{D1} = 0$. This means that $i_{D2} = 0$ and D2 diode has to be OFF.

*Case 1:* D1 is ON ($v_{D1} = V_{D0} = 0.7$ V, $i_{D1} \geq 0$) and D2 is in Zener state ($v_{D2} = -V_Z = -5$ V and $i_{D2} \leq 0$). By KVL:

$$v_i = Ri_{D1} + v_{D1} - v_{D2} + Ri_{D1} \quad \rightarrow \quad i_{D1} = \frac{v_i - v_{D1} + v_{D2}}{2R}$$

$$v_o = v_i - Ri_{D1} = v_i - 0.5(v_i - v_{D1} + v_{D2}) = 0.5(v_i + v_{D1} - v_{D2}) = 0.5(v_i + 5.7)$$

The range of validity of this solution can be found by setting $i_{D1} \geq 0$ ($i_{D2} \leq 0$ will be automatically satisfied).

$$i_{D1} = \frac{v_i - v_{D1} + v_{D2}}{2R} \geq 0 \quad \rightarrow \quad v_i \geq v_{D1} - v_{D2} = 0.7 + 5.0 = 5.7 \text{ V}$$

*Case 2:* D1 and D2 are OFF ($i_{D1} = i_{D2} = 0$, $v_{D1} < V_{D0} = 0.7$ V, $-V_Z < v_{D2} < V_{D0} = 0.7$ V).

In this case, $v_o = v_i - Ri_{D1} = v_i$.

The range of validity of this solution can be found by noting:

$$v_{D1} - v_{D2} = v_o = v_i$$

$$v_{D1} < V_{D0} \quad \text{and} \quad -V_{D0} < -v_{D2} < V_Z$$

$$v_{D1} - v_{D2} < V_{D0} + V_Z \quad \rightarrow \quad v_i < V_{D0} + V_Z = 5.7 \text{ V}$$

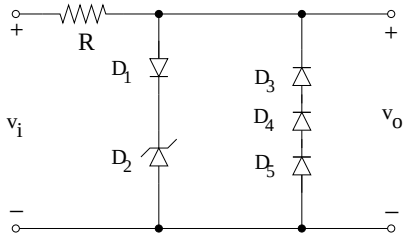
Transfer function:

$$v_i < 5.7 \text{ V} \quad \rightarrow \quad v_o = v_i$$

$$v_i \geq 5.7 \text{ V} \quad \rightarrow \quad v_o = 0.5(v_i + 5.7) \text{ V}$$

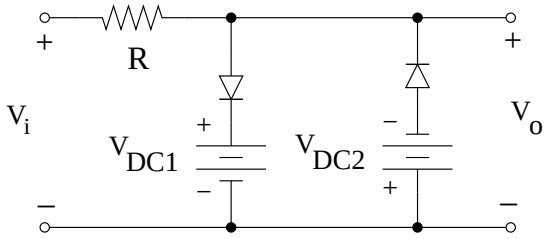
**Problem 12.** Find $v_o$ for $v_s = V_s \sin(\omega t)$.

Diodes D3, D4, and D5 all have the same state (all are ON or all OFF). So, they act like ONE diode with a cut-in voltage of $3V_{D0} = 2.1$ V. Therefore, examination of the circuit shows that this is a clipper circuit. It clips the input voltage above $V_{D0} + V_Z = 5.7$ V and clips the voltage below $-3V_{D0} = -2.1$ V

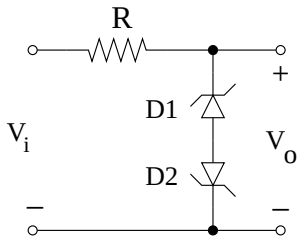



**Problem 14.** Design a clipper circuit that clips voltages above 5 V and below $-3$ V using a) DC power supplies only, b) Zener diodes only.

**Part A:** Set $v_{DC1} + V_{D0,1} = 5$ or $v_{DC1} = 4.3$ V
Set $-v_{DC2} - V_{D0,2} = -3$ or $v_{DC2} = 2.3$ V




**Part B:** Set $V_{Z,1} + V_{D0,2} = 5$ or $V_{Z,1} = 4.3$ V
Set $-V_{Z,2} - V_{D0,1} = -3$ or $V_{Z,2} = 2.3$ V

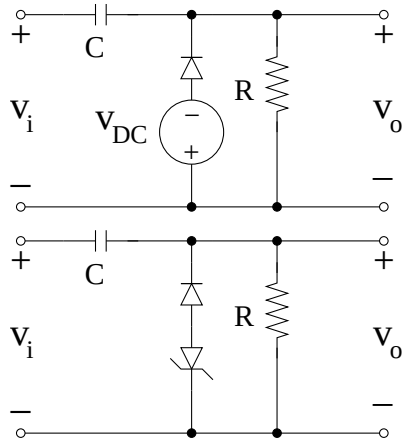



**Problem 16.** Consider a sinusoidal source with $v_i = 15 \sin(\omega t)$ V. Design a clamp circuit that adds a DC offset of +5 to the input voltage using a) DC power supplies only, b) Zener diodes only.

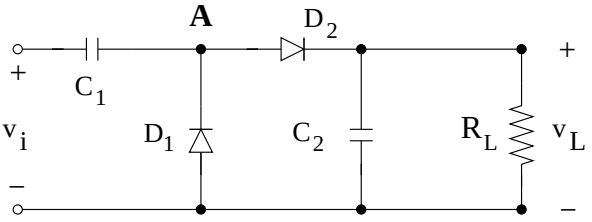
**Part A:** Set $V_p - V_{DC} = 5$ or $V_{DC} = 15 - 5 = 10$ V.

**Part B:** Set $V_p - V_Z = 5$ or $V_Z = 15 - 5 = 10$ V

Capacitor values should be chosen such that $RC = \tau \gg T = 1/f = 2\pi/\omega$.

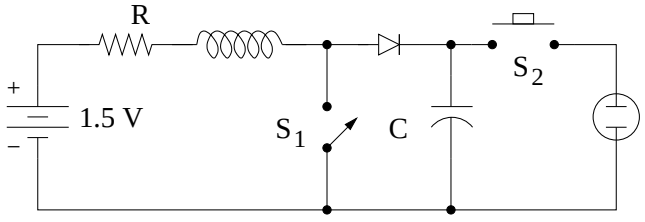


**Problem 18.** Circuit below is a "voltage doubler." Show that if $v_i = V_p \sin(\omega t)$, $v_o = 2V_p$ (Assume that capacitor C is large such that it discharge very little per cycle and $V_p \gg V_{D0}$.)




Capacitor C1 and diode D1 form a clamp circuit. As a result the voltage at point A is a sinusoidal voltage with a DC offset of $V_p$ (ignoring $V_{D0}$). Diode D2 and capacitor C2 form a peak-detector circuit. They will generate a DC signal with a value which is equal to the peak of AC signal or $2V_p$

**Problem 19.** Circuit below is a simplified version of an electronic flash for cameras. Switch S2 is controlled by the shutter and is closed to operate the flash bulb. Normally switch S2 is open. The circuit to the left of switch S2 charges the capacitor to about 100 V using a 1.5 V battery. Switch $S1$ is an electronic switch that is opened and closed at about 10 kHz. As a result, the capacitor is charged to about 100 V using a 1.5 V battery. Explain how the charge-up circuit works.




When the electronic switch is closed, the battery increases the inductor current, *i.e.,* inductor charges up as its magnetic stored energy increases. When the electronic switch opens, the inductor current cannot change suddenly. The inductor current has to flow through the diode and the capacitor which charges up the capacitor and increases its voltage (Note $i_L = i_C = Cdv_C/dt > 0$ leads to an increase in $v_C$). So each time, the electronic switch closes and opens, the capacitor voltage is increased. When the capacitor reaches its desired voltage, the electronic switch stays at open position. Diode D1 prevents the capacitor to discharge back into the power supply and resistor R.

Note that The inductor can charge the capacitor voltage to a high value without violating KVL as during the capacitor charge up cycle, a negative voltage appears across the inductor $v_L = Ldi/dt$ which means that capacitor voltage would become much larger than the battery voltage.