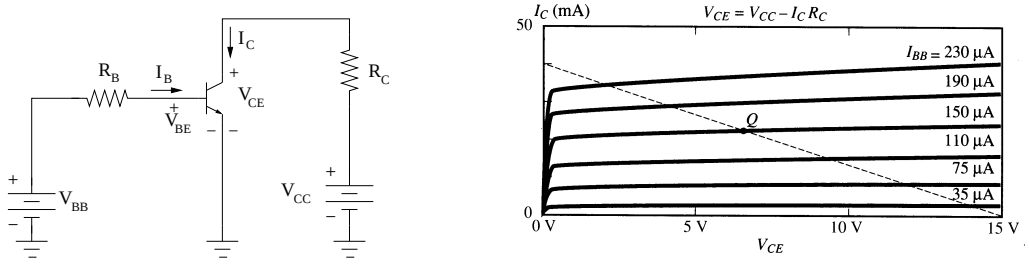
IV. Transistors (Biasing & Small-Signal Model)

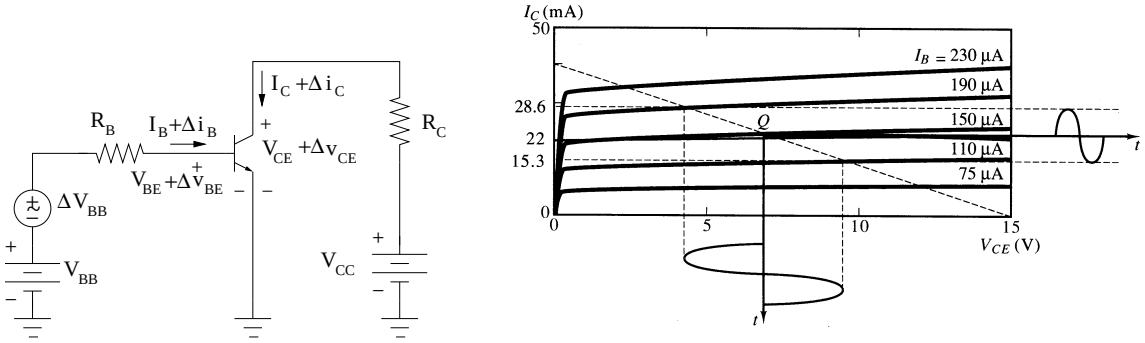
4.1 Introduction

Amplifiers are the main component of any analog circuit. Not only they can amplify the signal, they can be configured into may other useful circuits with a proper "feedback" (you will see this in 100 for OpAmps). In this course, we focus on simple transistor amplifiers. Transistor amplifiers utilizing BJT or MOSFET are similar in design and analysis. As such, we discuss them together. However, first we need to review some concepts which are essential in the design and analysis of the amplifier circuits.

Consider the circuit below with a NPN BJT. The operating point of the BJT is shown in the $i_C v_{CE}$ space.



Let us add a sinusoidal source with an amplitude of ΔV_{BB} in series with V_{BB}. In response to this additional source, the base current will become $I_B + \Delta i_B$ leading to a collector current of $I_C + \Delta i_C$ and a CE voltage of $V_{CE} + \Delta v_{CE}$.



Assume that without the sinusoidal source the base current is 150 μA, $I_C = 22$ mA, and $V_{CE} = 7$ V (the Q point). If the amplitude of Δi_B is 40 μA, then with the addition of the sinusoidal source $I_B + \Delta i_B = 150 + 40\cos(\omega t)$ μA and i_B varies from 110 to 190 μA.

As the BJT operating point should remain on the load line, the collector current and CE voltage change with changing base current while remaining on the load line. For example when base current is 190 μA, the collector current is 28.6 mA and CE voltage is about

4.5 V. As can be seen from the figure above, the collector current will approximately be $I_C + \Delta i_C = 22 + 6.6\cos(\omega t)$ mA and CE voltage is $V_{CE} + \Delta v_{CE} = 7 - 2.5\cos(\omega t)$ V. This example shows that the signal from the sinusoidal source ΔV_{BB} is greatly amplified and appears as signals in collector current and CE voltage.

It is also clear from the figure that this happens as long as the BJT stays in the active state. As the amplitude of Δi_B is increased, the swings of BJT operating point along the load line become larger and larger. At some value of Δi_B, BJT will enter either the cut-off (when $i_B + \Delta i_B \leq 0$) or saturation state and the output signals will not be a sinusoidal function.

The above circuit, however, has several major issues:

1) The input signal, ΔV_{BB}, is in series with the V_{BB} DC voltage. As typically the input signal is the output from another two-port network, this DC voltage will also appear in the output of the previous two-port network, making two-port networks dependent on the next and system design difficult. Similarly, the output signal is usually taken either across R_C as $R_C \times i_C$ or as v_{CE}. These output voltages have DC components which is of no interest and can cause problems in the design of the next two-port network. Basically, we have two choices: a) We can use capacitors to "add" or "subtract" the DC bias to/from the signal. This is called capacitive coupling (discussed in Sec. 4.2) and is the preferred method for most "discrete" circuits. b) Alternatively, we need to include the DC bias voltages in the amplifier design and analysis. This is the preferred method for ICs as capacitors take too much space on a chip. Unfortunately, this make circuit design considerably more difficult.

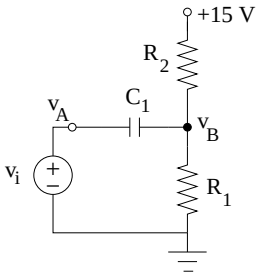
2) We have to ensure that the transistor is always in the active state or "biased" properly (Discussed in Sec. 4.3 and Sec. 4.5)

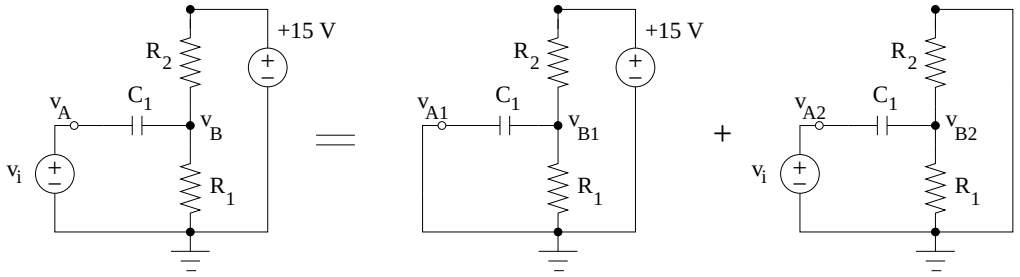
3) By definition amplifiers should be linear, *i.e.,* they should not alter the shape of the signal. However, transistors are non-linear devices. We will discuss how a non-linear device can produce a linear response in Sec. 4.4.

4.2 Capacitive Coupling

For DC voltages ($\omega = 0$) a capacitor is an open circuit (infinite impedance). For AC voltages, impedance of a capacitor, $|Z| = 1/(\omega C)$, can be made sufficiently small by choosing an appropriately large value for C (the higher the frequency, the lower the C value that one needs). This property of capacitors can be used to add or separate AC and DC voltages. Example below highlights this effect.

Consider the circuit below which includes a DC source of 15 V and an AC source of $v_i = V_i \cos(\omega t)$. We are interested to calculate voltages v_A and v_B. The best method to solve this circuit is superposition. The circuit is broken into two circuits. In circuit 1, we "kill" the AC source and keep the DC source. In circuit 2, we "kill" the DC source and keep the AC source. Superposition principle states that $v_A = v_{A1} + v_{A2}$ and $v_B = v_{B1} + v_{B2}$.





Consider the first circuit. It is driven by a DC source and, therefore, the capacitor will act as open circuit. The voltage $v_{A1} = 0$ as it is connected to ground and v_{B1} can be found by voltage divider formula: $v_{B1} = 15R_1/(R_1 + R_2)$. As can be seen both v_{A1} and v_{B1} are DC voltages.

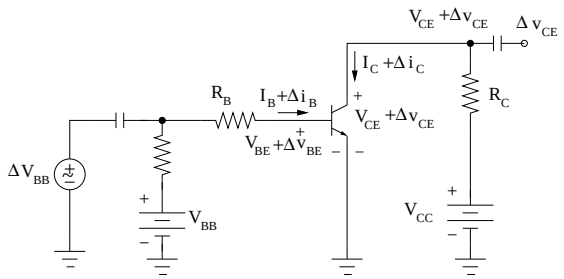
In the second circuit, resistors R_1 and R_2 are in parallel. Let $R_B = R_1 \parallel R_2$. The circuit is a high-pass filter: $V_{A2} = V_i$ and $V_{B2} = V_i(R_B)/(R_B + 1/j\omega C)$. If we operate the circuit at frequency above the cut-off frequency of the filter, *i.e.,* $R_B \gg 1/\omega C$, we will have $V_{B2} \approx V_{A2} = V_i$ and $v_{B2} \approx v_{A2} = V_i \cos(\omega t)$. Therefore, for $\omega \gg 1/R_B C$

$$v_A = v_{A1} + v_{A2} = V_i \cos(\omega t)$$

$$v_B = v_{B1} + v_{B2} = \frac{R_1}{R_1 + R_2} \times 15 + V_i \cos(\omega t)$$

Obviously, the capacitor is preventing the DC voltage to appear at point A, while the voltage at point B is the sum of DC signal from 15-V supply and the AC signal.

Using capacitive coupling, we can reconfigure our previous amplifier circuit to confine the DC bias voltages within the circuit (neither the input nor the output voltages contain the bias voltages)



Several important points:

1. Notation: As voltages/currents in analog transistor circuits are sums of bias values and responses to the signal, we will use the following notation. Upper case letters with upper case subscripts (*e.g.* V_{BE}, I_B) denote the bias components. Lower case letters with lower case subscripts (*e.g.* v_{be}, i_b) denote the signal components. Lower case letters with upper case subscripts (*e.g.* v_{BE}, i_B) denote the total value: $v_{BE} = V_{BE} + v_{be}$, *etc.* Note that although the bias component is generally a DC value, it is defined as the value when the signal is zero (not the DC value of current/voltages as the signal may have a DC component!).

2. In the above example to demonstrate the capacitive coupling concept, we used superposition to find the circuit response. We could do so because the circuit was linear. However transistor is a non-linear element. We CANNOT use superposition to find the response to bias or signal independently (although the method we will use looks a lot like superposition). We will see this when we discuss small-signal model.

3. In general, a signal is a time dependent function. We discussed in Sec. 1 that we can decompose a signal into a sum of sin-waves using Fourier transform and only consider the response the circuit to sinusoidal signals. As we saw in the example above, coupling capacitors act as high-pass filters (each capacitor having its own cut-off frequency or pole). As such, the response of the amplifier to the signal would also include these poles. Typically, we compute the response of the amplifier at frequencies above these poles (called "mid-frequency response"). At these frequencies, coupling capacitors can be assumed to be short-circuit. We separately calculate values of poles introduced by each coupling capacitors and deduce the lower cut-off frequency of the amplifier.

4) The input signal can have a DC component ($\omega = 0$ component in the Fourier decomposition). If we use coupling capacitors, the DC component of the signal is lost. This type of amplifiers is called an AC amplifier (it only amplifies AC signals). In order to amplify the DC component of the signal, we need to avoid using coupling capacitors. Such a circuit is typically called a DC amplifier (although it amplifies both DC and AC signals!)

4.3 Biasing

The purpose of biasing is to ensure that the BJT remains in the active state (or MOS in saturation) at all times. The major issue faced in biasing is that the location of the bias point can be very sensitive to transistor parameters (*i.e.,* manufacturing, temperature). As such, we will develop circuits that "force" the bias point to be independent of the transistor parameters to a large extent through feedback. As such, a simple model, such as the BJT large-signal piecewise linear model of page 3-6 is quite adequate for bias calculations. Also, the Early effect in BJTs and Channel-width modulation effect in MOS are usually ignored.

Because the BJT has to remain in the active state (or MOS in saturation), the location of the Q point determines the maximum size of the output signal. For example, consider the BJT load line discussion of page 4-1. The output voltage is $v_{CE} = V_{CE} + v_{ce}$ (note V_{CE} is always positive but v_{ce} can be negative). For BJT to remain in active state, we need:

$$v_{CE} = V_{CE} + v_{ce} \geq V_{D0} \quad \rightarrow \quad v_{ce} \geq -(V_{CE} - V_{D0})$$
$$i_C > 0 \quad \text{and CE-KVL} \quad \rightarrow \quad v_{CE} = V_{CE} + v_{ce} < V_{CC} \quad \rightarrow \quad v_{ce} < V_{CC} - V_{CE}$$

The first equation limits "negative" v_{ce} values as $V_{CE} \geq V_{D0}$. If $|v_{ce}|$ is raised above $V_{CE} - V_{D0}$ (by increasing the input signal amplitude), BJT will enter saturation. This is a universal limit and does not depend on how a transistor biased. The second equation limits positive v_{ce} values (or BJT will enter the cut-off state). This latter condition depends on how the transistor is biased (through CE-KVL). The limit above, $v_{ce} < V_{CC} - V_{CE}$, is derived for circuit of page 4-1.

It is clear that if the signal amplitude is raised above either of these limits, the output will depart from a linear response (top and/or bottom of the signal would be clipped). In this case, amplifier is said to be "saturated" (or hit the rails).

Similarly the maximum amplitude of the output signal in a MOS amplifier can be found:

$$v_{DS} \geq v_{GS} - V_t \quad \rightarrow \quad v_{ds} > v_{gs} - (V_{DS} - V_{GS} + V_t) \approx -(V_{DS} - V_{GS} + V_t)$$
$$i_D > 0 \quad \text{and DS-KVL} \quad \rightarrow \quad v_{ds} < ...$$

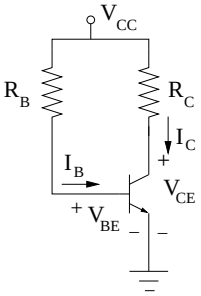
The first equation limits "negative" v_{ds} values (assuming $|v_{ds}| \gg |v_{gs}|$) and is universal. If $|v_{ds}|$ is raised above $V_{DS} - V_{GS} + V_t$, MOS will enter the triode state. The second equation limits positive v_{ds} value (or MOS will enter cut-off state) and depends on DS-KVL.

Above considerations generally imply that locating the Q point in the middle of the load line (*i.e.,* $V_{CE} = 0.5V_{CC}$ for BJT) would lead to the largest possible output signal.

Another consideration for choosing the Q point is the power dissipation in the transistor when there is no signal (and amplifier is not doing anything!). For BJT, the bias point power dissipation is $V_{CE}I_C$. Locating the Q point close to $I_C = 0$ (cut-off) or $V_{CE} = 0$ (saturation) would lead to the smallest power dissipation (but also the smallest output signal). For MOS, the bias point power dissipation is $V_{DS}I_D$. Locating the Q point close to $I_D = 0$ (cut-off) or $V_{DS} = V_{GS} - V_t$ (saturation) would lead to the smallest power dissipation (but also the smallest output signal). Typically, power dissipation is a concern only in the "power" stages of an amplifier and special classes of amplifiers are utilized to minimize power dissipation (see for example Sedra and Smith, 6th Ed., Chapter 11).

4.3.1 BJT Fixed Bias

This is the simplest bias circuit and is usually referred to as "fixed bias" as a fixed voltage is applied to the BJT base. As we like to have only one power supply, the base circuit is also powered by V_{CC}. Assuming that BJT is in active state, we have:



$$\text{BE-KVL:} \quad V_{CC} = I_B R_B + V_{BE} \quad \rightarrow \quad I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_C = \beta I_B = \beta \frac{V_{CC} - V_{BE}}{R_B}$$

$$\text{CE-KVL:} \quad V_{CC} = I_C R_C + V_{CE} \quad \rightarrow \quad V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = V_{CC} - \beta \frac{R_C}{R_B}(V_{CC} - V_{BE})$$

For a given circuit (known R_C, R_B, V_{CC}, and BJT β) the above equations can be solved to find the Q-point (I_B, I_C, and V_{CE}). Alternatively, one can use the above equations to design a BJT circuit to operate at a certain Q point. (Note: Do not memorize the above equations or use them as formulas, they can be easily derived from simple KVLs).

Example 1: Find values of R_C, R_B in the above circuit with $\beta = 100$ and $V_{CC} = 15$ V so that the Q-point is $I_C = 25$ mA and $V_{CE} = 7.5$ V.

Since the BJT is in the active state ($V_{CE} = 7.5 > V_{D0}$), $I_B = I_C/\beta = 0.25$ mA. BE-KVL and CE-KVL result in:

$$\text{BE-KVL:} \quad V_{CC} + R_B I_B + V_{BE} = 0 \quad \rightarrow \quad R_B = \frac{15 - 0.7}{0.250} = 57.2 \text{ k}\Omega$$

$$\text{CE-KVL:} \quad V_{CC} = I_C R_C + V_{CE} \quad \rightarrow \quad 15 = 25 \times 10^{-3} R_C + 7.5 \quad \rightarrow \quad R_C = 300 \ \Omega$$

Example 2: Consider the circuit designed in example 1. What is the Q point if $\beta = 200$.

We have $R_B = 57.2$ kΩ, $R_C = 300$ Ω, and $V_{CC} = 15$ V but I_B, I_C, and V_{CE} are unknown. Assuming that the BJT is in the active state:

$$\text{BE-KVL:} \quad V_{CC} + R_B I_B + V_{BE} = 0 \quad \rightarrow \quad I_B = \frac{V_{CC} - V_{BE}}{R_B} = 0.25 \text{ mA}$$

$$I_C = \beta I_B = 50 \text{ mA}$$

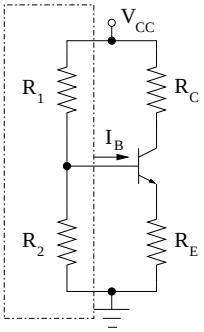
$$\text{CE-KVL:} \quad V_{CC} = I_C R_C + V_{CE} \quad \rightarrow \quad V_{CE} = 15 - 300 \times 50 \times 10^{-3} = 0$$

As $V_{CE} < V_{D0}$ the BJT is not in the active state (since $I_C > 0$, it should be in saturation).

The above examples show the problem with our simple fixed-bias circuit as the β of a commercial BJT can depart substantially from its average value given in the manufacturers' spec sheet (due to manufacturing or more importantly due to a change in temperature). In a given BJT, I_C increases by 9% per °C for a fixed V_{BE} (because of the change in β). Consider a circuit which is tested to operate perfectly at 25°C. At 35°C, β and I_C will be roughly doubled and the BJT can be in saturation! In fact, the circuit has a build-in positive feedback. If the temperature rises slightly, the corresponding increase in β makes I_C larger. Since the power dissipation in the transistor is $V_{CE}I_C$, the transistor may get hotter which increases transistor β and I_C further and can cause a "thermal runaway."

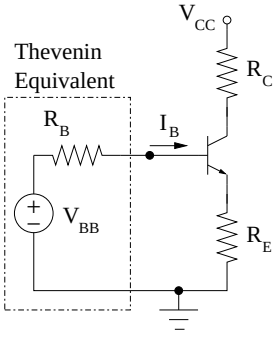
The problem is that our biasing circuit fixes the value of I_B (independent of BJT parameters) and, as a result, both I_C and V_{CE} are directly proportional to BJT β (see formulas in the previous page). A biasing scheme should be found that make the Q-point (I_C and V_{CE}) independent of transistor β and insensitive to the above problems → Use negative feedback!

4.3.2 BJT Emitter Degeneration Bias with a Voltage-Divider



The key to this biasing scheme is the emitter resistor which provides negative feedback. It is called "emitter degeneration" as the presence of R_E makes the circuit to behave very differently than when R_E is not present (even as an amplifier). This biasing scheme can be best analyzed and understood if we replace the voltage divider (portion in the dashed box) with its Thevenin equivalent:

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC} \qquad \text{and} \qquad R_B = R_1 \parallel R_2$$



The emitter resistor, R_E, provides the negative feedback. Suppose I_C becomes larger than the designed value (*e.g.,* larger β due to an increase in temperature). Then, $V_E = R_E I_E$ will increase. Since V_{BB} and R_B do not change, KVL in the BE loop shows that I_B should decrease. This will reduce I_C back towards its design value. If I_C becomes smaller than its design value opposite happens, I_B has to increase which will increase and stabilize I_C.

Analysis below shows that the Q point is indeed independent of BJT β:

$$I_C = \beta I_B, \qquad I_E = (\beta + 1) I_B$$

$$\text{BE-KVL:} \qquad V_{BB} = R_B I_B + V_{BE} + I_E R_E \quad \rightarrow \quad I_B = \frac{V_{BB} - V_{BE}}{R_B + (1+\beta) R_E}$$

CE-KVL: $V_{CC} = R_C I_C + V_{CE} + I_E R_E \quad \rightarrow \quad V_{CE} = V_{CC} - I_C \left[R_C + \frac{1+\beta}{\beta} R_E \right]$

Choose R_B such that $\underline{R_B \ll (1+\beta) R_E}$ (this is the condition for the feedback to be effective):

$$I_B \approx \frac{V_{BB} - V_{BE}}{(1+\beta) R_E}, \qquad I_C \approx I_E \approx \frac{V_{BB} - V_{BE}}{R_E}$$

$$V_{CE} \approx V_{CC} - \frac{R_C + R_E}{R_E} (V_{BB} - V_{BE})$$

where we have use $(1+\beta)/\beta \approx 1$. Note that now both I_C and V_{CE} are independent of β.

Another way to see how the circuit works is to consider BE-KVL: $V_{BB} = R_B I_B + V_{BE} + I_E R_E$. If we choose $R_B \ll (1+\beta) R_E \approx (I_E/I_B) R_E$ or $R_B I_B \ll I_E R_E$ (the feedback condition above), the KVL reduces to $V_{BB} \approx V_{BE} + I_E R_E$, forcing a constant I_E independent of the BJT β. As $I_C \approx I_E$ this will also fixes the Q point of BJT. If the BJT parameters change (different β due to a change in temperature), the circuit forces I_E to remain fixed and changes I_B accordingly. This biasing scheme is one of several methods which fix I_C and V_{CE} and forces the BJT to adjust I_B (through negative feedback) to achieve the proper bias.

Another important point follows from $V_{BB} \approx V_{BE} + I_E R_E$. As V_{BE} is not a constant and can change slightly (can drop to 0.6 or increase to 0.8 V for a Si BJT), we need to ensure that $I_E R_E$ is much larger than possible changes in V_{BE}. As changes in $V_{BE} = V_{D0}$ is about 0.1 V, we need to ensure that $V_E = I_E R_E \gg 0.1$ or $\underline{V_E > 10 \times 0.1 = 1 \text{ V}}$.

Example: Design a stable bias circuit with a Q point of $I_C = 2.5$ mA and $V_{CE} = 7.5$ V. Transistor β ranges from 50 to 200.

Step 1: Find V_{CC}: As we like to have the Q-point to be located in the middle of the load line, we set $V_{CC} = 2V_{CE} = 2 \times 7.5 = 15$ V.

Step 2: Find R_C and R_E:

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \quad \rightarrow \quad R_C + R_E = \frac{7.5}{2.5 \times 10^{-3}} = 3 \text{ k}\Omega$$

We are free to choose either R_C or R_E (we will see that the amplifier response sets the values of R_C and R_E). However, we need $V_E = I_E R_E > 1$ V or $R_E > 1/I_E = 400\ \Omega$. Let's choose $R_E = 1$ kΩ which gives $R_C = 3 - R_E = 2$ kΩ (both commercial values).

Step 3: Find R_B and V_{BB}: We need to set $R_B \ll (1 + \beta)R_E$. As any commercial BJT has a range of β values and we want to ensure that the above inequality is always satisfied, we should use the minimum β value:

$$R_B \ll (1 + \beta_{min})R_E \quad \rightarrow \quad R_B = 0.1(1 + \beta_{min})R_E = 0.1 * 51 * 1,000 = 5.1 \text{ k}\Omega$$
$$V_{BB} \approx V_{BE} + I_E R_E = 0.7 + 2.5 \times 10^{-3} \times 10^3 = 3.2 \text{ V}$$

Step 4: Find R_1 and R_2

$$R_B = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2} = 5.1 \text{ k}\Omega$$
$$\frac{V_{BB}}{V_{CC}} = \frac{R_2}{R_1 + R_2} = \frac{3.2}{15} = 0.21$$

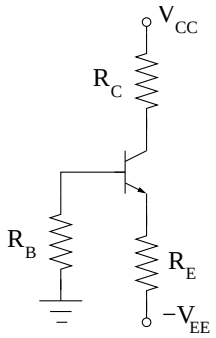
The above are two equations in two unknowns (R_1 and R_2). The easiest way to solve these equations are to divide the two equations to find R_1 and use that in the equation for V_{BB}:

$$R_1 = \frac{5.1 \text{ k}\Omega}{0.21} = 24 \text{ k}\Omega$$
$$\frac{R_2}{R_1 + R_2} = 0.21 \quad \rightarrow \quad 0.79R_2 = 0.21R_1 \quad \rightarrow \quad R_2 = 6.4 \text{ k}\Omega$$

Reasonable commercial values for R_1 and R_2 are and 24 kΩ and 6.2 kΩ, respectively.

The voltage divider biasing scheme is used frequently in BJT amplifiers. However, as $V_B > 0$, a coupling capacitor is needed to attach the input signal to the amplifier circuit. As a result, this biasing scheme leads to an "AC" amplifier (cannot amplify DC signals). In some applications, we need "DC" amplifiers. Biasing with two voltage sources, discussed below, can solve this problem.

4.3.3 BJT Emitter Degeneration Bias with 2 Voltage Sources



This scheme is similar to the voltage-divider method. We have only changed location of the zero voltage node. We should get the same currents through and voltages across each element as before if we replace V_{BB} with V_{EE} in the previous expressions and replace V_{CC} with $V_{CC}+V_{EE}$ (Understand why!). We should find that this is a stable bias point as long as $R_B \ll (1+\beta)R_E$.

BE-KVL: $$R_B I_B + V_{BE} + R_E I_E - V_{EE} = 0$$

$$R_B \frac{I_E}{1+\beta} + R_E I_E = V_{EE} - V_{BE} \quad \rightarrow \quad I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/(1+\beta)}$$

Similar to voltage-divider case, if we choose R_B such that, $R_B \ll (1+\beta)R_E$:

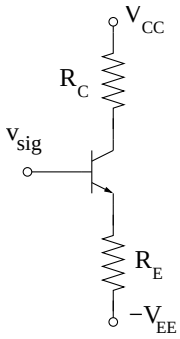
$$I_C \approx I_E \approx \frac{V_{EE} - V_{BE}}{R_E} = const$$

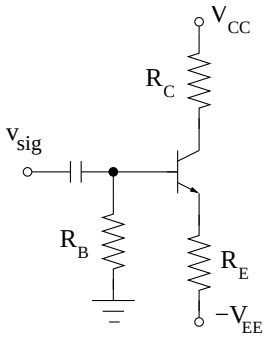
CE-KVL: $$V_{CC} = R_C I_C + V_{CE} + R_E I_E - V_{EE}$$

$$V_{CE} = V_{CC} + V_{EE} - I_C(R_C + R_E) = const$$

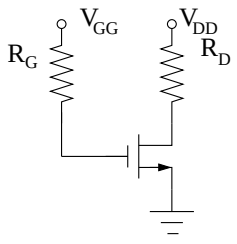
Note that above formulas are the same as those of page 4-7 (with $V_{BB} \rightarrow V_{EE}$ and $V_{CC} \rightarrow V_{CC}+V_{EE}$). Again, I_C and V_{CE} are independent of β and bias point is stable. Similar to the voltage-divider case, we need to ensure that $R_E I_E \geq 1$ V to account for variations in V_{BE}.

Since the condition for stable bias is $R_B \ll (1+\beta)R_E$, it appears that the best choice for R_B would be $R_B = 0$, eliminating R_B from the circuit altogether (connecting the BJT base to the ground). Indeed this is the preferred method if the signal is directly coupled to the circuit (see figure left below, when $v_{Sig} = 0$, the BJT base will be grounded). However, R_B is necessary if a coupling capacitor were used. At the bias condition when the coupling capacitor is an open circuit, the BJT base would not be connected to the ground if R_B did not exist and the bias would not work. In the case of a coupling capacitor, value of R_B should be chosen as the largest possible value that would satisfy $R_B \ll (1+\beta)R_E$ as R_B appears as a load for the previous stage (we will discuss this issue in depth later).





4.3.4 MOS Fixed Bias



The fixed-bias scheme for MOS is similar to the BJT fixed bias, but there are some differences: a) Two voltage sources are required as $I_G = 0$; 2) R_G is not necessary for biasing but is necessary when if coupling capacitors were used (see discussion of previous page).

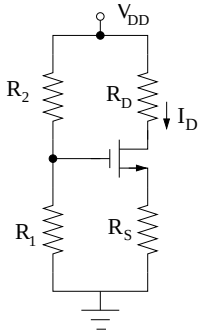
GS-KVL: $V_{GS} = V_{GG}$

$$I_D = 0.5k'_n(W/L)_n(V_{GS} - V_t)^2 = 0.5k'_n(W/L)_n(V_{GG} - V_t)^2$$

DS-KVL: $V_{DD} = I_D R_D + V_{DS} \quad \rightarrow \quad V_{DS} = V_{DD} - 0.5k'_n(W/L)_n R_D(V_{GG} - V_t)^2$

Similar to the BJT β, both V_t and $k'_n(W/L)_n$ vary due to the manufacturing variation and temperature. For example, as temperature is increased, both V_t and k'_n decrease: decreasing k'_n decreases I_D while decreasing V_t raises I_D. The net effect (usually) is that I_D decreases. While the "thermal runaway" is not a problem in MOS, the bias point is not stable.

4.3.5 MOS Bias with Source Degeneration



Similar to the BJT bias circuits, addition of a resistor R_S provides the negative feedback necessary to stabilize the bias point. If we replace the voltage divider with its Thevenin equivalent, we get:

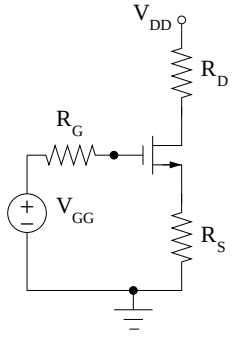
$$V_{GG} = \frac{R_2}{R_1 + R_2} V_{DD}$$

$$R_G = R_1 \parallel R_2$$

GS-KVL: $V_{GG} = V_{GS} + R_S I_D$

$$I_D = 0.5k'_n(W/L)_n(V_{GG} - V_t)^2$$

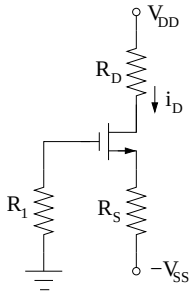
DS-KVL: $V_{DD} = I_D R_D + V_{DS} + I_D R_S$



If we substitute for I_D from the MOS characteristics equation in GS-KVL, we get a quadratic equation for V_{GS} that can be solved to find V_{GS} (and I_D). The value of V_{DS} can then be find from DS-KVL.

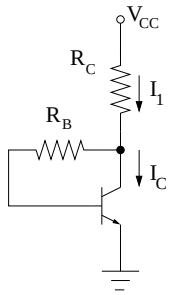
The negative feedback action can be seen by noting that since $V_{GS} = V_{GG} - R_S I_D$, any decrease in I_D would increase V_{GS} which would result in an increase I_D. Similarly, any increase in I_D would decrease V_{GS} and decreases I_D. As a result, I_D will stay nearly constant (it is not nearly constant like I_E in a BJT, rather I_D variations become much smaller by the negative feedback).

Another difference between voltage-divider bias for MOS with that of BJT is that in the case of BJT, we have to ensure that $R_B \ll (1+\beta)R_E$ for negative feedback to be effective. This generally limits the value of R_1 and R_2. In a MOS, $I_G = 0$ and no such limitation exists. Therefore, R_1 and R_2 can be taken to be large (MΩ) which is important in the amplifier response as is discussed later.



Similar to the BJT case, two voltage sources can be used. Again, we can eliminate R_G from the circuit if the signal can be coupled directly to the transistor.

4.3.6 Self Bias



This is another stable biasing scheme. This scheme uses R_c as the feedback resistor. The interesting property of this biasing scheme is that the transistor is always in active state. We write a KVL through BE and CE terminals:

$$V_{CE} = R_B I_B + V_{BE} = R_B I_B + V_{D0} > V_{D0}$$

Since $V_{CE} > V_{D0}$, BJT is always in the active state with $i_C/i_B = \beta$. Noting (by KCL) that $I_1 = I_C + I_B$:

$$\text{BE-KVL:} \qquad V_{CC} = R_C I_1 + R_B I_B + V_{BE} = R_C I_C + (R_B + R_C)\frac{I_C}{\beta} + V_{D0}$$

$$I_C = \frac{V_{CC} - V_{D0}}{R_C + (R_C + R_B)/\beta}$$

If, $(R_B + R_C)/\beta \ll R_C$ or $R_B \ll (\beta - 1)R_C$, we will have:

$$I_C \approx \frac{V_{CC} - V_{D0}}{R_C}$$

and the bias point is stable as I_C is independent of β.

To see the negative feedback effect, rewrite BE-KVL as:

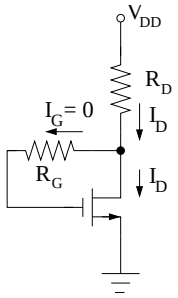
$$I_B = \frac{V_{CC} - V_{D0} - R_C I_C}{R_B}$$

Suppose that the circuit is operating and BJT β is increased (*e.g.,* an increase in the temperature). In this case I_C will increase which raises the voltage across resistor R_C ($R_C I_C$).

From the above equation, this will lead to a reduction in I_B which, in turn, will decrease $I_C = \beta I_B$ and compensate for any increase in β. If BJT β is decreased (*e.g.,* a decrease in the temperature), I_C will decrease which reduces the voltage across resistor R_C ($R_C I_C$). From the above equation, this will lead to an increase in I_B which, in turn, will increase $I_C = \beta I_B$ and compensate for any decrease in β.

The issue with this bias scheme is that it automatically includes a feedback (*i.e.,* a connection) between the input and output of the transistor through R_B which has an important impact on the amplifier response.

MOS fixed bias case is shown. Similar to the BJT case, this configuration ensures that MOS is always in saturation. Since $I_G = 0$, $V_{DS} = V_{GS} > V_{GS} - V_{tn}$. The bias parameters can be found from:



$$\text{DS-KVL:} \quad V_{DD} = I_D R_D + V_{GS}$$

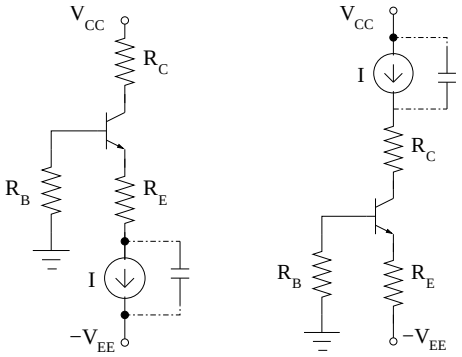
$$I_D = 0.5 k'_n (W/L)_n (V_{GG} - V_t)^2$$

where we have used $V_{DS} = V_{GS}$. The above two equations can be solved to find a unique set of I_D and V_{GS} (or alternatively, for a given bias we can calculate R_D).

Note that as $I_G = 0$, value of R_G does not affect the bias parameters. However, R_G cannot be removed from the circuit (*i.e.,* replaced with a short circuit) as in this case, the gate and drain will be directly connected to each other leading to a two-terminal element (see Problem 23).

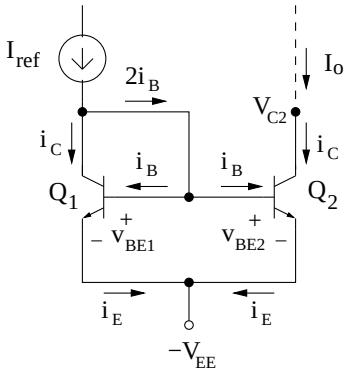
4.3.7 Biasing with Current Mirrors

The stable biasing techniques above (emitter or source degeneration) essentially operate the same way: They set I_E (and $I_C \approx I_E$) in the BJT or $I_S = I_D$ in MOS independent of the transistor parameters. In principle, the same objective can be achieved (and with a higher accuracy) if we could bias the transistor with a current source as is shown for a BJT. We need to bias the transistor with two voltage sources, however.



By using a current source, no bias resistor is needed and we only need to include resistors necessary for signal amplification. As such, biasing with a current source is the preferred way in most integrated circuits as resistors take a lot of space on the chip compared to transistors. Note that if we use an ideal current source, a "by-pass" capacitor is needed in parallel to the current source. If such a capacitor were not included, the collector current

will remain fixed at $i_c = I$ regardless of the signal. The capacitor allows the signal to by-pass the current source. We will see that we can design circuits that act as a current source for bias voltage but not for the signal. For these circuits, no bypass capacitor is needed. An example of such a circuit is a current mirror.



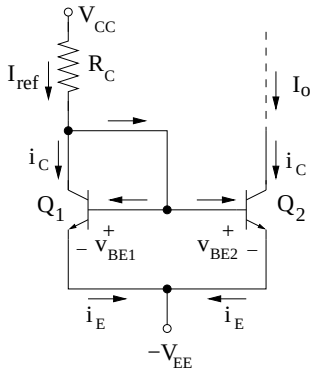
Consider the circuit shown with two identical transistors. Because I_{ref} flows in Q1, it should be ON. As $V_{CE1} = V_{BE1} = V_{D0}$, Q1 has to be in the active state. Since both bases and emitters of transistors are connected together, KVL leads to $V_{BE1} = V_{BE2}$. Then, BJT equations (Page 3-3) indicate that $I_{C1} = I_{C2} \equiv I_C$ if we ignore the Early effect. Similarly, $I_{B1} = I_{B2} \equiv I_B$ and, therefore, $I_{E1} = I_{E2} \equiv I_E$. Assuming that Q2 is in the active state

$$I_B = \frac{I_C}{\beta}, \qquad I_o = I_C = \beta I_B$$

KCL: $$I_{ref} = I_C + 2I_B = (\beta + 2)I_B$$

$$\frac{I_o}{I_{ref}} = \frac{\beta}{\beta + 2} = \frac{1}{1 + 2/\beta}$$

For $\beta \gg 1$, $I_o \approx I_{ref}$ (with an accuracy of $2/\beta$). This circuit is called a "current mirror" as the two transistors work in tandem to ensure that current I_o remains the same as I_{ref} no matter what circuit is attached to the collector of Q_2. As such, the circuit behaves as a current source and can be used to bias BJT circuits, *i.e.,* Q_2 collector is attached to the emitter circuit of the BJT amplifier to be biased.



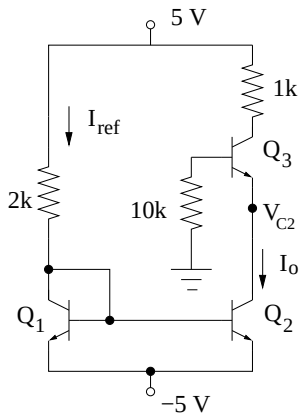
Note that we had assumed that Q2 is in the active state. This requires that $V_{CE2} = V_{C2} + V_{EE} \geq V_{D0}$ or $V_{C2} \geq V_{EE} + V_{D0}$.

Value of I_{ref} can be set in many ways. The simplest is by using a resistor R_c as is shown. By KVL, we have:

$$V_{CC} = R_C I_{ref} + V_{BE1} - V_{EE}$$

$$I_{ref} = \frac{V_{CC} + V_{EE} - V_{D0}}{R_C} = const$$

Example: Find the bias point of Q3 (Si BJTs with $\beta = 100$).



Q1 and Q2 from a current mirror. Therefore, $I_o \approx I_{ref}$ as long as Q2 is in the active state. BE-KVL for Q1 gives I_{ref}:

$$\text{BE1-KVL:} \quad 5 = 2 \times 10^3 I_{ref} + V_{BE1} + (-5)$$
$$I_{ref} = 4.65 \text{ mA}$$

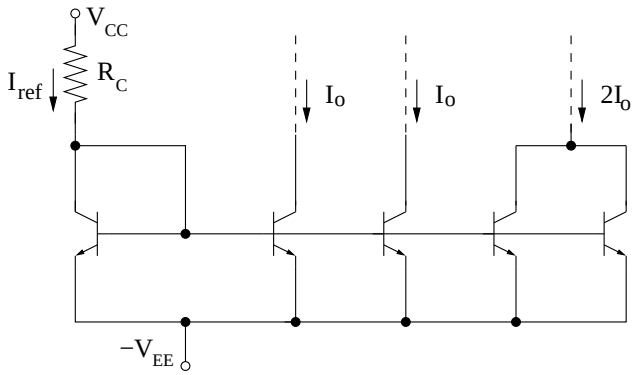
Therefore, $I_{E3} = I_o \approx 4.65$ mA and Q3 is ON with $V_{BE3} = V_{D0} = 0.7$ V. Assuming Q3 active:

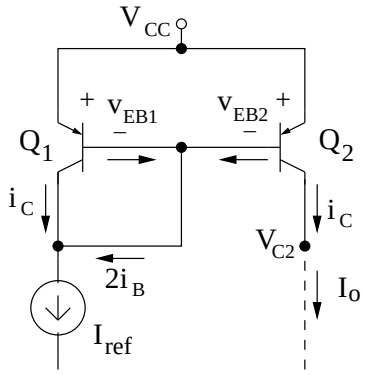
$$I_{B3} = I_{E3}/(1+\beta) = 46\ \mu\text{A}, \quad I_{C3} = I_{E3} - I_{B3} = 4.60 \text{ mA}$$
$$\text{BE3-KVL:} \quad 0 = 10 \times 10^3 I_{B3} + V_{BE3} + V_{C2} \quad \rightarrow \quad V_{C2} = -1.16 \text{ V}$$
$$\text{CE3-KVL:} \quad 5 = 10^3 I_{C3} + V_{CE3} + V_{C2} = 4.6 + V_{CE3} - 1.16 \quad \rightarrow \quad V_{CE3} = 1.56 \text{ V}$$

As $V_{CE3} > V_{D0} = 0.7$ V, assumption of Q3 in active is justified. We also need to show that the current mirror acts properly, *i.e.,* Q2 is in active. We find $V_{CE2} = V_{C2} - (-5) = 3.84 > V_{D0}$.

In the simple current mirror circuit above, $I_o \approx I_{ref}$ with a relative accuracy of $2/\beta$ and I_{ref} is constant with an accuracy of small changes in V_{BE1}. Variations of the above simple current mirror, such as Wilson current mirror and Widlar current mirror, have $I_o \approx I_{ref}$ even with a higher accuracy and also compensate for the small changes in V_{BE} (See Problems). Wilson current mirror is especially popular because it replace R_c with a transistor.

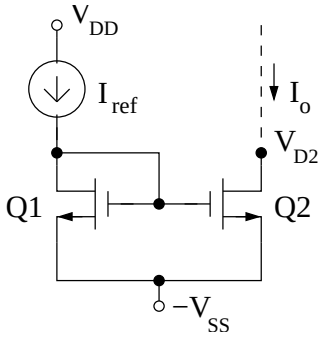
The right hand part of the current mirror circuit can be duplicated such that one current mirror circuit can bias several BJT circuits as is shown. In fact, by coupling output of two or more of the right hand BJTs, integer multiples of I_{ref} can be made for biasing circuits which require a higher bias current as is shown below (left figure). Similarly, a current mirror can be constructed with the PNP transistors (right figure below).





Similar current mirror circuits can be constructed with MOSFETs. MOS allows greater flexibility. Assume Q1 and Q2 are constructed on the same chip and close to each other such that both have the same k'_n and V_t.

From the circuit, as $I_{G1} = 0$, $I_{D1} = I_{ref}$. Also, $I_0 = I_{D2}$ and $V_{GS2} = V_{GS1} \equiv V_{GS}$. Note that Q1 is always in saturation because $V_{DS1} = V_{GS1} > V_{GS1} - V_t$. Assume Q2 in saturation:



$$I_{ref} = I_{D1} = 0.5k'_n(W/L)_1(V_{GS} - V_t)^2$$

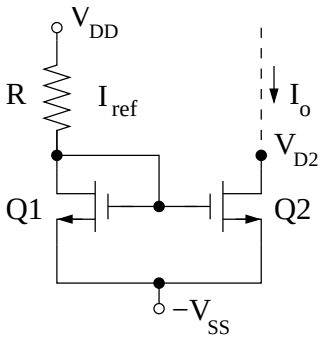
$$I_o = I_{D2} = 0.5k'_n(W/L)_2(V_{GS} - V_t)^2$$

$$\frac{I_o}{I_{ref}} = \frac{(W/L)_2}{(W/L)_1}$$

As such, we can set I_o to any desired value by controlling $(W/L)_2$. (Note that if Q1 and Q2 were identical, $I_o = I_{ref}$.) For Q2 in saturation, we need:

$$V_{DS2} = V_{D2} - (-V_{SS}) > V_{GS2} - V_t \quad \rightarrow \quad V_{D2} > -V_{SS} + V_{GS2} - V_t$$

Similar to simple BJT current mirror, value of I_{ref} can be set by using a resistor R as is shown. By KVL, we have:

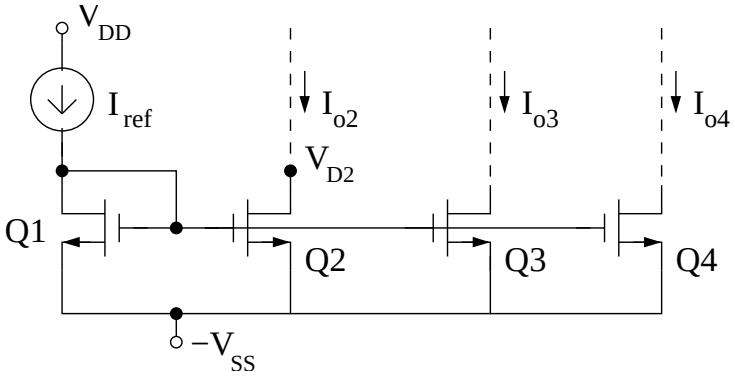


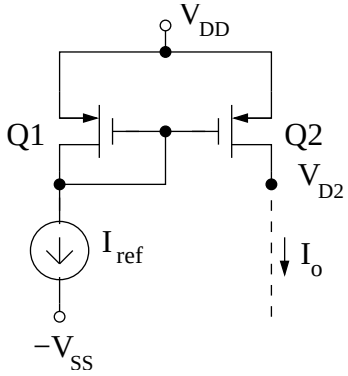
$$V_{DD} = RI_{ref} + V_{GS1} - V_{SS}$$

$$I_{ref} = I_{D1} = 0.5k'_n(W/L)_1(V_{GS1} - V_t)^2$$

The above equations can be solved to find V_{GS1} and I_{ref} (or alternatively, for a desired I_{ref} one can find V_{GS1} and R).

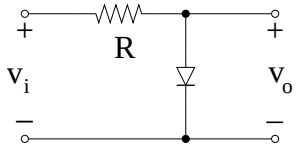
Similar to a BJT current mirror, the right hand part of the current mirror circuit can be duplicated such that one current mirror circuit can bias several MOS circuits as is shown. MOS allows much greater flexibility as by adjusting (W/L) of each transistor, arbitrary bias currents can be generated. Similarly, a current mirror can be constructed with the PMOS transistors (right figure below).

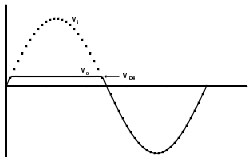




4.4 Small Signal Model

In previous sections, we have studies three type of non-linear elements/devices: diode, BJT, and MOS. In general a circuit containing these elements is non-linear and will have a non-linear transfer function. For example, consider the clipper circuit below. For a diode with $V_{D0} = 0.7$ V, we found that input voltages above 0.7 V will be clipped (see below). Figure below shows the response of the circuit when $v_i = 5\cos(\omega t)$. Obviously as output and input waveforms have different shapes, the system response is non-linear.

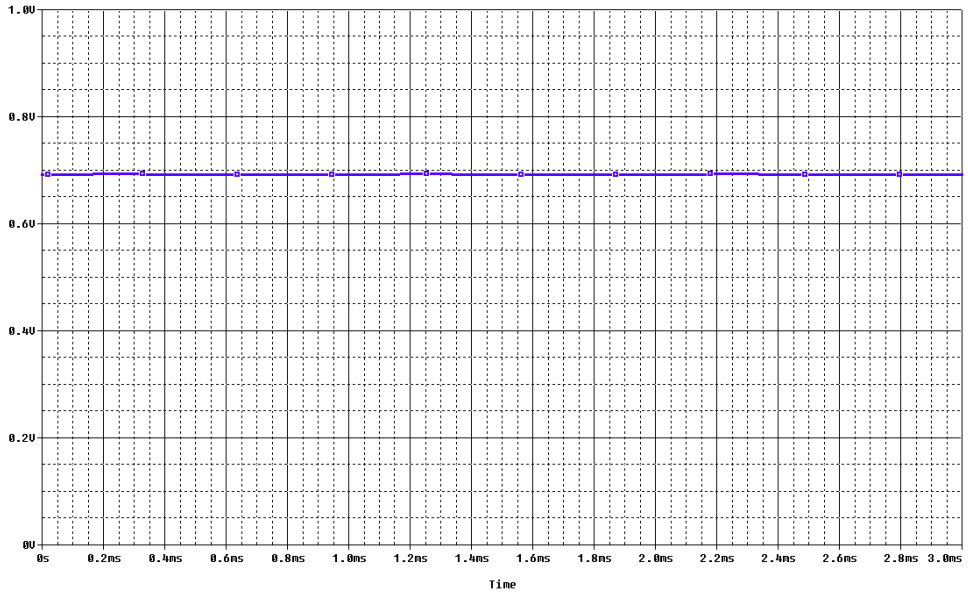




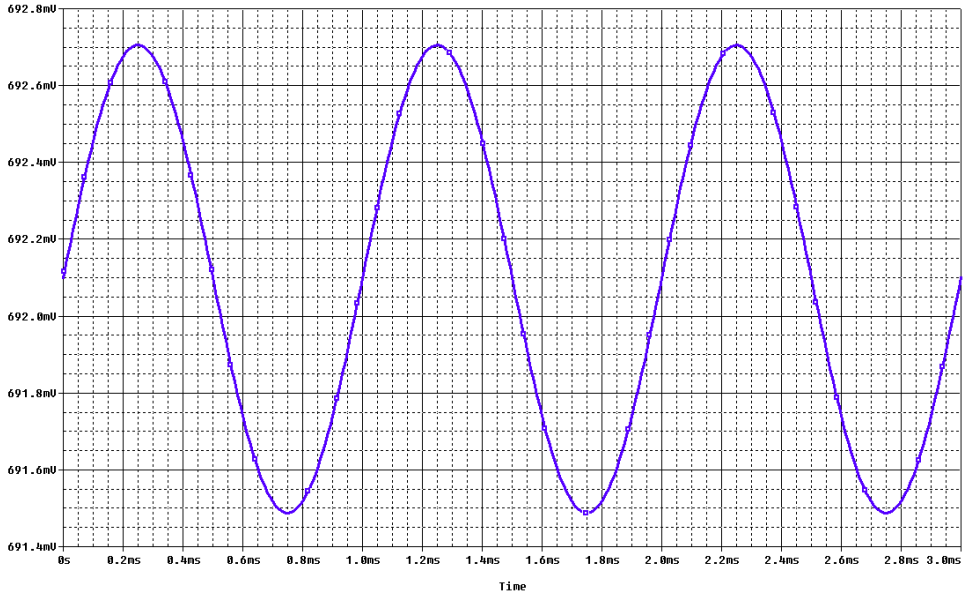
Now, consider the same circuit with $v_i = 5 + 0.05\cos(\omega t)$. For distinction, we call the $0.05\cos(\omega t)$ part of the input voltage the signal (similar to ΔV_{BB} signal that we applied to a BJT in page 3-1) and the constant large 5 V the bias voltage.

Solve this circuit with our constant-voltage-drop model, we find that as $v_i > 0.7 = V_{D0}$ at all times, diode is always ON and $v_o = V_{D0} = 0.7$ V.

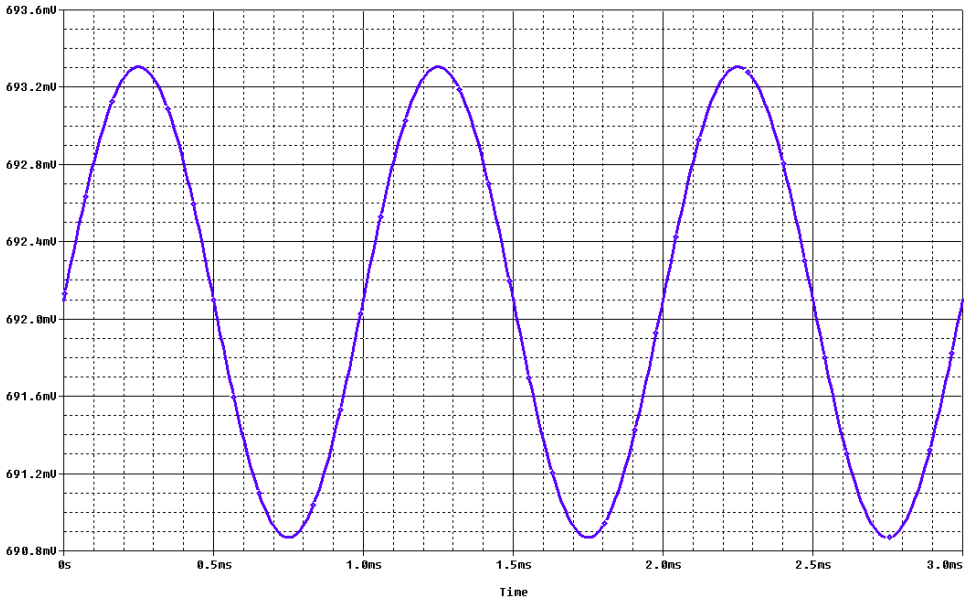
Now let's simulate the same circuit with PSpice (1N4148 diode, $R = 750\ \Omega$, and 1 kHz). PSpice results for this circuit is very close to what one see in the lab. The figure below shows the simulation result with $v_O \approx 0.69$ V, very close to the estimate from the piecewise linear model.



Now, let's zoom on the v_o plot from PSpice. We see that the output waveform is actually composed of two parts: A DC part and a sine wave (similar to the input signal): $v_o = 692.1 + 0.6\sin(\omega t)$ mV. Interestingly, if we simulate the same circuit with $v_i = 5$ V (no signal), the output voltage would be exactly 692.1 mV.



This simulation (or experiment) indicates that when we add a small signal to the DC bias input voltage, a similar shape signal appears at the output. Moreover, if double the signal amplitude: $v_i = 5 + 0.1\cos(\omega t)$ and run the simulation, we find the output signal amplitude is also doubled: $v_o = 692.1 + 1.2\sin(\omega t)$ mV as is shown below.



This behavior (sine-in sine-out) and proportionality (double the input, output is doubled) is indicative of a linear system behavior. This is surprising as diode is a non-linear element. The reason for this behavior is that the input signal represents a small change in the input and the output signal represents a corresponding small change in the output voltage.

This is called the small signal behavior: For small signals, non-linear circuit elements behave as linear ones. This is the reason we can build linear circuits with diodes and transistors. Note that for this work, the non-linear element should be always in ONE particular state (*i.e.,* in the above examples, diode was always ON).

This small-signal behavior can be understood by noting that any non-linear function can be approximated in the "neighborhood" of a point by its tangent line at that particular point. Mathematically, this approximation is based on Taylor series expansion. Consider function $f(x)$. Suppose we know the value of the function and all of its derivative at some known point X_0. Then, the value of the function in the "neighborhood" of X_0 can be found from the Taylor Series expansion as:

$$f(X_0 + \Delta x) = f(X_0) + \Delta x \left.\frac{df}{dx}\right|_{x=X_0} + \frac{(\Delta x)^2}{2!}\left.\frac{d^2 f}{dx^2}\right|_{x=X_0} + ...$$

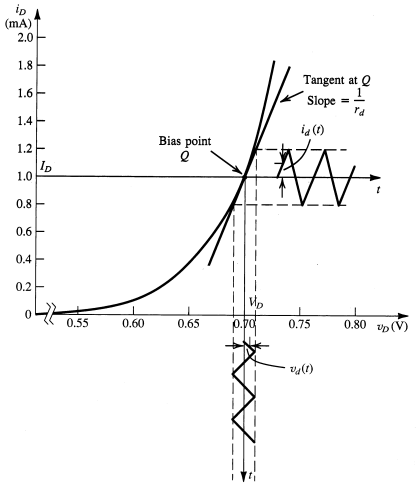
If Δx is small (*i.e.,* close to our original point of X_0), the high order terms of this expansion (terms with $(\Delta x)^n,\ n = 2, 3, ...$) usually become very small:

$$f(X_0 + \Delta x) \approx f(X_0) + \Delta x \left.\frac{df}{dx}\right|_{x=X_0}$$

As can be seen, the value of the function at a point close to X_0 is approximated by the tangent line to $f(x)$ at X_0. Let's apply this approximation to a diode.

4.4.1 Diode Small Signal Model

Consider the diode iv characteristics equation in which the diode current is a function of its voltage, $i_D(v_D)$ [similar to $f(x)$] and we apply $v_D = V_D + v_d$ to the diode with v_d being a small signal, V_D the "large" bias voltage and v_D the total voltage across the diode (here, the DC voltage V_D is X_0 and the small signal v_d is Δx). Then, following Taylor series expansion, we get:



$$
\begin{aligned}
i_D(V_D + v_d) \quad &\approx i_D(V_D) + v_d \times \left.\frac{di_D}{dv_D}\right|_{v_D=V_D} \\
&= I_D + v_d \times \left.\frac{di_D}{dv_D}\right|_{v_D=V_D}
\end{aligned}
$$

Where we have defined the bias current, $I_D \equiv i_D(V_D)$ (*i.e.,* when the signal is zero). Then, $i_d = i_D - I_D$ is the response of the diode to the signal v_d:

$$
i_D(V_D + v_d) = I_D + i_d \approx I_D + v_d \times \left.\frac{di_D}{dv_D}\right|_{v_D=V_D} \qquad \rightarrow \qquad i_d = v_d \times \left.\frac{di_D}{dv_D}\right|_{v_D=V_D}
$$

We see that the diode response (i_d) to a small signal v_d is linear. Moreover the response of the diode to a small signal is like a resistor ($i_d = v_d/r_d$) with

$$
r_d \equiv \left(di_D/dv_D|_{v_D=V_D}\right)^{-1}
$$

Note that r_d is inverse of the slope of a line tangent to $i_D v_D$ characteristics of the diode at the bias point, *i.e.,* we are approximating the diode characteristic plot with a line tangent to its bias point as is shown in the above figure.

Value of r_d can be found from the full expression for the diode current:

$$
\begin{aligned}
&i_D = I_s e^{v_D/nV_T} \qquad \rightarrow \qquad \frac{di_D}{dv_D} = \frac{1}{nV_T} \times I_s e^{v_D/nV_T} \\
&\left.\frac{di_D}{dv_D}\right|_{v_D=V_D} = \frac{1}{nV_T} \times I_s e^{V_D/nV_T} = \frac{I_D}{nV_T} \\
&r_d = \frac{nV_T}{I_D}
\end{aligned}
$$

where we have used the fact that $I_D = i_D(V_D) = I_s \exp(V_D/nV_T)$. Note that the value of r_d depends on the value of bias current, I_D, and r_d changes with temperature (through V_T).

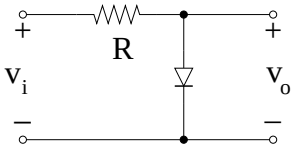
It is essential to remember that the small signal model applies only to the response of the diode to small signals, *i.e.,* the circuit solution should be divided into two parts,

1) Bias Analysis (zero signal) where we should use a large-signal model (*e.g.,* constant-voltage drop model) to find bias voltages and currents (I_D for example),

2) Small-Signal Analysis (zero out the bias values and use the small signal model of the diode, *i.e.,* r_d resistor) to compute the small-signal response.

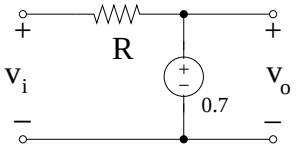
If needed, the total response of the circuit then is the sum of Bias and Small-Signal responses.

Let's analyze the circuit that we had simulated with PSpice before (1N4148 diode, $R = 750\ \Omega$, and 1 kHz) with $v_i = 5 + 0.05\cos(\omega t)$ mV. by KVL:



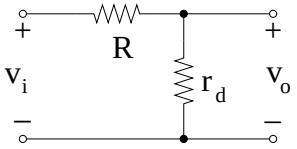
$$v_i = i_D R + v_D$$

To find the bias point, we set the signal to be zero ($v_i = 5$ V). Using the large signal constant voltage drop model, it is easy to show that the diode will be ON and $V_D = 0.7$ V. The diode bias current is



$$5 = 750 I_D + 0.7 \qquad \rightarrow \qquad I_D = 5.73 \text{ mA}$$

We now compute the response to the small signal. In this case, we need to zero out that the bias voltage ($v_i = 0.05\sin(\omega t)$ V) and use the diode small-signal model. We first compute the value of r_d from the bias current ($n = 2$ for discrete Si diodes):



$$r_d = \frac{nV_T}{I_D} = \frac{2 \times 25 \times 10^{-3}}{5.73 \times 10^{-3}} = 8.73\ \Omega$$

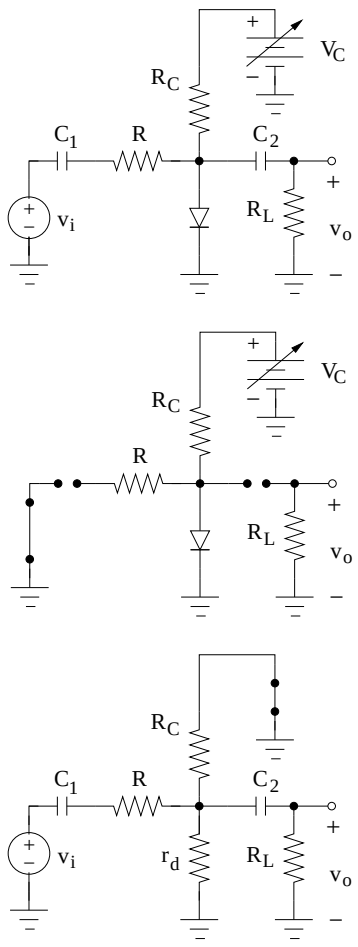
$$v_d = \frac{r_d}{r_D + R} \times 0.05\sin(\omega t) = 0.58\sin(\omega t) \text{ mV}$$

Therefore, $v_o = v_D = V_D + v_d = 700 + 0.58\sin(\omega t)$ mV which is very close to simulation results of $v_o = 692 + 0.6\sin(\omega t)$ mV.

Similarly, we can find the response to the PSpice simulation with $v_i = 5 + 0.1\cos(\omega t)$ to be $v_o = 700 + 1.16\sin(\omega t)$ mV which is again close to our simulation results of $v_o = 692 + 1.2\sin(\omega t)$ mV.

Example: Voltage-controlled Attenuator

In this circuit, v_i is a small signal sine wave, V_C is a DC source which biases the diode (and its value can be changed). Capacitors are large (*i.e.,* their impedance is small at the frequency of the signal).



Bias: We zero the signal (v_i become a short circuit). Because the voltage source, V_C, is a DC source, capacitors become open circuits (See circuit). Then,

$$I_D = \frac{V_C - VD0}{R_C}$$

Because of C_2, no voltage appears at v_o.

Small Signal Analysis: Setting bias voltage, V_C to zero will make V_C source to be grounded. We replace the diode with its small-signal model, r_d. We note that R_C, r_d, and R_L are in parallel (Caps are both short circuit). The, defining $R_p = R_C \parallel r_d \parallel R_L$, we get:

$$\frac{v_o}{v_i} = \frac{R_p}{R_p + R}$$

For $r_D \ll R_C$ and $r_D \ll R_L$, $R_p \approx r_d$ and

$$\frac{v_o}{v_i} = \frac{r_d}{r_d + R}$$
$$r_d = \frac{nV_T}{I_D} = \frac{nV_T R_C}{V_C - V_{D0}}$$

Thus, if V_C increases, it will decrease r_d and decrease v_o for a given v_i. Alternatively, reducing V_C, increases r_d and v_o.

An application of this circuit is in a speakerphone. A frequent problem is that some speakers speak quietly (or are far from the microphone) and some speak loudly (or are close). If v_i is the output of the microphone and v_o is attached to a high-gain amplifier and phone system, control voltage can compensate for changes in v_i (V_C, for example, can be the output of a peak detector circuit with v_i as the input, large v_i makes V_C larger and decreases v_o/v_i in the voltage-controlled attenuator).

4.4.2 MOS Small Signal Model

We can develop similar small-signal models for transistors. Let's first take the simpler case of a MOS. We assume that MOS is always in the saturation state. As we discussed before, each transistor has 4 independent parameters, two currents (i_G and i_D for MOS) and two voltages (v_{GS} and v_{DS} for NMOS). The iv characteristics equations gives the value of the two currents in terms of the two voltages. For NMOS, we have

$$i_G(v_{GS}, v_{DS}) = 0$$
$$i_D(v_{GS}, v_{DS}) = 0.5k'_n(W/L)_n(v_{GS} - V_{tn})^2(1 + \lambda v_{DS})$$

Let's assume MOS bias point parameters are I_D, V_{GS} and V_{DS} (note $I_G = 0$). If we apply a small signal to the transistor, MOS current and voltages are modified according to:

$$i_D = I_D + i_d \qquad v_{GS} = V_{GS} + v_{gs} \qquad v_{DS} = V_{DS} + v_{ds}$$

where i_d, v_{ds}, and v_{gs} are signal related quantities.

We will now follow a procedure similar to the diode small signal model, *i.e.,* use a Tyler series expansion. The only difference for a transistor is that i_D is a function of TWO variables. In this case, we should use Taylor series expansion around a point (X_0 and Y_0). Keeping only first order terms:

$$f(X_0 + \Delta x, Y_0 + \Delta y) \approx f(X_0, Y_0) + \Delta x \left.\frac{\partial f}{\partial x}\right|_{X_0,Y_0} + \Delta y \left.\frac{\partial f}{\partial y}\right|_{X_0,Y_0}$$

For MOS, $i_D(v_{GS}, v_{DS})$, *i.e.,* i_D is a function of v_{GS} and v_{DS} (similar to $f(x, y)$). Thus,

$$i_D(V_{GS} + v_{gs}, V_{DS} + v_{ds}) = i_D(V_{GS}, V_{DS}) + \left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q v_{gs} + \left.\frac{\partial i_D}{\partial v_{DS}}\right|_Q v_{ds}$$

Since $i_G(V_{GS} + v_{gs}, V_{DS} + v_{ds}) = I_G + i_g$ and $i_D(V_{GS} + v_{gs}, V_{DS} + v_{ds}) = I_D + i_d$, we find the signal components to be:

$$i_g = 0 \qquad \text{and} \qquad i_d = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q v_{gs} + \left.\frac{\partial i_D}{\partial v_{DS}}\right|_Q v_{ds}$$

Defining

$$g_m \equiv \left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q = 2 \times 0.5k'_n(W/L)_n(v_{GS} - V_{tn})\,(1 + \lambda v_{DS})|_Q$$
$$g_m = \frac{2}{V_{GS} - V_{tn}} \times \left[0.5k'_n(W/L)_n(V_{GS} - V_{tn})^2(1 + \lambda V_{DS})\right] = \frac{2I_D}{V_{GS} - V_{tn}}$$

and

$$\frac{1}{r_o} \equiv \left.\frac{\partial i_D}{\partial v_{DS}}\right|_Q = \lambda \times [0.5k'_n(W/L)_n]\,(v_{GS} - V_{tn})^2\Big|_Q$$

$$\frac{1}{r_o} = \frac{\lambda I_D}{1 + \lambda V_{DS}} \qquad \rightarrow \qquad r_o = \frac{V_A + V_{DS}}{I_D} \approx \frac{V_A}{I_D}$$

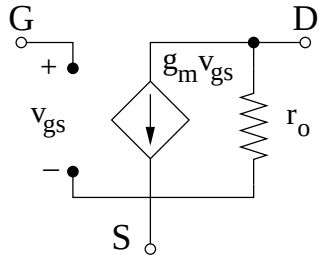
where $V_A = 1/\lambda$. Substituting g_m and r_o in the MOS small signal equations we get:

$$i_g = 0 \qquad \text{and} \qquad i_d = g_m v_{gs} + \frac{v_{ds}}{r_o}$$

It is useful to relate the above equations to circuit elements so that we can solve MOS circuits with circuit-analysis tools. The first equation $i_g = 0$ indicates that there is an "open circuit" between gate and source terminals. As $i_d = i_s$, the second equation applies between drain and source terminals. Furthermore, this equation is like a KCL: current i_d is divided into two parts. The first term, $g_m v_{gs}$, is a voltage-controlled current source (as its value does not depend on v_{ds}). The second term, v_{ds}/r_o is the Ohm's law for a resistor r_o. Thus, the small-signal model for a NMOS is:

$$g_m = \frac{2I_D}{V_{GS} - V_{tn}}$$

$$r_o = \frac{V_A + V_{DS}}{I_D} \approx \frac{V_A}{I_D}$$



Similarly, we can derive a small-signal model for a PMOS. The small-signal model for a PMOS looks exactly like an NMOS (we do NOT need to replace v_{gs} with v_{sg}) with

$$g_m = \frac{2I_D}{V_{SG} - |V_{tp}|}$$

$$r_o = \frac{V_A + V_{SD}}{I_D} \approx \frac{V_A}{I_D}$$

We will use this MOS small-signal model to analysis MOS amplifiers in the next section.

4.4.3 BJT Small Signal Model

The small-signal model for BJT can be similarly constructed. The BJT *iv* characteristics equations gives values of i_B and i_C in terms of v_{BE} and v_{CE}: For NPN transistors:

$$i_B = \frac{I_S}{\beta} e^{v_{BE}/nV_T}$$

$$i_C = I_S e^{v_{BE}/nV_T} \left(1 + \frac{v_{CE}}{V_A}\right)$$

Let's assume that BJT is biased to be in active state and the bias point parameters are I_B, I_C, V_{CE} and V_{BE}. If we apply a small signal to the BJT, transistor currents and voltages are modified according to:

$$i_B = I_B + i_b \qquad i_C = I_C + i_c \qquad v_{BE} = V_{BE} + v_{be} \qquad v_{CE} = V_{CE} + v_{ce}$$

where i_b, i_c, v_{be}, and v_{ce} are signal related quantities. The, using Taylor series expansion (note $i_B(v_{BE})$ while $i_C(v_{BE}, v_{CE})$:

$$i_B(V_{BE} + v_{be}) = i_B(V_{BE}) + \left.\frac{di_B}{dv_{BE}}\right|_Q v_{be}$$

$$i_C(V_{BE} + v_{be}, V_{CE} + v_{ce}) = i_C(V_{BE}, V_{CE}) + \left.\frac{\partial i_C}{\partial v_{BE}}\right|_Q v_{be} + \left.\frac{\partial i_C}{\partial v_{CE}}\right|_Q v_{ce}$$

Since $i_B(V_{BE}) = I_B$ and $i_B(V_{BE} + v_{be}) = I_B + i_b$, we get

$$i_b = \left.\frac{di_B}{dv_{BE}}\right|_Q v_{be} \equiv \frac{v_{be}}{r_\pi}$$

$$\frac{1}{r_\pi} \equiv \left.\frac{di_B}{dv_{BE}}\right|_Q = \frac{1}{nV_T} \times \frac{I_S}{\beta} e^{V_{BE}/nV_T} = \frac{I_B}{nV_T} \qquad \rightarrow \qquad r_\pi = \frac{nV_T}{I_B}$$

Similarly, since $i_C(V_{BE}, V_{CE}) = I_C$ and $i_C(V_{BE} + v_{be}, V_{CE} + v_{ce}) = I_C + i_c$, we get

$$i_c = \left.\frac{\partial i_C}{\partial v_{BE}}\right|_Q v_{be} + \left.\frac{\partial i_C}{\partial v_{CE}}\right|_Q v_{ce} \equiv g_m v_{be} + \frac{v_{ce}}{r_o}$$

$$g_m \equiv \left.\frac{\partial i_C}{\partial v_{BE}}\right|_Q = \frac{1}{nV_T} \times I_S e^{V_{BE}/nV_T} \left(1 + \frac{V_{CE}}{V_A}\right) = \frac{I_C}{nV_T}$$

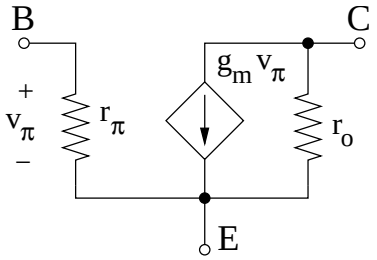
$$\frac{1}{r_o} \equiv \left.\frac{\partial i_C}{\partial v_{CE}}\right|_Q = \frac{1}{V_A} \times I_S e^{V_{BE}/nV_T} = \frac{I_C}{V_A(1 + V_{CE}/V_A)} = \frac{I_C}{V_A + V_{CE}}$$

Thus, response of BJT to small signals can be written as (setting $v_{be} = v_\pi$):

$$i_b = \frac{v_{be}}{r_\pi} \qquad \text{and} \qquad i_c = g_m v_{be} + v_{ce}/r_o$$

Similar to MOS, we relate the above equation to circuit elements to derive a small-signal circuit model for the BJT. The first equation is the statement of Ohm's law between base and emitter terminals (resistor r_π between B and E). The right equation is a KCL with a voltage-controlled current source and a resistor (similar to NMOS model).

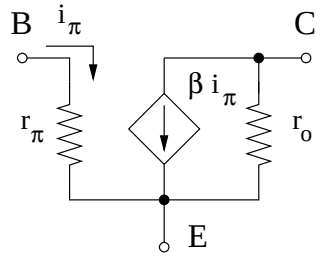
$$r_\pi = \frac{nV_T}{I_B}$$
$$g_m = \frac{I_C}{nV_T}$$
$$r_o = \frac{V_A + V_{CE}}{I_C}$$



Similarly, we can derive a small-signal model for a PNP which looks exactly like a NPN with $r_o = (V_A + V_{EC})/I_C$. Typically, $V_{CE}/V_A \ll 1$. In this case, $I_C \approx \beta I_B$ and

$$r_\pi = \frac{nV_T}{I_B}$$
$$g_m = \frac{I_C}{nV_T} = \frac{I_C}{I_B} \times \frac{I_B}{nV_T} \approx \frac{\beta}{r_\pi}$$
$$r_o = \frac{V_A(1 + V_{CE}/V_A)}{I_C} \approx \frac{V_A}{I_C}$$

(above formulas are correct for both NPN and PNP transistors). Since $g_m v_\pi = \beta(v_\pi/r_\pi) = \beta i_\pi$, an alternative model for BJT can be developed using a current-controlled current source as is shown.



We will use BJT small-signal models to analysis BJT amplifiers in the next section.

4.5 Exercise Problems

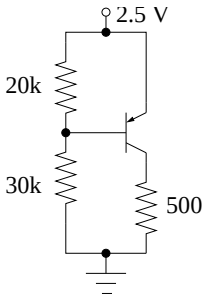
Problem 1. Find the bias point of the transistor (Si BJT with $\beta = 100$ and $V_A \to \infty$).

Problem 2. Find parameters and state of transistor of problem 1 if $\beta = 200$.

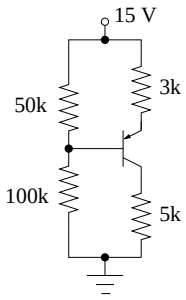
Problems 3-6. Find the bias point of the transistor (Si BJTs with $\beta = 200$ and $V_A \to \infty$).

Problems 7-8. Find the bias point of the transistor (Si BJTs with $\beta = 100$ and $V_A \to \infty$).

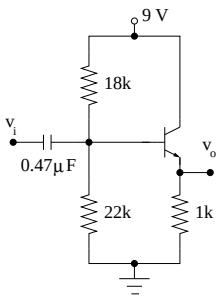
Problem 9. In the circuit below with a SI BJT ($V_A \to \infty$), we have measured $V_E = 1.2$ V. Find BJT β and V_{CE}.



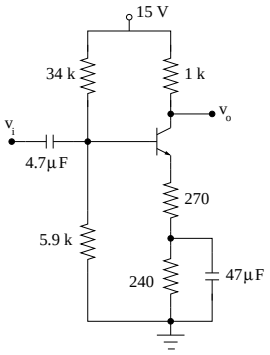
Problem 1



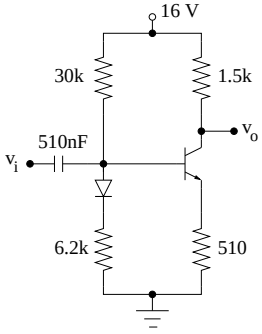
Problem 3



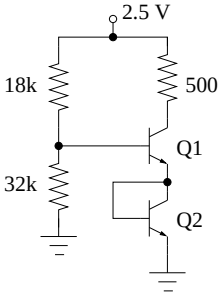
Problem 4



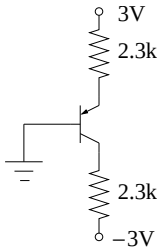
Problem 5



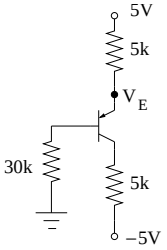
Problem 6



Problem 7



Problem 8



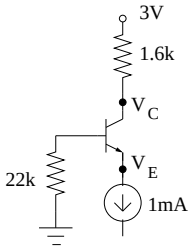
Problem 9

Problem 10. Find V_E and V_C (SI BJT with $\beta \to \infty$ and $V_A \to \infty$).

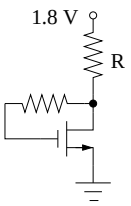
Problem 11. Find R such that $V_{DS} = 0.8$ V ($k_n'(W/L) = 1.6$ mA/V^2, $V_{tn} = 0.5$ V, and $\lambda = 0$).

Problem 12. Find the bias point of the transistor below ($k_p'(W/L) = 1$ mA/V^2, $V_{tp} = -1$ V, and $\lambda = 0$.

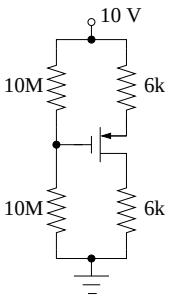
Problem 13. Find V_D and V_S ($k_n'(W/L) = 1$ mA/V^2, $V_{tn} = 2$ V, and $\lambda = 0$).



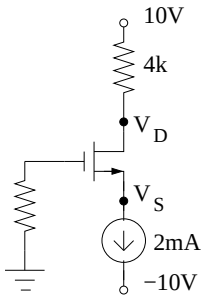
Problem 10



Problem 11



Problem 12



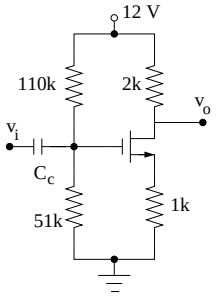
Problem 13

Problem 14. Find the bias point of the transistor ($V_{tn} = 1$ V, $k'_n(W/L) = 0.5$ mA/V^2, $\lambda = 0$, and large capacitors).

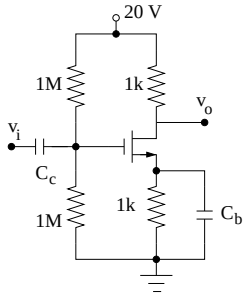
Problem 15. Find the bias point of the transistor ($V_{tn} = 3$ V, $k'_n(W/L) = 0.4$ mA/V^2, $\lambda = 0$ and large capacitors).

Problem 16. Find the bias point of the transistor ($V_{tp} = -4$ V, $k'_p(W/L) = 0.4$ mA/V^2, $\lambda = 0$ and large capacitors).

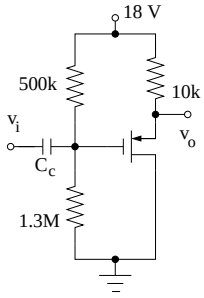
Problem 17. Find the bias point of the transistor $V_{tn} = 0.5$ V, ($k'_n(W/L) = 1.6$ mA/V^2, and $\lambda = 0$).



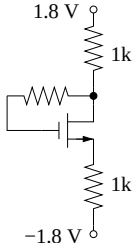
Problem 14



Problem 15

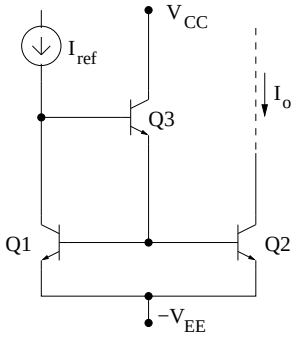


Problem 16

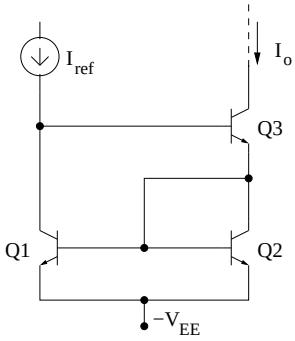


Problem 17

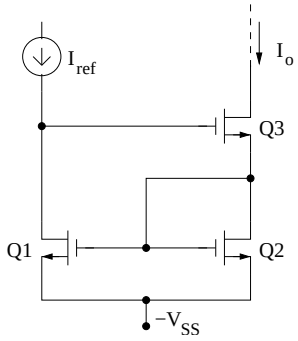
Problem 18 to 20. Compute I_o assuming identical transistors.



Problem 18



Problem 19

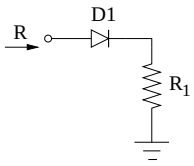


Problem 20

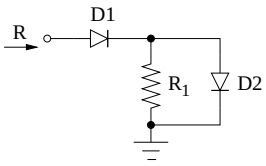
Problem 21-22. Assume that the diode is forward biased (bias circuit is NOT shown). Replace the diode with its small signal model and find the Thevenin Equivalent resistance between the indicated terminal and the ground in terms of r_d.

Problem 23-24. This configuration is called a diode-connected transistor, making the MOS into a two terminal device. A) Show that MOS will be always in saturation if $i_D > 0$, B) Replace the MOS with its small signal model and show that for small signal, the diode-connected transistor reduces to a resistor.

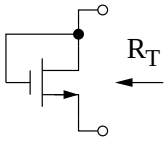
Problem 25-26. Assume that the MOS is biased and is in saturation (bias circuit is NOT shown). Replace the MOS with its small signal model (and zero out Bias voltage V_G) and find the Thevenin Equivalent resistance between the indicated terminal and the ground in terms of g_m and r_o.



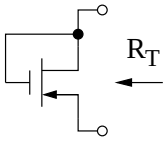
Problem 21



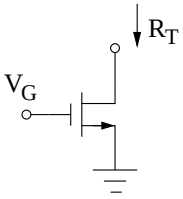
Problem 22



Problem 23



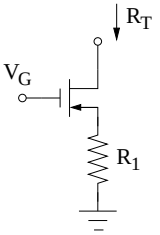
Problem 24



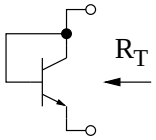
Problem 25

Problem 27-28. This is the BJT version of the diode-connected transistor, making the BJT into a two-terminal device. A) Show that BJT will be always in active if $i_C > 0$, B) Replace the BJT with its small signal model and show that for small signal, the diode-connected transistor reduces to a resistor.

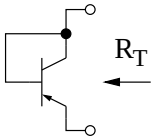
Problem 29-30. Assume that the BJT is biased and is in active (bias circuit is NOT shown). Replace the BJT with its small signal model and find the Thevenin Equivalent resistance between the indicated terminal and the ground in terms of g_m and r_o.



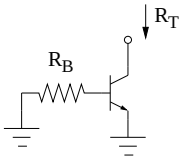
Problem 26



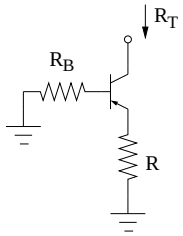
Problem 27



Problem 28



Problem 29

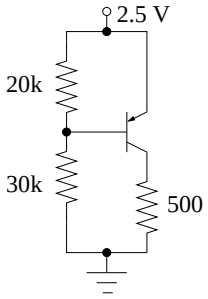


Problem 30

4.6 Solution to Selected Exercise Problems

Problem 1. Find the bias point of the transistor (Si BJT with $\beta = 100$ and $V_A \to \infty$).

This is a fixed bias scheme (because there is no R_E) with a voltage divider providing V_{BB} (It is unstable to temperature changes, see problem 2).



Assuming BJT (PNP) in the active state and replacing R2/R1 voltage divider with its Thevenin equivalent:

$$R_B = 30 \text{ k} \parallel 20 \text{ k} = 12 \text{ k}, \qquad V_{BB} = \frac{30}{30+20} \times 2.5 = 1.5 \text{ V}$$

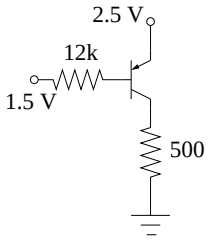
EB-KVL: $2.5 = V_{EB} + 12 \times 10^3 I_B + 1.5$

$$I_B = (2.5 - 1.5 - 0.7)/(12 \times 10^3) = 25 \ \mu\text{A}$$

$$I_C = \beta I_B = 2.5 \text{ mA}$$

EC-KVL: $2.5 = V_{EC} + 500 I_C$

$$V_{EC} = 2.5 - 500 \times 2.5 \times 10^{-3} = 1.25 \text{ V}$$

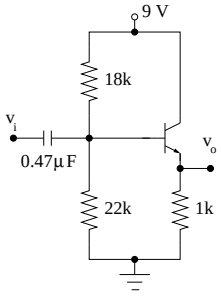


Since $V_{EC} \geq 0.7$ V and $I_C > 0$, assumption of BJT in active is justified.

Bias Summary: $V_{EC} = 1.25$ V, $I_C = 2.5$ mA, and $I_B = 25 \ \mu$A.

Problem 4. Find the bias point (Si BJT with $\beta = 200$ and $V_A \to \infty$).

Assume BJT (NPN) in active. Replace R_1/R_2 voltage divider with its Thevenin equivalent (note capacitors are open):



$$R_B = 18 \text{ k} \parallel 22 \text{ k} = 9.9 \text{ k}, \qquad V_{BB} = \frac{22}{18+22} \times 9 = 4.95 \text{ V}$$

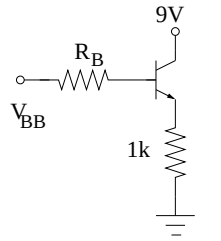
BE-KVL: $V_{BB} = R_B I_B + V_{BE} + 10^3 I_E \qquad I_B = \dfrac{I_E}{1+\beta} = \dfrac{I_E}{201}$

$$4.95 - 0.7 = I_E \left(\frac{9.9 \times 10^3}{201} + 10^3 \right)$$

$$I_E = 4 \text{ mA} \approx I_C, \qquad I_B = \frac{I_C}{\beta} = 20 \ \mu\text{A}$$

CE-KVL: $V_{CC} = V_{CE} + 10^3 I_E$

$$V_{CE} = 9 - 10^3 \times 4 \times 10^{-3} = 5 \text{ V}$$

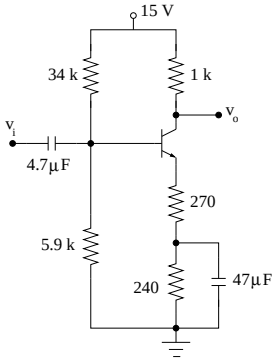


Since $V_{CE} \geq 0.7$ V and $I_C > 0$, assumption of BJT in active is justified.

Bias Summary: $V_{CE} = 5$ V, $I_C = 4$ mA, and $I_B = 20 \ \mu$A.

Problem 5. Find the bias point (Si BJT with $\beta = 200$ and $V_A \to \infty$).

Assume BJT (NPN) is in active. Replace R_1/R_2 voltage divider with its Thevenin equivalent. Since capacitors are open, the emitter resistance for bias is $270 + 240 = 510\ \Omega$.



$$R_B = 5.9\text{ k} \parallel 34\text{ k} = 5.0\text{ k}, \qquad V_{BB} = \frac{5.9}{5.9+34}\,15 = 2.22\text{ V}$$

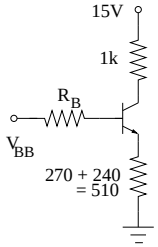
BE-KVL: $\quad V_{BB} = R_B I_B + V_{BE} + 510 I_E \qquad I_B = \dfrac{I_E}{1+\beta} = \dfrac{I_E}{201}$

$$2.22 - 0.7 = I_E\left(\frac{5.0\times 10^3}{201} + 510\right)$$

$$I_E = 3\text{ mA} \approx I_C, \qquad I_B = \frac{I_C}{\beta} = 15\ \mu\text{A}$$

CE-KVL: $\quad V_{CC} = 1000 I_C + V_{CE} + 510 I_E$

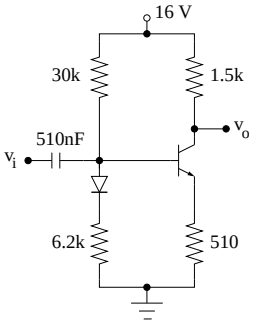
$$V_{CE} = 15 - 1{,}510 \times 3 \times 10^{-3} = 10.5\text{ V}$$

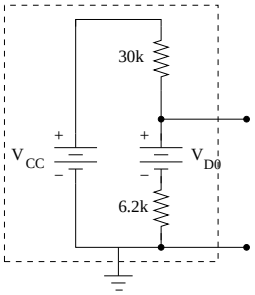


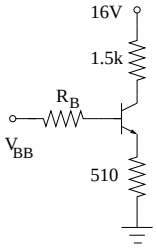
Since $V_{CE} \geq 0.7$ V and $I_C > 0$, assumption of BJT in active is justified.

Bias Summary: $V_{CE} = 10.5$ V, $I_C = 3$ mA, and $I_B = 15\ \mu$A.

Problem 6. Find the bias point (Si BJT with $\beta = 200$ and $V_A \to \infty$).







Assuming that the BJT is in the active state, the base voltage has to be large enough to forward bias the BE junction and, therefore, the diode would also be forward biased. We can find the Thevenin equivalent of the voltage divider part by noting (see circuit above:)

$$V_{BB} = V_{oc} = \frac{6.2}{30+6.2}\,(V_{CC} - V_{D0}) + V_{D0} = 2.74 + 0.83 V_{D0}\ (\text{V})$$

$$R_B = R_T = 30\text{ k} \parallel 6.2\text{ k} = 5.14\text{ k}$$

BE-KVL: $V_{BB} = R_B I_B + V_{BE} + 510 I_E$

$$2.74 + 0.83 V_{D0} = 5.14 \times 10^3 \frac{I_E}{201} + V_{D0} + 510 I_E$$

$$I_E = \frac{2.74 - 0.17 V_{D0}}{536} = 4.9 \text{ mA} \approx I_C, \qquad I_B = \frac{I_C}{\beta} = 24 \ \mu\text{A}$$

CE-KVL: $V_{CC} = 1,500 I_C + V_{CE} + 510 I_E$

$$V_{CE} = 16 - 2,010 \times 4.9 \times 10^{-3} = 6.15 \text{ V}$$

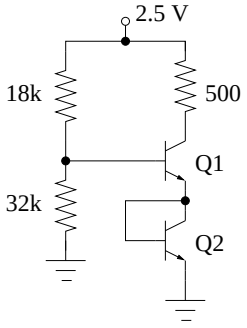
Since $V_{CE} \geq 0.7$ V and $I_C > 0$, assumption of BJT in active is justified. Note that the dependence of I_E to V_{D0} is reduced by a factor of 6 i.e., I_E now scales as $2.74 - 0.17 V_{D0}$ instead of $2.74 - V_{D0}$ (the case with no diode). As such, changes in V_{D0} due to temperature has a much smaller impact on this circuit (and $R_E I_E \geq 1$ V condition can be relaxed.)

Bias Summary: $V_{CE} = 6.15$ V, $I_C = 4.9$ mA, and $I_B = 24 \ \mu$A.

Problem 7. Find the bias point (Si BJTs with $\beta = 100$ and $V_A \to \infty$).

Assume Q1 in active. Replace R_1/R_2 voltage divider with its Thevenin equivalent:

$$R_B = 18 \text{ k} \parallel 32 \text{ k} = 11.5 \text{ k}, \qquad V_{BB} = \frac{32}{32 + 18} \times 2.5 = 1.6 \text{ V}$$



BE-KVL: $V_{BB} = R_B I_{B1} + V_{BE1} + V_{BE2}$

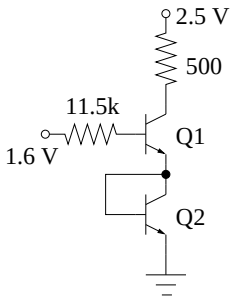
$$I_{B1} = \frac{1.6 - 1.4}{11.5 \times 10^3} = 17.4 \ \mu\text{A}$$

$$I_{C1} = \beta I_{B1} = 1.74 \text{ mA},$$

$$I_{E1} = (\beta + 1) I_{B1} = 1.76 \text{ mA}$$

CE-KVL: $2.5 = 500 I_{C1} + V_{CE1} + V_{BE2}$

$$V_{CE1} = 2.5 - 500 \times 1.74 \times 10^{-3} - 0.7 = 0.93 \text{ V}$$

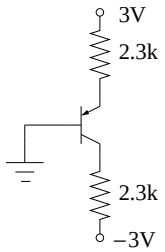


Since $V_{CE1} \geq 0.7$ V and $I_{B1} > 0$, assumption of Q1 active is justified. For Q2, we note that $V_{CE2} = V_{BE2} = 0.7$ V and $I_{E2} = I_{E1} = 1.76$ mA. So, Q2 should be in active and $I_{B2} = I_{E2}/(1 + \beta) = 17.4 \ \mu$A and $I_{C2} = 1.74$ mA.

Bias Summary: $V_{CE1} = 0.93$ V, $I_{C1} = 1.74$ mA, and $I_{B1} = 17.4 \ \mu$A.

Problem 8. Find the bias point of the transistor (Si BJT with $\beta = 100$ and $V_A \to \infty$).

Assume BJT (PNP) in active.



EB-KVL: $3 = 2.3 \times 10^3 I_E + V_{EB}$

$I_E = (3 - 0.7)/(2.3 \times 10^3) = 1$ mA

$I_B = I_E/(\beta + 1) = 10$ μA

$I_C = \beta I_B = 0.99$ mA

EC-KVL: $3 = 2.3 \times 10^3 I_E + V_{EC} + 2.3 \times 10^3 I_C - 3$

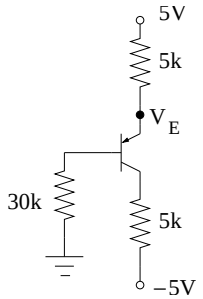
$V_{EC} = 2.4$ V

Since $V_{EC} \geq 0.7$ V and $I_C > 0$, assumption of BJT in active is justified.

Bias Summary: $V_{EC} = 2.4$ V, $I_C = 1$ mA, and $I_B = 10$ μA.

Problem 9. In the circuit below with a SI BJT ($V_A \to \infty$), we have measured $V_E = 1.2$ V. Find BJT β and V_{CE}.

Assume BJT (PNP) in active:



Ohm Law: $5 \times 10^3 I_E = 5 - V_E = 3.8 \quad \to \quad I_E = 0.76$ mA

EB-KVL: $V_E = V_{EB} + 30 \times 10^3 I_B$

$I_B = (1.2 - 0.7)/(30 \times 10^3) = 16.7$ μA

$I_C = I_E - I_B = 0.74$ mA

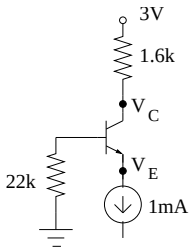
$$\beta = \frac{I_C}{I_B} = \frac{0.74 \times 10^{-3}}{16.7 \times 10^{-6}} \approx 47$$

EC-KVL: $V_E = V_{EC} + 5 \times 10^3 I_C - 5$

$1.2 = V_{EC} + 5 \times 10^3 \times 0.74 \times 10^{-3} - 5 \quad \to \quad V_{EC} = 2.4$ V

Since $V_{EC} \geq 0.7$ V and $I_C > 0$, assumption of BJT in active is justified.

Problem 10. Find V_E and V_C (SI BJT with $\beta \to \infty$ and $V_A \to \infty$).



Assume Q1 in active. Since $\beta \to \infty$, then $I_B \to 0$ (this does not mean that BJT is in cut-off, rather I_B is so small that it can be ignored in calculations).:

$$I_E = 1 \text{ mA} \qquad I_C = I_E - I_B = 1 \text{ mA}$$

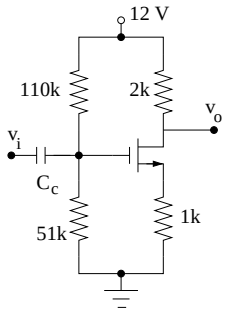
$$\text{BE-KVL} \quad 0 = 22 \times 10^3 I_B + V_{BE} + V_E \quad \to \quad V_E = -0.7 \text{ V}$$

$$\text{KVL} \quad 3 = 1.6 \times 10^3 I_C + V_C \quad \to \quad V_C = 1.4 \text{ V}$$

and $V_{CE} = V_C - V_E = 1.4 - (-0.7) = 2.1$ V. Since $V_{CE} > 0.7$ V and $I_E > 0$, assumption of BJT in active is justified.

Bias Summary: $I_C = 1$ mA and $V_{CE} = 2.1$ V.

Problem 14. Find the bias point of the transistor ($V_{tn} = 1$ V, $k'_n(W/L) = 0.5$ mA/V^2, $\lambda = 0$, and large capacitors).



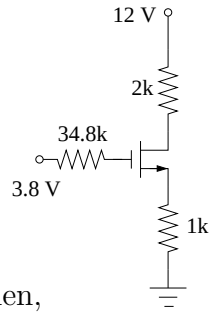
Replacing R_1/R_2 voltage divider with its Thevenin equivalent, we get:

$$R_G = 51 \text{ k} \parallel 110 \text{ k} = 34.8 \text{ k}, \qquad V_{GG} = \frac{51}{51+110} \times 12 = 3.80 \text{ V}$$

Assume NMOS is in the active state,

$$I_D = 0.5 k'_n (W/L)(V_{GS} - V_{tn})^2 = 0.5 \times 0.5 \times 10^{-3}(V_{GS} - 1)^2$$

$$\text{GS-KVL:} \quad 3.8 = 34.8 \times 10^3 I_G + V_{GS} + 1{,}000 I_D = V_{GS} + 1{,}000 I_D$$



Substituting for I_D in GS-KVL, we get:

$$3.8 = V_{GS} + 0.25(V_{GS} - 1)^2 \quad \to \quad 0.25 V_{GS}^2 + 0.5 V_{GS} - 3.55 = 0$$

Two roots: 2.9 and -4.9. As the negative root is unphysical, $V_{GS} = 2.9$. Then,

$$\text{GS-KVL:} \quad 3.8 = V_{GS} + 1{,}000 I_D \quad \to \quad I_D = 0.9 \text{ mA}$$

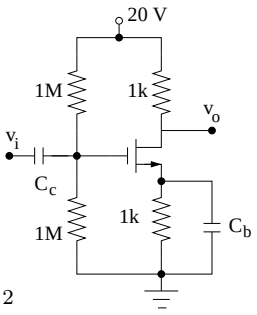
$$\text{DS-KVL:} \quad 12 = 2{,}000 I_D + V_{DS} + 1{,}000 I_D = V_{DS} + 2.7 \quad \to \quad V_{DS} = 9.3 \text{ V}$$

As $V_{DS} = 9.3 > V_{GS} - V_{tn} = 2.9 - 1 = 1.95$, our assumption of NMOS in active is correct.

Bias Summary: $V_{GS} = 2.9$ V, $V_{DS} = 9.3$ V, and $I_D = 0.9$ mA.

Problem 15. Find the bias point of the transistor ($V_{tn} = 3$ V, $k'_n(W/L) = 0.4$ mA/V^2, $\lambda = 0$ and large capacitors).

Replacing R_1/R_2 voltage divider with its Thevenin equivalent, we get:

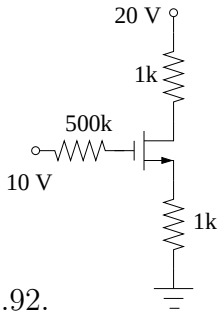


$$R_G = 1 \text{ M} \parallel 1 \text{ M} = 500 \text{ k}, \qquad V_{GG} = \frac{1}{1+1} \times 20 = 10 \text{ V}$$

Assume NMOS is in the active state,

$$I_D = 0.5k'_n(W/L)(V_{GS} - V_{tn})^2 = 0.5 \times 0.4 \times 10^{-3}(V_{GS} - 3)^2$$

GS-KVL: $\quad 10 = V_{GS} + 10^3 I_D$



Substituting for I_D in GS-KVL, we get:

$$10 = V_{GS} + 0.2(V_{GS} - 3)^2 \quad \rightarrow \quad V_{GS}^2 - V_{GS} - 41 = 0$$

Two roots: 6.92 and -5.92. As the negative root is unphysical, $V_{GS} = 6.92$.

GS-KVL: $\quad 10 = 6.92 + 10^3 I_D \quad \rightarrow \quad I_D = 3.08$ mA

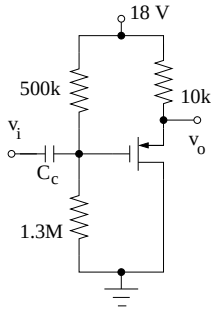
DS-KVL: $\quad 20 = 10^3 I_D + V_{DS} + 10^3 I_D \quad \rightarrow \quad V_{DS} = 20 - 2 \times 10^3 \times 3.08 \times 10^{-3} = 13.8$ V

Since $V_{DS} = 13.8 \geq V_{GS} - V_{tn} = 6.92 - 3 = 3.92$ V, our assumption of NMOS in active state is justified.

Bias summary: $V_{GS} = 6.92$ V, $V_{DS} = 13.8$ V, and $I_D = 3.08$ mA

Problem 16. Find the bias point of the transistor ($k_p'(W/L) = 0.4$ mA/V^2, $V_{tp} = -4$ V, and $\lambda = 0$ and large capacitors).

Replacing R_1/R_2 voltage divider with its Thevenin equivalent, we get:

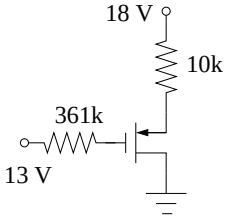


$$R_G = 1.3 \text{ M} \parallel 500 \text{ k} = 361 \text{ k}, \qquad V_{GG} = \frac{1.3}{1.3 + 0.5} \times 18 = 13 \text{ V}$$

Assume PMOS is in the active state,

$$I_D = 0.5k_n'(W/L)(V_{SG} - |V_{tp}|)^2 = 0.5 \times 0.4 \times 10^{-3}(V_{GS} - 4)^2$$

SG-KVL: $\quad 13 = V_{SG} + 10^4 I_D$



Substituting for I_D in SG-KVL, we get:

$$13 = V_{SG} + 2(V_{SG} - 4)^2 \quad \rightarrow \quad 2V_{SG}^2 - 15V_{SG} + 19 = 0$$

Two roots: -5.9 and -1.6. Since $V_{SG} = 1.6 < |V_{tp}| = 4$ V required for NMOS to be ON, this root is unphysical. So, $V_{SG} = 5.9$ V.

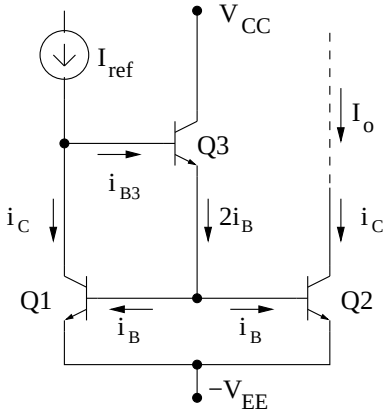
SG-KVL: $\quad 13 = V_{SG} + 10^4 I_D = 5.9 + 10^4 I_D \quad \rightarrow \quad I_D = 0.71$ mA

SD-KVL: $\quad 18 = V_{SD} + 10^4 I_D \quad \rightarrow \quad V_{SD} = 18 - 10^4 \times 0.71 \times 10^{-3} = 10.9$ V

Since $V_{SD} = 10.9 \geq V_{SG} - |V_{tp}| = 5.9 - 4 = 1.9$ V, our assumption of PMOS in active is justified.

Bias summary: $V_{SG} = 5.9$ V, $V_{SD} = 10.9$ V, and $I_D = 0.71$ mA

Problem 18. Compute I_o assuming identical transistors.



Because both bases and emitters of the transistors Q1 and Q2 are connected together, KVL leads to $v_{BE1} = v_{BE2}$. As BJT's are identical, they should have similar i_B ($i_{B1} = i_{B2} = i_B$) and, therefore, similar $i_E = i_{E1} = i_{E2}$ and $i_C = i_{C1} = i_{C2}$. Using $i_C = \beta i_B$ and $i_E = (\beta + 1)i_B$ to illustrate the impact of β:

$$i_B = \frac{i_E}{\beta + 1} \qquad I_o = i_C = \frac{\beta i_E}{\beta + 1}$$

KCL: $$i_{E3} = 2i_B = \frac{2i_E}{\beta + 1}$$

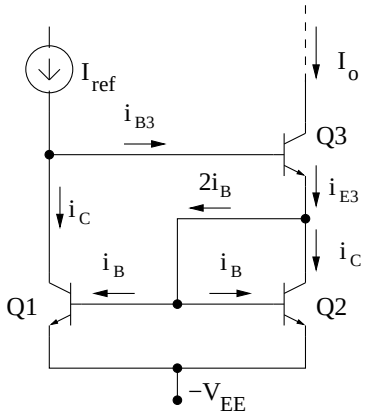
$$i_{B3} = \frac{i_{E3}}{\beta + 1} = \frac{2i_E}{(\beta + 1)^2}$$

KCL: $$I_{ref} = i_C + i_{B3} = \frac{\beta i_E}{\beta + 1} + \frac{2i_E}{(\beta + 1)^2}$$

$$\frac{I_o}{I_{ref}} = \frac{\beta}{\beta + 2/(\beta + 1)} = \frac{1}{1 + 2/\beta(\beta + 1)} \approx \frac{1}{1 + 2/\beta^2}$$

As can be seen, this is a better current mirror than our simple version as $I_o \approx I_{ref}$ with an accuracy of $2/\beta^2$. Similar to our simple current-mirror circuit, I_{ref} can be set by using a resistor R_c.

Problem 19. Compute I_o assuming identical transistors.



Because both bases and emitters of the transistors Q1 and Q2 are connected together, KVL leads to $v_{BE1} = v_{BE2}$. As BJT's are identical, they should have similar i_B ($i_{B1} = i_{B2} = i_B$) and, therefore, similar $i_E = i_{E1} = i_{E2}$ and $i_C = i_{C1} = i_{C2}$. Using $i_C = \beta i_B$ and $i_E = (\beta + 1)i_B$ to illustrate the impact of β:

$$i_B = \frac{i_E}{\beta + 1}$$

KCL: $$i_{E3} = 2i_B + i_c = \frac{2i_E}{\beta + 1} + \frac{\beta i_E}{\beta + 1} = \frac{\beta + 2}{\beta + 1}\, i_E$$

$$i_{B3} = \frac{i_{E3}}{\beta + 1} = \frac{\beta + 2}{(\beta + 1)^2}\, i_E$$

KCL: $$I_{ref} = i_C + i_{B3} = \frac{\beta i_E}{\beta + 1} + \frac{\beta + 2}{(\beta + 1)^2}\, i_E = \frac{\beta(\beta + 1) + \beta + 2}{(\beta + 1)^2}\, i_E$$

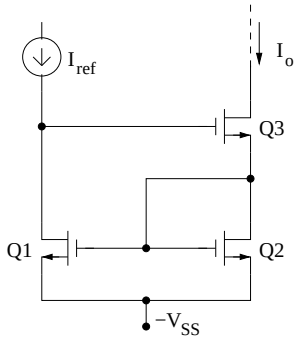
$$I_o = i_{C3} = \frac{\beta}{\beta + 1}\, i_{E3} = \frac{\beta(\beta + 2)}{(\beta + 1)^2}\, i_E$$

$$\frac{I_o}{I_{ref}} = \frac{\beta(\beta + 2)}{\beta(\beta + 1) + \beta + 2} = \frac{\beta(\beta + 2)}{\beta(\beta + 2) + 2} == \frac{1}{1 + \dfrac{2}{\beta(\beta + 2)}} \approx \frac{1}{1 + 2/\beta^2}$$

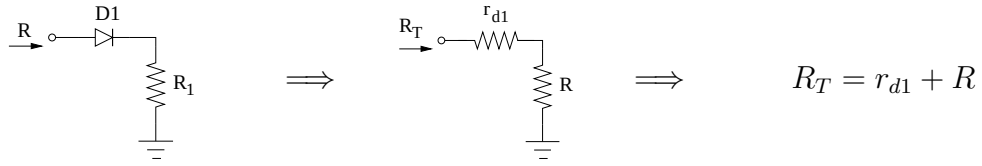
This circuit is called the Wilson current mirror after its inventor. It has a reduced β dependence compared to our simple current mirror and has a greater output impedance compared to the current mirror of problem 2.

Problem 20. Compute I_o assuming identical transistors.

This is the MOS version of the Wilson current mirror. Solution is similar to those of Problems 18 and 19. The advantage of this current mirror over the simple current mirror of Problem 18 is its much larger output resistance.

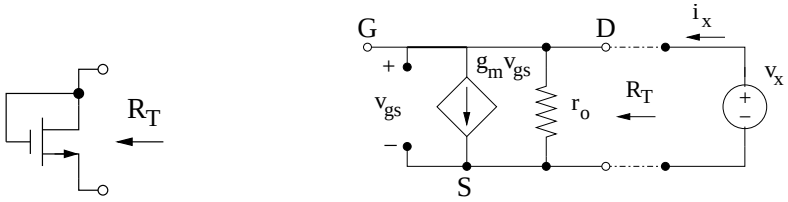


Problem 21. Assume that the diode is forward biased (bias circuit is NOT shown). Replace the diode with its small signal model and find the Thevenin Equivalent resistance between the indicated terminal and the ground in terms of r_d.



$$\Longrightarrow \qquad \Longrightarrow \qquad R_T = r_{d1} + R$$

Problem 23. This configuration is called a diode-connected transistor, making the MOS into a two terminal device. A) Show that MOS will be always in saturation if $i_D > 0$, B) Replace the MOS with its small signal model and show that for small signal, the diode-connected transistor reduces to a resistor.



A) Since $v_{DS} = v_{GS} > v_{GS} - V_{tn}$, NMOS will be in saturation if $i_D > 0$.

B) The figure to the right above is the small-signal equivalent of the diode-connected NMOS. Calculation of R_T is not straight-forward because of the controlled current source. We need to attach a voltages source v_x to the circuit, calculate i_x with $R_T i_x = v_x$.

From the circuit $v_{gs} = v_x$, noting $i_x = (1/R_T)v_x$,

$$\text{KCL at D:} \qquad i_x = \frac{v_x}{r_o} + g_m v_{gs} = v_x \left(\frac{1}{r_o} + g_m \right)$$

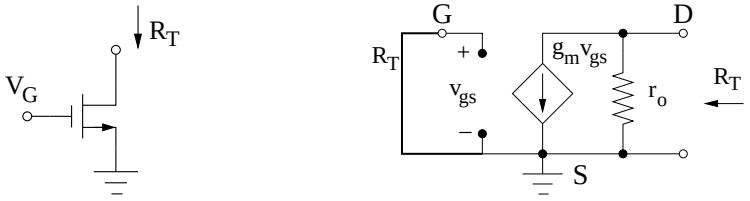
$$\frac{1}{R_T} = \frac{1}{r_o} + \frac{1}{1/g_m} \quad \rightarrow \quad R_T = r_o \parallel (1/g_m)$$

Problem 24. This configuration is called a diode-connected transistor, making the MOS in to a two terminal device. A) Show that MOS will be always in saturation if $i_D > 0$, B) Replace the MOS with its small signal model and show that for small signal, the diode-connected transistor reduces to a resistor.

A) Since $v_{SD} = v_{SG} > v_{SG} - |V_{tp}|$, PMOS will be in saturation if $i_D > 0$.

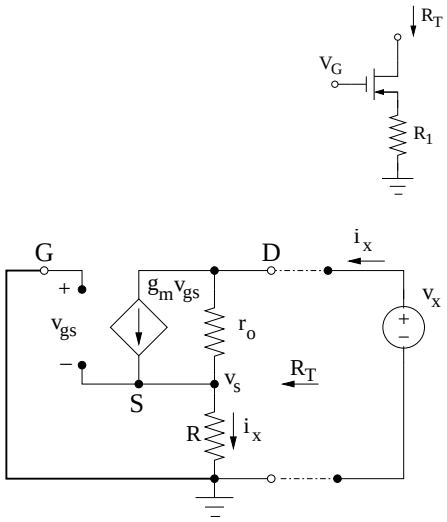
B) Since the small signal model of PMOS and NMOS are identical, result of problem 23 applies here, *i.e.,* $R_T = r_o \parallel (1/g_m)$.

Problem 25. Assume that the MOS is biased and is in saturation (bias circuit is NOT shown). Replace the MOS with its small signal model (and zero out Bias voltage V_G) and find the Thevenin Equivalent resistance between the indicated terminal and the ground in terms of g_m and r_o.



The figure to the right above is the small-signal equivalent of the circuit. Note that since bias voltage V_G is "zeroed," the gate is now connected to the ground making $v_{gs} = 0$. In this case, the controlled current source becomes an open circuit and $R_T = r_o$.

Problem 26. Assume that the MOS is biased and is in saturation (bias circuit is NOT shown). Replace the MOS with its small signal model (and zero out Bias voltage V_G) and find the Thevenin Equivalent resistance between the indicated terminal and the ground in terms of g_m and r_o.



The figure below is the small-signal equivalent of the circuit. Note that since bias voltage V_G is "zeroed," the gate is now connected to the ground (note $v_{gs} \neq 0$). Because of the controlled current source, we need to attach a voltages source v_x to the circuit, calculate i_x with $R_T i_x = v_x$. Note that by KCL, current i_x has to flow in the resistor R:

Ohm Law: $v_s = i_x R$

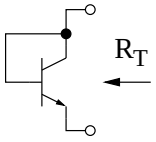
$$v_{gs} = v_g - v_s = -Ri_x$$

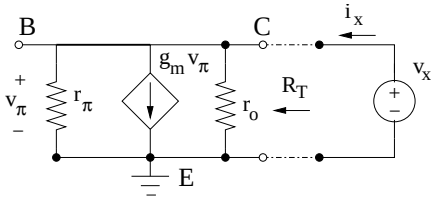
KCL at D: $$i_x = \frac{v_x - v_s}{r_o} + g_m v_g s$$

$$i_x r_o = v_x - (i_x R) + r_o g_m (-Ri_x)$$

$$i_x(r_o + R + g_m r_o R) = v_x \quad \rightarrow \quad R_T = r_o + R + g_m r_o R$$

Problem 27. This is the BJT version of the diode-connected transistor, making the BJT into a two-terminal device. A) Show that BJT will be always in active if $i_C > 0$, B) Replace the BJT with its small signal model and show that for small signal, the diode-connected transistor reduces to a resistor.





A) Since $v_{CE} = v_{BE} = V_{D0}$, BJT will be in active if $i_C > 0$.

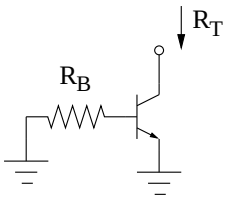
B) The figure to the right above is the small-signal equivalent of the diode-connected BJT. Because of the controlled current source, we need to attach a voltages source v_x to the circuit, calculate i_x with $R_T i_x = v_x$.

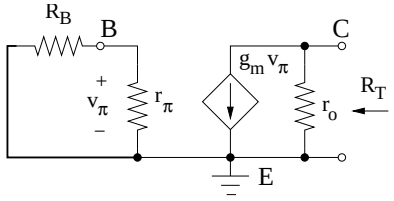
From the circuit $v_\pi = v_x$, noting $i_x = (1/R_T)v_x$,

$$\text{KCL:} \quad i_x = \frac{v_x}{r_o} + g_m v_\pi + \frac{v_x}{r_\pi} = v_x\left(\frac{1}{r_o} + g_m + \frac{1}{r_\pi}\right)$$

$$\frac{1}{R_T} = \frac{1}{r_o} + \frac{1}{1/g_m} + \frac{1}{r_\pi} \quad \rightarrow \quad R_T = r_o \parallel r_\pi \parallel (1/g_m)$$

Problem 29. Assume that the BJT is biased and is in active (bias circuit is NOT shown). Replace the BJT with its small signal model and find the Thevenin Equivalent resistance between the indicated terminal and the ground in terms of g_m and r_o.





The figure to the right above is the small-signal equivalent of the circuit. Because there is no sources in the left hand part of the circuit, $v_\pi = 0$. In this case, the controlled current source becomes an open circuit and $R_T = r_o$.