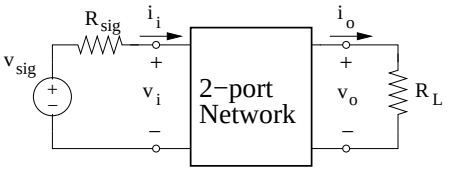
V. Transistor Amplifiers

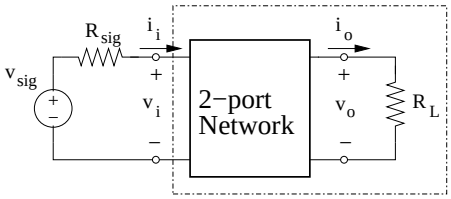
5.1 Introduction

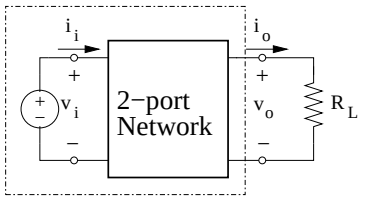
In page 1-11, we showed that the response of a two-port networks in a system is completely determined if we solve the simple circuit shown. Furthermore, one can show that if a two-port network contains only linear elements, the two-port network can be modeled with a maximum of four circuit elements.



For practical circuit in which the two-port network does not contain any independent sources, the two-port network can be modeled with 3 elements: the input resistance, the output resistance, and the voltage transfer function as is shown below:

As the combination of the two-port network and the load (dashed box in the circuit) is a two-terminal network, it can be modeled by its Thevenin equivalent. Furthermore, as this "box" does not contain an independent source, $V_T = 0$. As such, the "box" can be modeled as a resistor, called the input resistance of the two-port network:





$$\text{Input Resistance:} \qquad R_i = \frac{v_i}{i_i}$$

Note that in general R_i depends on R_L.

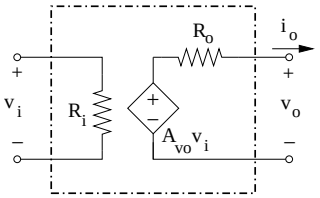
To find a model for the output port of a two-port network, we assume a voltage v_i is directly applied to the two-port network (*i.e.*, $v_{sig} = v_i$ and $R_{sig} = 0$). In this manner, the output port model will be independent of R_{sig}. Again, as the box containing v_i and the two-port network is a two-terminal network, it can be modeled with its Thevenin equivalent (see Figure). We call the Thevenin resistance of this "box," the output resistance of the two-port network:

$$\text{Output Resistance:} \qquad R_o = -\left.\frac{v_o}{i_o}\right|_{v_i=0} \qquad \text{(Thevenin Resistance)}$$

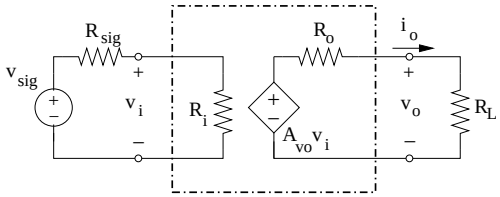
The Thevenin voltage source, $V_T = v_{oc}$ the open-loop voltage value. For an amplifier, the output voltage should be proportional to v_i. Therefore, if we define

$$\text{Open-loop Gain:} \qquad A_{vo} = \frac{v_{oc}}{v_i} = \left.\frac{v_o}{v_i}\right|_{R_L\to\infty}$$

Then, $V_T = v_{oc} = A_{vo} v_i$, *i.e.,* the Thevenin voltage can be modeled by a controlled voltage source. Combining the models for the input and output ports, we arrive at the model for an amplifier which consists of three circuit elements as is shown below (left).



Voltage Amplifier Model



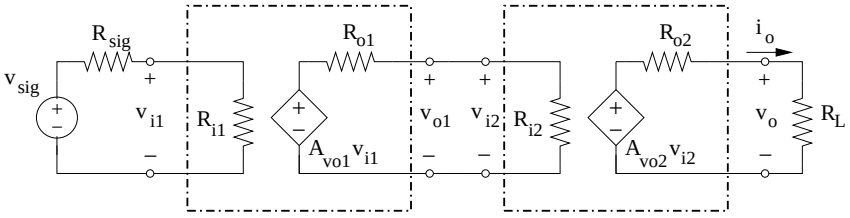
The amplifier circuit model allows us to solve any amplifier configuration once to compute the three parameters: A_{vo}, R_i and R_o. We can then find the response of any circuit containing this amplifier by utilizing these three parameters (similar to using Thevenin Theorem to "label" any two-terminal network with R_T and V_T). For example, for the generic two-port network circuit (circuit right above), we can find the response of the amplifier to the presence of R_{sig} and Load:

$$A_v = \frac{v_o}{v_i} = \frac{R_L}{R_o + R_L} A_{vo} \qquad \frac{v_i}{v_{sig}} = \frac{R_i}{R_i + R_{sig}}$$

$$\frac{v_o}{v_{sig}} = \frac{v_i}{v_{sig}} \times \frac{v_o}{v_i} = \frac{R_i}{R_i + R_{sig}} \times A_v = \frac{R_i}{R_i + R_{sig}} \times A_{vo} \times \frac{R_L}{R_o + R_L}$$

We see that the open-loop gain A_{vo} is the maximum value for the amplifier gain A_v. In addition, to maximize v_o/v_{sig}, we need $R_i \to \infty$ and $R_o \to 0$. A practical voltage amplifier, thus, is designed to have a "large" R_i and a "small" R_o (*i.e.,* $R_i \gg R_{sig}$ and $R_o \ll R_L$). A voltage-controlled voltage source is an ideal voltage amplifier as $R_i \to \infty$ and $R_o = 0$.

Similarly, for a two-stage amplifier:



$$\frac{v_o}{v_{sig}} = \frac{R_{i1}}{R_{i1} + R_{sig}} \times A_{vo1} \times \frac{R_{i2}}{R_{i2} + R_{o1}} \times A_{vo2} \times \frac{R_L}{R_{o2} + R_L}$$

Note that the input resistance of the second amplifier, R_{i2}, is the "load" for the first amplifier and the output resistance of the first amplifier, R_{o1} is R_{sig} for the second one.

We see that in order to maximize the voltage gain, we need to ensure that the input resistance of the first stage is much larger than R_{sig}, the output resistance of the last stage is much smaller than R_L, and the input resistance of any stage to be much larger than the output resistance of the previous stage: $R_{i,N} \gg R_{o,N-1}$ as R_i of the "N"th stage appears as the load for "N-1"th stage.

For single-transistor amplifier configurations (rest of this section), we will see that is simpler to compute A_v (with load present) directly instead of A_{vo} and R_o separately. In this case, the above formula for computing total gain of a two-stage amplifier can be simplified to

$$\frac{v_o}{v_{sig}} = \frac{R_{i1}}{R_{i1} + R_{sig}} \times A_{v1}(R_L = R_{i2}) \times A_{v2}(R_L = R_L)$$

where $A_{v1}(R_L = R_{i2})$ is the voltage gain with R_{i2} being the load, *etc.*

An important caution: In general, A_{vo} and R_o are independent of both R_{sig} and R_L (why?). However, R_i may depend on R_L. Amplifier configurations in which R_i is independent of R_L are called unilateral. It is easy, however, to incorporate the dependence of R_i on R_L by solving any multi-stage amplifier from the load side toward the signal side: In the above figure, we know the final load R_L which can be used to compute R_{i2} and R_{i2} is the "load" for stage one and gives R_{i1}.

Analysis of Transistor Amplifier Circuits

Analysis of a transistor amplifier circuit follows these three steps as we need to address several issues: bias, linear response (to small signals) and the impact of coupling capacitors.

Bias: Zero out the signal and replace capacitors with open circuits. Analyze the circuit using a large-signal model such as those of page 3-4 or 3-6 for BJT and 3-22/3-23 for MOS.

Small Signal Response:
1) Compute g_m, r_o (and r_π for BJT) from bias point parameters
2) Zero out all bias sources
3) Assume capacitors are short circuit.
4) Replace the transistor with its small signal model.
5) Inspect the circuit. If you identify the circuit as a prototype circuit, you can directly use the formulas for that circuit. Otherwise solve for A_v, A_{vo}, R_i and R_o .

Frequency-response: Value of A_v found in the small signal response above is called the mid-frequency gain of the amplifier. Coupling and bypass capacitors as well as the internal capacitance of transistors introduce poles both at low and high frequencies. We will introduce a method to compute the low-frequency poles. ECE102 include a more thorough review of the amplifier frequency response.

There are four fundamental single transistor amplifier configurations possible and are examined in the following sections.

Notes:

1) The small-signal models of PNP and NPN transistors (or PMOS and NMOS transistors) are similar. Thus, the formulas derived below can be used for either case.

2) The small-signal model of a BJT is similar to that of a MOS with the exception of the additional resistor r_π (the input ports in a MOS is open circuit circuit). As such, we expect that formulas for MOS amplifiers would be the same as those of BJT amplifier if we set $r_\pi \to \infty$.

3) For MOS circuits, we use the common approximation $g_m r_o \gg 1$ as

$$g_m = \frac{2I_D}{V_{GS} - V_{tn}}, \qquad r_o \approx \frac{V_A}{I_D} \quad \to \quad g_m r_o = \frac{2V_A}{V_{GS} - V_{tn}} \gg 1$$

typically $g_m r_o$ is 50 or more.

4) For BJT circuits, we use the common approximation $g_m r_o \gg 1$ as

$$g_m = \frac{I_C}{nV_T}, \qquad r_o = \frac{V_A + V_{CE}}{I_C} \approx \frac{V_A}{I_C} \quad \to \quad g_m r_o = \frac{V_A + V_{CE}}{nV_t} \gg 1$$

typically $g_m r_o$ is several thousands. In addition, $g_m r_\pi = \beta \gg 1$

5) In many text books (*e.g.,* Sedra & Smith), the formulas for BJT amplifiers are given in terms of β & r_e (instead of g_m & r_π) where

$$r_e = \frac{1}{g_m} = \frac{r_\pi}{\beta}$$

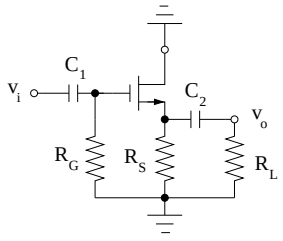
with r_e typically in 10s or 100 Ω range. Here we keep both g_m form (so we can see the comparison to MOS amplifiers) and also derive the formula in r_e form.

6) Some manufacturer spec sheet for BJTs (*e.g.,* spec sheet for 3N3904) use the older notation (hybrid π model) for BJT which are $h_{fe} \equiv \beta$, $h_{re} \equiv r_\pi$, and $h_{oe} \equiv 1/r_o$

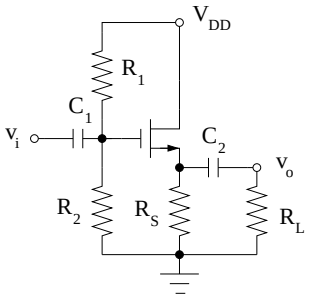
5.2 Common-Drain and Common-Collector Amplifiers

Common-Drain or Source Follower Configuration

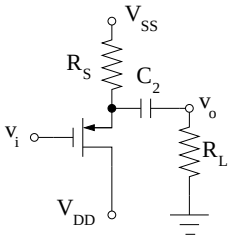
Circuit shown is the generic "small-signal" circuit of a common-drain amplifier (*i.e.,* we have "zeroed" out all Bias sources). Note that the input is applied at the gate and the output is taken at the source. As the drain is grounded (for small signal), it is the common terminal of input and output. Thus, this circuit is called the common-drain amplifier.



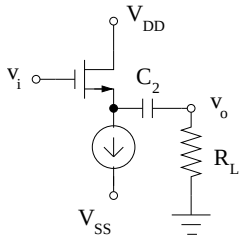
It is important to realize that as a transistor can be biased in many ways, several "complete" circuits (*i.e.,* including the bias elements) will reduce to the above "small-signal" form of a common-drain amplifier. Some examples are given below.



$R_G = R_1 \parallel R_2$

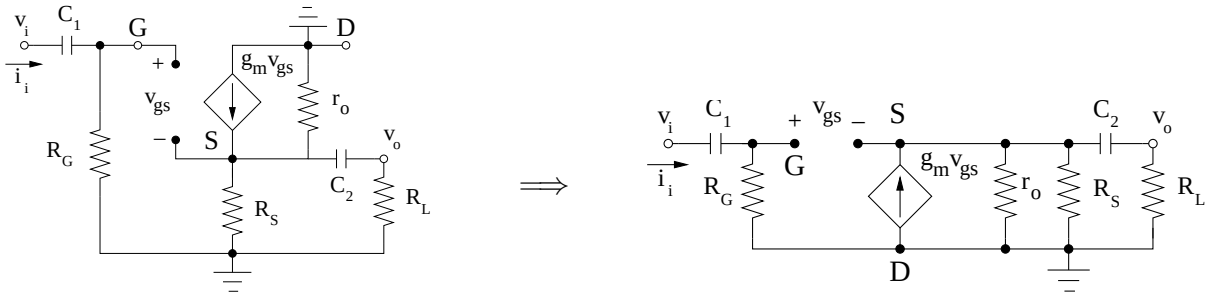


$R_G \to \infty$,
no Pole from C1



$R_G \to \infty$, $R_S \to \infty$,
no Pole from C1

We now proceed with the small-signal analysis by replacing the MOS with its small-signal model. An important observation is that the resistor R_S is parallel to R_L and appears as the load for the transistor. In fact, in many applications, R_S is replaced by the load (*e.g.* a speaker, input of another amplifier circuit). As such, we define $R'_L = R_S \parallel R_L$. The open-loop gain of the amplifier is calculated with $R'_L \to \infty$ (both R_S and R_L are open circuit) and the output resistance is taken to the left of R_S (see page 5-6)



We compute, A_v (in the presence of a load) directly as this does not complicate the analysis. The open-loop gain is then calculated by setting $R'_L \to \infty$. Inspecting the circuit, we find

that the current $g_m v_{gs}$ will flow in $r_o \parallel R'_L$ (from v_o to the ground). Thus,

$$v_{gs} = v_i - v_o$$

Ohm Law: $$v_o = g_m v_{gs}(r_o \parallel R'_L) = g_m(r_o \parallel R'_L)(v_i - v_o)$$

$$A_v = \frac{v_o}{v_i} = \frac{g_m(r_o \parallel R'_L)}{1 + g_m(r_o \parallel R'_L)} = \frac{g_m r_o R'_L}{r_o + R'_L + g_m r_o R'_L} \approx \frac{g_m R'_L}{1 + g_m R'_L}$$

where we have used $g_m r_o \gg 1$ to drop R'_L compared to $g_m r_o R'_L$ in the denominator.

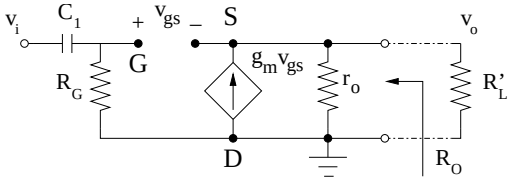
The open-loop gain can be find by setting $R'_L \to \infty$ to get $r_o \parallel R'_L = r_o$ and

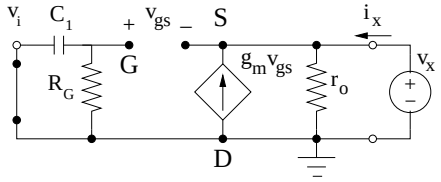
$$A_{vo} = \frac{g_m r_o}{1 + g_m r_o} \approx 1$$

Because $A_{vo} \approx 1$, $v_o = v_S \approx v_G = v_i$ and v_S "follows" the input voltage. Thus, this configuration is also called the Source Follower.

Finding R_i is easy as $v_i = R_G\, i_i$ (see circuit) and, therefore, $R_i = R_G$. As R_i is independent of R_L, this configuration is unilateral. Note that if R_G were not present (see example complete circuit of page 5-5), $R_i \to \infty$.

To find R_o we need to zero out v_i and compute the Thevenin Equivalent resistance seen at the output terminals. Because of the presence of the controlled source, we need to attach a v_x voltage source to the circuit and compute i_x:





$$v_{gs} = v_i - v_x = -v_x$$

KCL: $$i_x = -g_m v_{gs} + \frac{v_x}{r_o} = v_x \frac{g_m r_o + 1}{r_o}$$

$$R_o = \frac{r_o}{1 + g_m r_o} \approx \frac{1}{g_m}$$

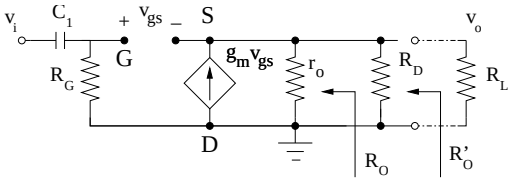
R_o is typically small, a few 100 Ω. Note that:

$$A_v = A_{vo} \times \frac{R_L}{R_L + R_o} = 1 \times \frac{R'_L}{R'_L + 1/g_m} = \frac{g_m R'_L}{1 + g_m R'_L}$$

which is exactly the expression we had derived before.

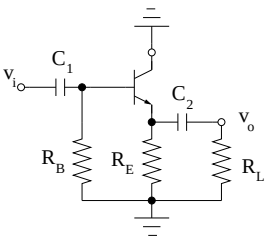
In summary, the general properties of the common-drain amplifier (source follower) include an open-loop voltage gain of unity, a large input resistance (and can be made infinite in some biasing schemes) and a small output resistance. This type of circuit is typically called a buffer and often used when there is a mismatch between input resistance of one stage and the output resistance of the previous stage. Additionally, $i_L = i_o \gg i_i$ as $A_{vo} = 1$ but $R_i \gg R_o$. As such, this circuit can be used to amplify the signal current (and power) and drive a load (used typically as the last stage of an amplifier circuit)

Note re R_o: In some text books (*e.g.,* Sedra & Smith), the output resistance is defined to include R_D (see circuit). If we call this resistance to be R'_o, inspection of the circuit shows that $R'_o = R_D \parallel R_o$.

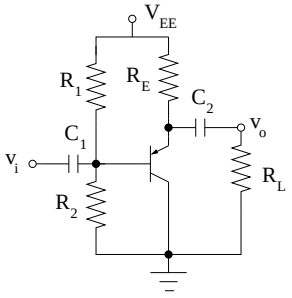


Common-Collector or Emitter Follower Configuration

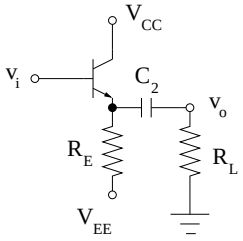
Circuit shown is the generic "small-signal" circuit of a common-collector amplifier (*i.e.,* we have "zeroed" out all Bias sources). Note that the input is applied at the base and the output is taken at the emitter. As the collector is grounded (for small signal), it is the common terminal of input and output. Thus, this circuit is called the common-collector amplifier.



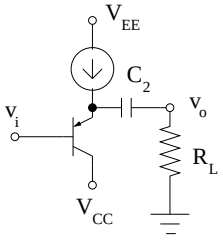
As can be seen this configuration is analogous to MOS common-drain. Similarly to the MOS case, the BJT can be biased many ways. Several "complete" circuits (*i.e.,* including the bias elements) will reduce to the above "small-signal" form of a common-collector amplifier. Some examples are given below.



$R_G = R_1 \parallel R_2$

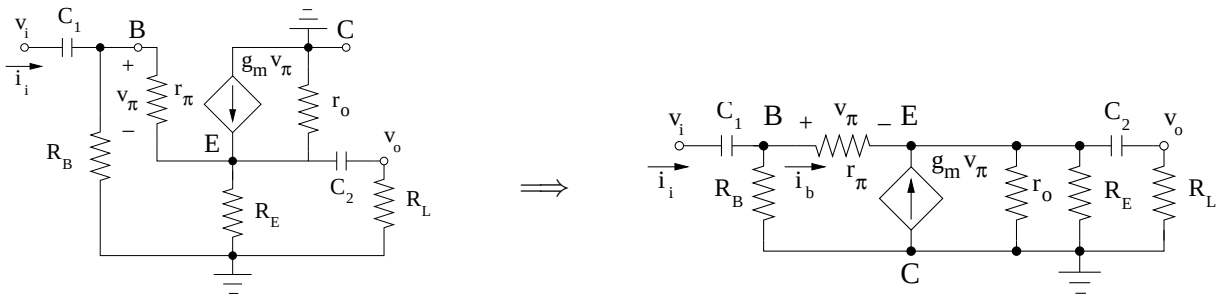


$R_G \to \infty$,
no Pole from C1



$R_G \to \infty$, $R_S \to \infty$,
no Pole from C1

Similar to the common-drain configuration, R_E is parallel to R_L and appears as the load for the transistor. We define $R'_L = R_E \parallel R_L$. and the output resistance is taken to the left of R_E in the circuit above. Proceeding with the small-signal analysis by replacing the BJT with its small-signal model:



Inspecting the circuit, we find that a total current of $i_b + g_m v_\pi$ flows flow in $r_o \parallel R'_L$ (from v_o to the ground) where $i_b = v_\pi / r_\pi$:

$$v_\pi = v_i - v_o$$

Ohm Law: $$v_o = \left(g_m v_\pi + \frac{v_\pi}{r_\pi}\right)(r_o \parallel R'_L) \approx g_m v_\pi (r_o \parallel R'_L) = g_m (r_o \parallel R'_L)(v_i - v_o)$$

$$A_v = \frac{v_o}{v_i} \approx \frac{g_m r_o \parallel R'_L}{g_m r_o \parallel R'_L + 1} = \frac{g_m r_o R'_L}{r_o + R'_L + g_m r_o R'_L}$$

$$A_v \approx \frac{g_m R'_L}{1 + g_m R'_L} = \frac{R'_L}{R'_L + r_e} \qquad A_{vo} = \frac{g_m r_o}{1 + g_m r_o} \approx 1$$

where we have used $g_m r_\pi = \beta \gg 1$ in the 2nd equation to drop v_π / r_π term, and $g_m r_o \gg 1$ to drop R'_L in the denominator of the 3rd equation. Since $r_e \equiv 1/g_m$ in typically a few tens of Ohms, $A_v \approx 1$ unless R'_L is very small (tens of Ω).

This configuration is also called the Emitter Follower. as $v_o = v_e \approx v_b = v_i$ and v_e "follows" the input voltage.

To find $R_i = v_i / i_i$ (note $g_m r_\pi = \beta$):

KCL: $$i_i = \frac{v_i}{R_B} + i_b$$

KVL: $$v_i = i_b r_\pi + (i_b + g_m v_\pi)(r_o \parallel R'_L) = i_b [r_\pi + (1 + g_m r_\pi)(r_o \parallel R'_L)]$$

$$i_i = \frac{v_i}{R_B} + i_b = \frac{v_i}{R_B} + \frac{v_i}{r_\pi + (1+\beta)(r_o \parallel R'_L)}$$

$$\frac{1}{R_i} = \frac{i_i}{v_i} = \frac{1}{R_B} + \frac{1}{r_\pi + (1+\beta)(r_o \parallel R'_L)}$$

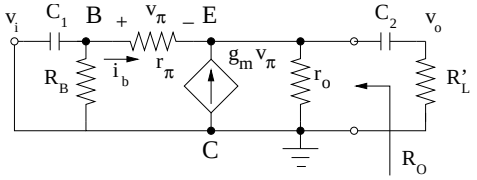
$$R_i = R_B \parallel [r_\pi + (1+\beta)(r_o \parallel R'_L)]$$

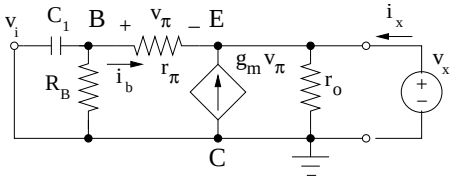
Since R_i depends on R_L, this amplifier configuration is NOT unilateral.

Note that when emitter degeneration biasing is used, we need to have $R_B \ll (1+\beta) R_E$. In this case, $R_i \approx R_B$ (similar to the common-drain amplifier in which $R_i = R_G$) and the

configuration becomes unilateral. If R_B is not present, the input resistance is large although it is not infinite as is the case for the common-drain amplifier.

To find R_o we need to zero out v_i and compute the Thevenin Equivalent resistance seen at the output terminals:





Because of the presence of the controlled source, we need to attach v_x voltage source to the circuit and compute i_x. Noting that $v_\pi = -v_x$

$$\text{KCL:} \qquad i_x = -g_m v_\pi + \frac{v_x}{r_o} + \frac{v_x}{r_\pi} = \frac{v_x}{1/g_m} + \frac{v_x}{r_o} + \frac{v_x}{r_\pi}$$

$$\frac{1}{R_o} = \frac{i_x}{v_x} = \frac{1}{1/g_m} + \frac{1}{r_o} + \frac{1}{r_\pi} \quad \rightarrow \quad R_o = (1/g_m) \parallel r_o \parallel r_\pi \approx (1/g_m) = r_e$$

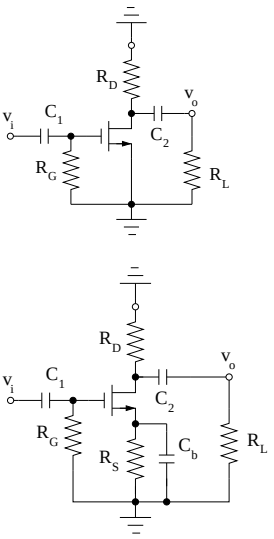
since $g_m r_\pi \gg 1$ and $g_m r_o \gg 1$.

If the output resistance is taken include R_C, $R'_o = R_C \parallel R_o$ (similar to the source follower, see figure in page 5-7).

In summary, the general properties of the common-collector amplifier (emitter follower) include an open-loop voltage gain of unity, a large input resistance and a small output resistance (similar to the common-drain amplifier). Thus, emitter follower is also used as a buffer or to amplify the signal current (and power) and drive a load.

5.3 Common-Source and Common-Emitter Amplifiers

Common-Source Configuration



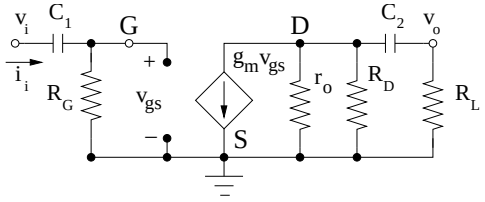
Circuit shown is the generic "small-signal" circuit of a common-drain amplifier (*i.e.,* we have "zeroed" out all Bias sources). Note that the input is applied at the gate and the output is taken at the drain. As the source is grounded (for small signal), it is the common terminal of input and output. Thus, this circuit is called the common-source amplifier.

If source degeneration biasing is used for the common-source configuration, a resistor R_S should be present. A "by-pass" capacitor is typically used so that small signals by-pass R_S, effectively making the source grounded for small signal as is shown.

We replace the MOS with its small-signal model. In this configuration, R_D is parallel to R_L and appears as the load for the transistor. As such, we define $R'_L = R_D \parallel R_L$ and the output resistance is taken to the left of R_D (see below).

Inspection of the circuit shows that $v_i = v_{gs}$. Also, a current of $g_m v_{gs}$ flows in $r_o \parallel R'_L$ (from the ground to v_o).

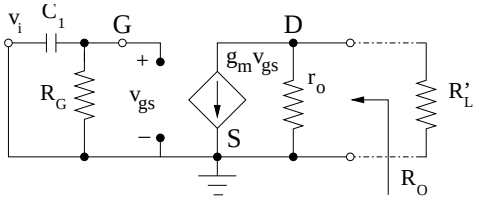
Ohm Law:
$$v_o = -g_m v_{gs}(r_o \parallel R'_L)$$
$$A_v = \frac{v_o}{v_i} = -g_m(r_o \parallel R'_L)$$
$$A_{vo} = -g_m r_o$$



The negative sign in the gain is indicative of a 180° phase shift in the output signal.

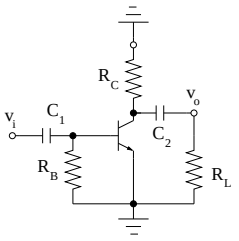
Inspecting the circuit, we find $R_i = v_i/i_i = R_G$ (unilateral amplifier).

To find R_o, we set $v_i = 0$. As $v_{gs} = v_i = 0$, the controlled current source becomes an open circuit and $R_o = r_o$. If the output resistance is taken to include R_D (see discussion in page 5-7), $R'_o = R_D \parallel R_o$.

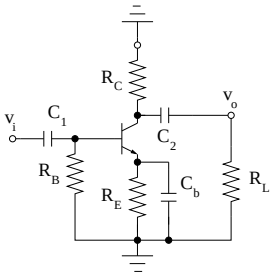


In summary, the general properties of the common-source amplifier include a large open-loop voltage, a large input resistance (and can be made infinite with some biasing schemes) but a medium output resistance.

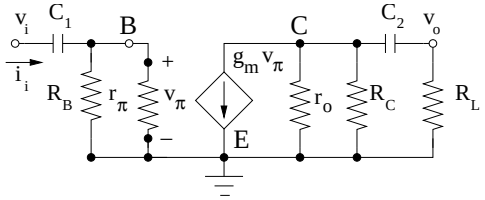
Common-Emitter Configuration



Circuit shown is the generic "small-signal" circuit of a common-emitter amplifier (*i.e.,* we have "zeroed" out all Bias sources). Note that the input is applied at the base and the output is taken at the collector. As the emitter is grounded (for small signal), it is the common terminal of input and output. Thus, this circuit is called the common-emitter amplifier.



Similar to the common-drain configuration, if emitter degeneration biasing is used, a resistor R_E should be present with a by-pass capacitor. This capacitor effectively make the emitter grounded for small signal as is shown.



We now replace the BJT with its small signal model. In this configuration, R_C is parallel to R_L and appears as the load for the transistor ($R'_L = R_C \parallel R_L$) and the output resistance is taken to the left of R_C in the circuit above.

Inspection of the circuit shows that $v_i = v_\pi$. Also, a current of $g_m v_\pi$ flows in $r_o \parallel R'_L$ (from the ground to v_o).

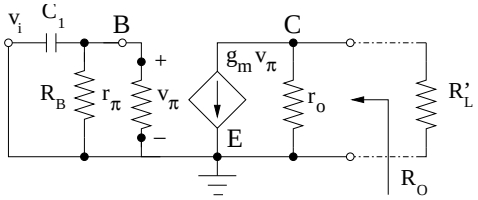
Ohm Law: $v_o = -g_m v_\pi (r_o \parallel R'_L)$

$$A_v = \frac{v_o}{v_i} = -g_m(r_o \parallel R'_L) = -\frac{r_o \parallel R'_L}{r_e}$$

$$A_{vo} = -g_m r_o = \frac{r_o}{r_e}$$

The negative sign in the gain is indicative of a 180° phase shift in the output signal.

From the circuit, we find $R_i = v_i/i_i = R_B \parallel r_\pi$ (a unilateral amplifier)

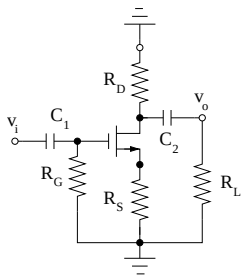


To find R_o, we set $v_i = 0$. As $v_\pi = v_i = 0$, the controlled current source becomes an open circuit and $R_o = r_o$. Similarly, $R'_o = R_C \parallel R_o R_C \parallel r_o$.

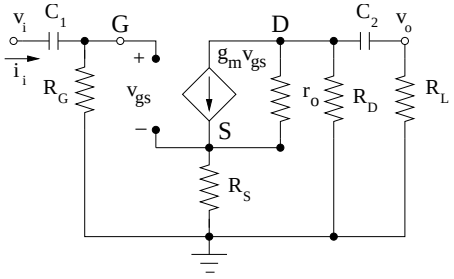
In summary, the general properties of the common-emitter amplifier include a large open-loop voltage, a "medium" input resistance and a medium to large output resistance.

5.4 Common-Source and Common-Emitter Amplifiers with Degeneration

Common-Source Configuration with a Source Resistor



Circuit shown is the generic "small-signal" circuit of a common-source amplifier with degeneration. Note that the input is applied at the gate and the output is taken at the drain similar to a common-drain amplifier but a source resistor is now present.



We replace the MOS with its small-signal model. Similar to the common-drain amplifier, R_D is parallel to R_L and appears as the load for the transistor ($R'_L = R_D \parallel R_L$ and the output resistance is taken to the left of R_D in the circuit above). Using node-voltage method:

$$\text{Node } v_s: \quad \frac{v_s}{R_S} + \frac{v_s - v_o}{r_o} - g_m v_{gs} = 0$$

$$\text{Node } v_o: \quad \frac{v_o}{R'_L} + \frac{v_o - v_s}{r_o} + g_m v_{gs} = 0$$

$$\frac{v_s}{R_S} + \frac{v_o}{R'_L} = 0$$

where the last equation is found by summing the first two. Substituting for $v_{gs} = v_i - v_s$ in the first equation, computing v_s, and substituting in the third equation, we get:

$$A_v = \frac{v_o}{v_i} = -\frac{r_o(g_m R'_L)}{R'_L + r_o + R_S(1 + r_o g_m)} \approx -\frac{r_o(g_m R'_L)}{R'_L + r_o + R_S r_o g_m}$$

$$A_v = -\frac{g_m R'_L}{1 + g_m R_S + R'_L/r_o} \qquad A_{vo} = -g_m r_o$$

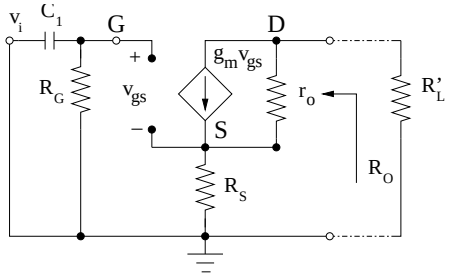
If r_o is large compared to R'_L and/or if R_S and R'_L of the same order (*i.e.*, $R'_L/R_S \ll g_m r_o$), we can drop the last term to find:

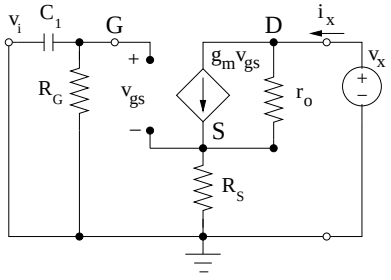
$$A_v \approx -\frac{g_m R'_L}{1 + g_m R_S}$$

The amplifier gain is substantially reduced with the presence of R_S but it has become much less sensitive to change in g_m.

Inspecting the circuit we find $R_i = v_i/i_i = R_G$, similar to a common-source amplifier.

To find R_o, we set $v_i = 0$ and compute the Thevenin Equivalent resistance seen at the output terminals. Because of the presence of the controlled source, we need to attach v_x voltage source to the circuit and compute i_x.





By KCL, a current of $i_x - g_m v_{gs}$ should flow in r_o and i_x should flow in R_S. Since $v_{gs} = -R_S i_x$:

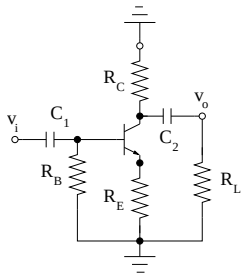
$$\text{KVL}: \quad v_x = r_o(i_x - g_m v_{gs}) + R_S i_x = r_o(i_x + g_m R_S i_x) + R_s i_x = i_x(r_o + g_m r_o R_S + R_S)$$

$$R_o = \frac{v_x}{i_x} = r_o + R_S + g_m r_o R_S \approx r_o(1 + g_m R_S)$$

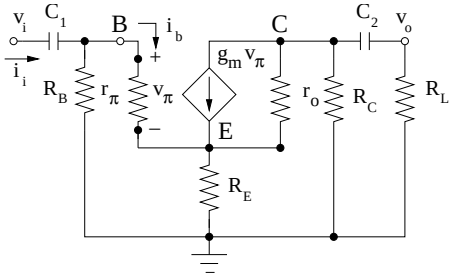
In summary, source degeneration has led to an amplifier with a lower gain which is less sensitive to transistor parameters and several other benefits (*e.g.,* larger band-width) which are beyond the scope of this course.

Common-Emitter Configuration with an Emitter Resistor

Circuit shown is the generic "small-signal" circuit of a common-emitter amplifier with degeneration (*i.e.,* with emitter resistor). Note that the input is applied at the base and the output is taken at the collector similar to a common-emitter amplifier.



We now replace the BJT with its small-signal model. Similar to the common-drain amplifier, R_C is parallel to R_L and appears as the load for the transistor ($R'_L = R_C \parallel R_L$) and the output resistance is taken to the left of R_C in the circuit above. Using node-voltage method and noting $v_\pi = v_i - v_e$:



$$\text{Node } v_e: \quad 0 = \frac{v_e}{R_E} + \frac{v_e - v_i}{r_\pi} + \frac{v_e - v_o}{r_o} - g_m v_\pi$$

$$\text{Node } v_o: \quad 0 = \frac{v_o}{R'_L} + \frac{v_o - v_e}{r_o} + g_m v_\pi = 0$$

$$\frac{v_e}{R_E} + \frac{v_o}{R'_L} + \frac{v_e - v_i}{r_\pi} = 0$$

The third equation is the sum of the first two. Finding v_e from the third equation and substituting in the 2nd equation, we get:

$$A_v = \frac{v_o}{v_i} = -\frac{g_m R'_L}{g_m R_E + (1 + R'_L/r_o)(1 + R_E/r_\pi)} = -\frac{R'_L}{R_E + (1 + R'_L/r_o)(R_E + r_\pi)/\beta}$$

$$A_v \approx -\frac{R'_L}{R_E + r_e + (R'_L/r_o)(R_E + r_\pi)/\beta}$$

$$A_{vo} = -\frac{g_m r_o}{1 + R_E/r_\pi} = -\frac{r_o}{r_e + R_E/\beta}$$

If $(R'_L/r_o)/\beta \ll 1$ (a very good approximation), we can drop the last term to find:

$$A_v \approx -\frac{g_m R'_L}{1 + g_m R_E} = -\frac{R'_L}{R_E + r_e}$$

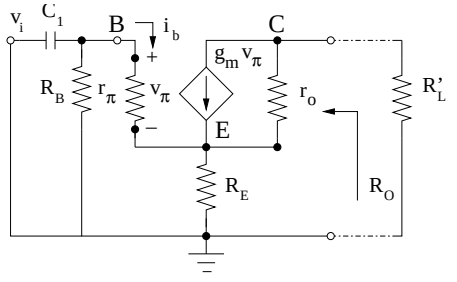
which is the expression often used. Note that the amplifier gain is reduced with the presence of R_E but it has become substantially less sensitive to any change in β (only through r_e).

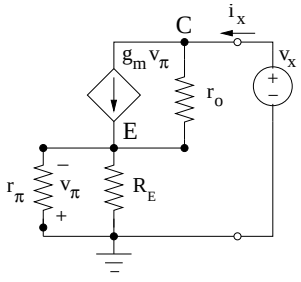
From the circuit we find $R_i = v_i/i_i = R_B \parallel (v_i/i_b)$. The exact formulation for v_i/i_b is cumbersome. A good approximation which leads to a simple expression is $r_o \gg R_E$. In this case, r_o can be removed from the circuit and

$$v_i = i_b r_\pi + (i_b + g_m v_\pi) R_E = i_b r_\pi + (i_b + \beta i_b) R_E = i_b [r_\pi + (1 + \beta) R_E]$$

$$R_i = R_B \parallel [r_\pi + (1 + \beta) R_E]$$

To find R_o, we set $v_i = 0$ and compute the Thevenin Equivalent resistance seen at the output terminals. Because of the presence of the controlled source, we need to attach v_x voltage source to the circuit and compute i_x. By KCL, current $i_x - g_m v_\pi$ will flow through r_o and current i_x will flow through $R_E \parallel r_\pi$:





$$v_\pi = -i_x (R_E \parallel r_\pi)$$

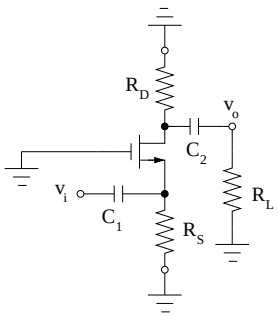
KVL: $$v_x = (i_x - g_m v_\pi) r_o + i_x (R_E \parallel r_\pi) = i_x [r_o + g_m r_o (R_E \parallel r_\pi)]$$

$$R_o = r_o [1 + g_m (R_E \parallel r_\pi)] = r_o \left(1 + \frac{\beta R_E}{r_\pi + R_E}\right)$$

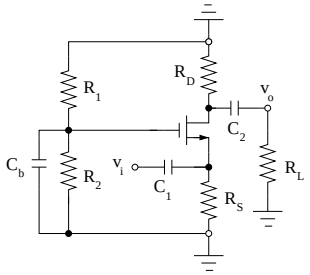
In summary, emitter degeneration has led to an amplifier with a lower gain which is much less sensitive to transistor parameters, a substantially larger input resistance and a somewhat larger output resistance.

5.5 Common-Gate and Common-Base Amplifiers

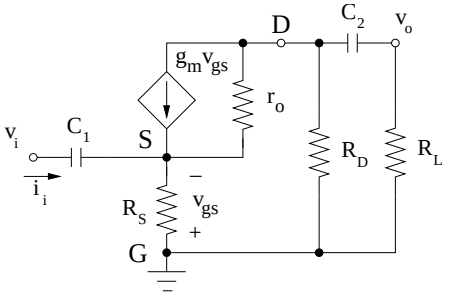
Common-Gate Configuration



Circuit shown is the generic "small-signal" circuit of a common-gate amplifier. Note that the input is applied at the source and the output is taken at the drain. As the gate is grounded (for small signal), it is the common terminal of input and output. Thus, this circuit is called the common gate amplifier. If the base has to biased to a DC value (for example using voltage divider circuit shown), a by-pass capacitor is added to short the base for small signals as is shown with $R_G = R_2 \parallel R_1$.



We replacing MOS with its small signal model. In this configuration, R_D is parallel to R_L and appears as the load for the transistor. As such, we define $R'_L = R_D \parallel R_L$ and the output resistance is taken to the left of R_D in the circuit above. Noting that $v_i = -v_{gs}$ and writing the node equation at v_o:

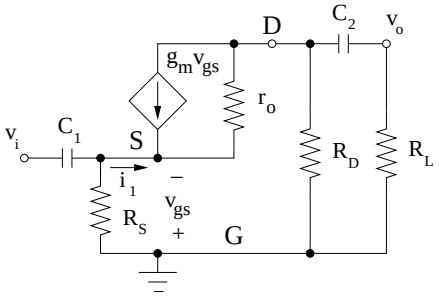


$$\frac{v_o}{R'_L} + \frac{v_o - v_i}{r_o} + g_m(-v_i) = 0$$

$$v_o\left(\frac{1}{R'_L} + \frac{1}{r_o}\right) = v_i \times \frac{1 + g_m r_o}{r_o} \approx v_i \times \frac{g_m r_o}{r_o}$$

$$A_v = \frac{v_o}{v_i} = g_m(R'_L \parallel r_o)$$

$$A_{vo} = g_m r_o$$



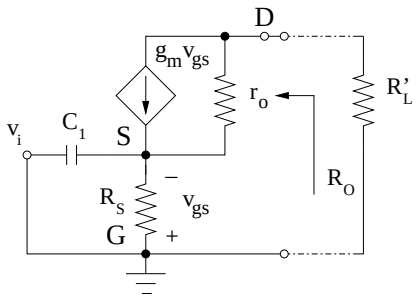
To find R_i, it is easier to write $R_i = R_S \parallel \frac{v_i}{i_1}$ (see circuit). By KCL at node S, current $i_1 + g_m v_{gs}$ will flow in r_o and current i_1 will flow in $R'_L = R_D \parallel R_L$. Thus:

$$v_i = (i_1 + g_m v_{gs}) r_o + i_1 R'_L$$

$$v_i = i_1 r_o - g_m r_o v_i + i_1 R'_L$$

$$\frac{v_i}{i_1} = \frac{r_o + R'_L}{1 + g_m r_o} \approx \frac{1 + R'_L/r_o}{g_m}$$

$$R_i = R_S \parallel \frac{1 + R'_L/r_o}{g_m}$$



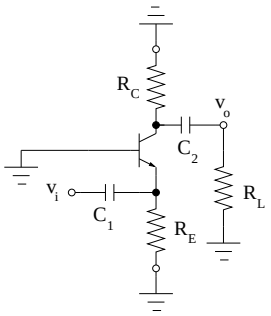
As can be seen, the common-gate amplifier is NOT unilateral *i.e.,* R_i depends on the load.

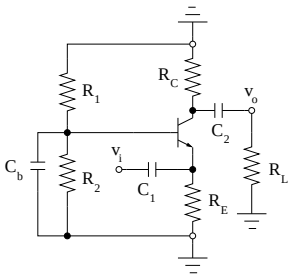
To find R_o, we set $v_i = 0$. As $v_{gs} = v_i = 0$, the controlled current source becomes an open circuit and $R_o = r_o$ (Note that R_S is shorted out).

In summary, the general properties of the common-gate amplifier include a large open-loop voltage, a small input resistance and a medium output resistance (it has the same gain and output resistance values as that of a common-source configuration but a much lower input resistance).

Common-Base Configuration

Circuit shown is the generic "small-signal" circuit of a common-base amplifier. Note that the input is applied at the source and the output is taken at the drain. As the gate is grounded (for small signal), it is the common terminal of input and output. Thus, this circuit is called the common-gate amplifier. If the base has to biased to a DC value (for example using voltage divider circuit shown), a by-pass capacitor is added to short the base for small signals as is shown with $R_B = R_2 \parallel R_1$.





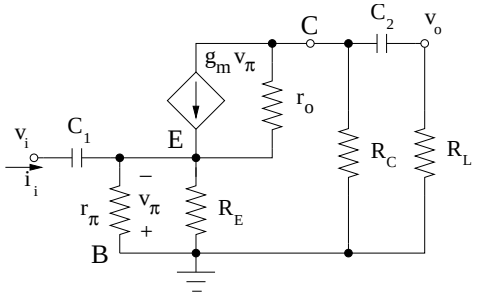
We replace the BJT with its small signal model. In this configuration, R_C is parallel to R_L and appears as the load for the transistor. As such, we define $R'_L = R_C \parallel R_L$ and the output resistance is taken to the left of R_C in the circuit above. Noting that $v_i = -v_\pi$ and writing the node equation at v_o:

$$\frac{v_o}{R'_L} + \frac{v_o - v_i}{r_o} + g_m v_\pi = 0$$

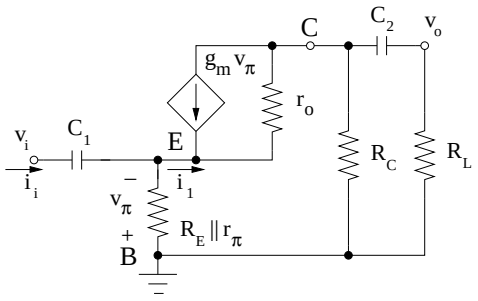
$$v_o \left(\frac{1}{R'_L} + \frac{1}{r_o} \right) = v_i \times \frac{1 + g_m r_o}{r_o} \approx v_i \times \frac{g_m r_o}{r_o}$$

$$A_v = \frac{v_o}{v_i} = g_m (R'_L \parallel r_o)$$

$$A_{vo} = g_m r_o$$



To find R_i, it is easier to write $R_i = (R_E \parallel r_\pi) \parallel \frac{v_i}{i_1}$ (see circuit). By KCL at node E, current $i_1 + g_m v_\pi$ will flow in r_o and current i_1 will flow in $R'_L = R_C \parallel R_L$. Thus (setting $v_\pi = -v_i$) by KVL:



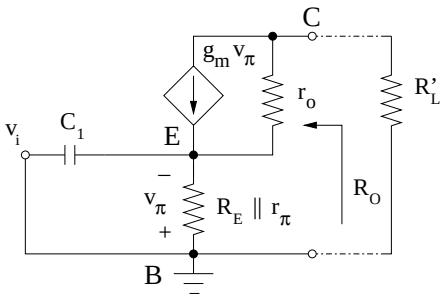
$$v_i = (i_1 + g_m v_\pi) r_o + i_1 R'_L = i_1 r_o - g_m r_o v_i + i_1 R'_L$$

$$\frac{v_i}{i_1} = \frac{r_o + R'_L}{1 + g_m r_o} \approx \frac{1 + R'_L/r_o}{g_m}$$

$$R_i = R_E \parallel r_\pi \parallel \frac{1 + R'_L/r_o}{g_m}$$

As can be seen, the common-base amplifier is NOT unilateral *i.e.,* R_i depends on the load.

To find R_o, we set $v_i = 0$. As $v_\pi = 0$, the controlled current source becomes an open circuit and $R_o = r_o$ (Note that $R_E \parallel r_\pi$ is shorted out).



In summary, the common-base configuration has a large open-loop voltage, a small input resistance and a medium output resistance (it has the same gain and output resistance values as that of a common-emitter configuration but a much lower input resistance).

5.6 Summary of Amplifier Configurations

- The common-source (CS) and common-emitter (CE) amplifiers have a high gain and are the main configuration in a practical amplifier. Ignoring bias resistors R_G or R_B, the CS configuration has an infinite input resistance while the CE amplifier has a modest input resistance. Both CS and CE amplifier have a rather high output resistance r_o and a limited high-frequency response (you will see this in 102).

- Addition of source or emitter resistor (degenerated CS or CE) leads to several benefits: a gain which is less sensitive to temperature, a much larger input resistance for CE configuration, a better control of amplifier saturation, and a much improved high-frequency response. However, these are realized at the expense of a lower gain.

- The common-gate (CG) and commons-base (CB) amplifiers have a high gain (similar to CS and CE) but a low input resistance. As such, they are only used for specialized applications. CG and CB amplifiers have an excellent high-frequency response. They are typically used in combination with a CS or CE stage (such as cascode amplifiers)

- The source-follower and emitter-follower configurations have a high input resistance, a gain close to unity, and a low output resistance. They are employed as a voltage buffer and/or as the output stage to increase the current and power to the load.

5.7 Low Frequency Response of Transistor Amplifiers

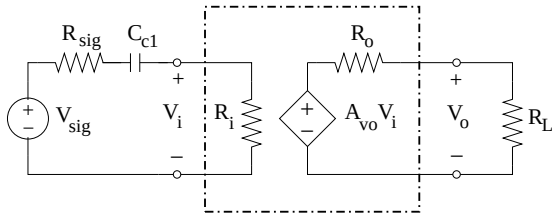
Up to now, we have neglected the impact of the coupling and by-pass capacitors (assumed they were short circuit). Each of these capacitors introduce a pole in the response of the circuit. For example, let's consider the coupling capacitor at the input to the amplifier (C_{c1} in amplifier configurations that we examined before). We need to perform the analysis in the frequency domain (voltage are represented by capital letter as they are in "phasor" form):

$$A_v = \frac{V_o}{V_i} = \frac{R_L}{R_o + R_L} A_{vo}$$

$$\frac{V_i}{V_{sig}} = \frac{R_i}{R_i + R_{sig} + 1/(sC_{c1})}$$

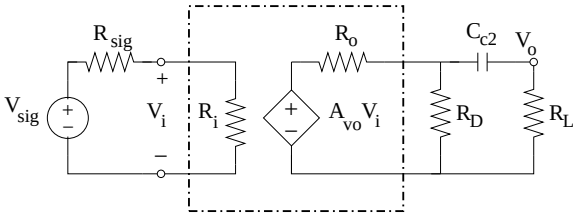
$$\frac{V_i}{V_{sig}} = \frac{R_i}{R_i + R_{sig}} \times \frac{s}{s + \omega_{p1}}, \qquad 2\pi f_{p1} = \omega_{p1} \equiv \frac{1}{C_{c1}(R_i + R_{sig})}$$

$$\frac{V_o}{V_{sig}} = \frac{R_i}{R_i + R_{sig}} \times A_v \times \frac{s}{s + \omega_{p1}}$$



Where A_v is the mid-frequency gain that we have calculated for all transistor configurations (*i.e.,* with capacitors short). As can be seen, the coupling capacitor C_{c1} has introduced a low-frequency pole and the amplifier gain falls at low frequencies.

One may be tempted to compute the impact of the coupling capacitor at the output in a similar manner. Figure below is for a common-drain amplifier (with R_D appearing as the load, see figure in page 5-5). It is straightforward to show (left as an exercise):



$$\frac{V_o}{V_{sig}} = \frac{R_i}{R_i + R_{sig}} \times A_v \times \frac{s}{s + \omega_{p2}} \qquad 2\pi f_{p2} = \omega_{p2} \equiv \frac{1}{C_{c2}(R_L + R_D \parallel R_o)}$$

For unilateral amplifiers, f_{p2} calculated above is the pole introduced by C_{c2}. However, if the amplifier is NOT unilateral, R_i depends on the load and the expression of R_i will include C_{c2} as this capacitor is part of the load ($R'_L = R_D \parallel (R_L + 1/sC_{c2})$). As such, we need to compute the $R_i/(R_i + R_{sig})$ term to find the pole introduced by C_{c2}. This issue is specially important for amplifiers with small R_i, *i.e.,* common-gate and common-base amplifiers.

We can still use the above formula, however, if we replace R_o (output resistance with $v_i = 0$) with R_{out} (output resistance with $v_{sig} = 0$).

Similarly, if a by-pass capacitor is present (see page 5-8), it will introduce yet another pole, f_{p3}.

The following method allows one to compute the poles by "inspection."

1. Zero out V_{sig}.

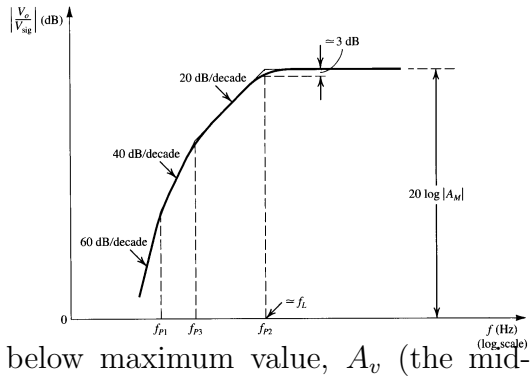
2. Consider each capacitor separately (*i.e.,* assume all other capacitors are short)

3. Compute, $\bar{R}$, the "total" resistance between the terminals of the capacitor. The pole introduced by that capacitor is given by

$$f_p \equiv \frac{1}{2\pi C\bar{R}}$$

With all poles associated with by-pass and coupling capacitors in hand, we can find the overall frequency response of the amplifier as

$$\frac{V_o}{V_{sig}} = A_v \times \frac{s}{s+\omega_{p1}} \times \frac{s}{s+\omega_{p2}} \times \frac{s}{s+\omega_{p3}} \times \cdot$$



and the lower cut-off frequency is located at 3dB below maximum value, A_v (the mid-frequency gain). If poles are sufficiently separated (such as the figure above), the lower cut-off frequency of the amplifier is given by the highest-frequency pole. Otherwise, finding the lower cut-off frequency would be cumbersome.

A simple approximation for hand calculations (which is surprisingly very good) is to set

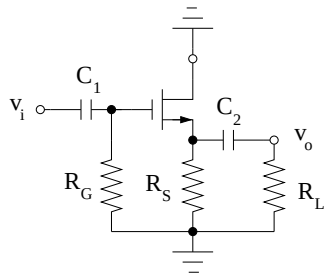
$$f_l \approx f_{p1} + f_{p2} + f_{p3} + \cdot$$

Exercise: Show that the method above gives the poles corresponding to C_{c1} and C_{C2} (for unilateral amplifier) as was calculated previously.

The next two pages include a summary of formulas for elementary transistor configurations. These formulas are correct within approximation of $g_m r_o \gg 1$ and $\beta \gg 1$ both of which are always valid. Many of these formulas can be simplified (before plugging in numbers) as they include resistances that are in parallel and "typically" one is much smaller (at least a factor of ten) than the others. For example, in a common emitter amplifier, we often find that $R_C \ll R_L$ and $R_C \ll r_o$. Then, $r_o \parallel R_C \parallel R_L \approx R_C$ and the gain formula can be simplified to $A_v = -R_C/r_e$.

Summary of Elementary MOS Configurations•

Common Drain (Source Follower):



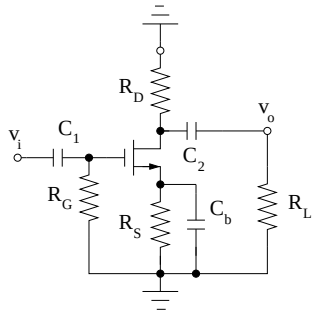
$$A_v = \frac{g_m(R_S \parallel R_L)}{1 + g_m(R_S \parallel R_L)}$$

$$R_i = R_G$$

$$R_o = \frac{1}{g_m} \parallel r_o \approx \frac{1}{g_m} \qquad R'_o = R_S \parallel R_o$$

$$f_{p2} = 1/[2\pi C_{c2}(R_L + R_S \parallel R_{out})] \qquad R_{out} = \frac{1}{g_m}$$

Common Source:



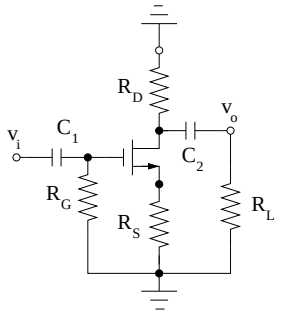
$$A_v = -g_m(r_o \parallel R_D \parallel R_L)$$

$$R_i = R_G \qquad R_o = r_o \qquad R'_o = R_D \parallel R_o$$

$$f_{p2} = 1/[2\pi C_{c2}(R_L + R_D \parallel R_{out})] \qquad R_{out} = r_o$$

$$f_{pb} = \frac{1}{2\pi C_b[R_S \parallel (1/g_m)]}$$

Common Source with Source Resistance:



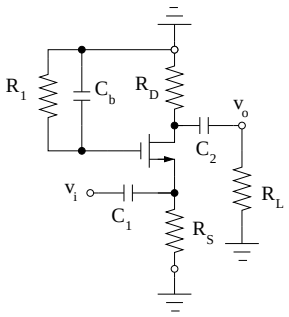
$$A_v = -\frac{g_m(R_D \parallel R_L)}{1 + g_m R_S + (R_D \parallel R_L)/r_o}$$

$$R_i = R_G$$

$$R_o = r_o(1 + g_m R_S) \qquad R'_o = R_D \parallel R_o$$

$$f_{p2} = 1/[2\pi C_{c2}(R_L + R_D \parallel R_{out})] \qquad R_{out} = r_o(1 + g_m R_S)$$

Common Gate:



$$A_v = g_m(r_o \parallel R_D \parallel R_L)$$

$$R_i = R_S \parallel [1/g_m + (R_D \parallel R_L)/g_m r_o]$$

$$R_o = r_o \qquad R'_o = R_D \parallel R_o$$

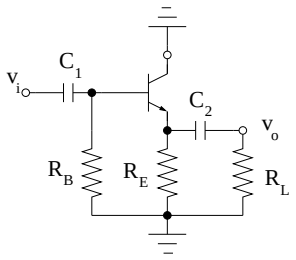
$$f_{p2} = 1/[2\pi C_{c2}(R_L + R_D \parallel R_{out})] \qquad R_{out} = r_o(1 + g_m R_S)$$

$$f_{pb} = 1/[2\pi C_b R_G]$$

• $f_l = \Sigma_j f_{pj}$ and $f_{p1} = 1/[2\pi C_{c1}(R_i + R_{sig})]$.

Summary of Elementary BJT Configurations•

Common Collector (Emitter Follower):



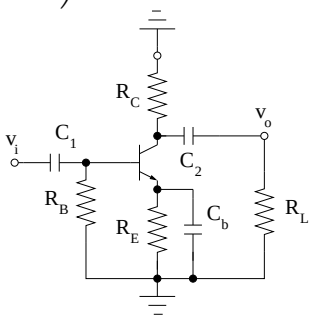
$$A_v = \frac{g_m(R_E \parallel R_L)}{1 + g_m(R_E \parallel R_L)} = \frac{R_E \parallel R_L}{R_E \parallel R_L + r_e}$$

$$R_i = R_B \parallel [r_\pi + (1+\beta)(r_o \parallel R_E \parallel R_L)]$$

$$R_o = r_\pi \parallel \frac{1}{g_m} \approx \frac{1}{g_m} = r_e \qquad R'_o = R_E \parallel R_o$$

$$f_{p2} = 1/[2\pi C_{c2}(R_L + R_E \parallel R_{out})] \qquad R_{out} = r_o \parallel \left(\frac{r_\pi + R_B \parallel R_{sig}}{1+\beta}\right) \approx r_e$$

Common Emitter:



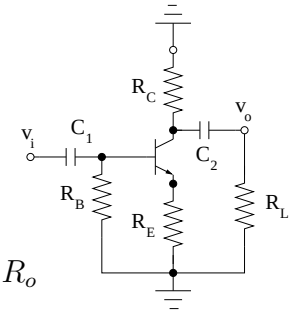
$$A_v = -g_m(r_o \parallel R_C \parallel R_L) = -\frac{r_o \parallel R_C \parallel R_L}{r_e}$$

$$R_i = R_B \parallel r_\pi \qquad R_o = r_o \qquad R'_o = R_C \parallel R_o$$

$$f_{p2} = 1/[2\pi C_{c2}(R_L + R_C \parallel R_{out})] \qquad R_{out} = r_o$$

$$f_{pb} = \frac{1}{2\pi C_b[R_E \parallel (r_e + (R_B \parallel R_{sig})/\beta)]}$$

Common Emitter with Emitter Resistor:



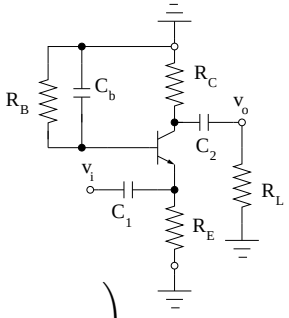
$$A_v = -\frac{g_m(R_C \parallel R_L)}{1 + g_m R_E} = -\frac{R_C \parallel R_L}{R_E + r_e}$$

$$R_i = R_B \parallel [r_\pi + (1+\beta)R_E]$$

$$R_o = r_o[1 + g_m(R_E \parallel r_\pi)] = r_o\left(1 + \frac{\beta R_E}{r_\pi + R_E}\right) \qquad R'_o = R_C \parallel R_o$$

$$f_{p2} = 1/[2\pi C_{c2}(R_L + R_C \parallel R_{out})] \qquad R_{out} = r_o\left(1 + \frac{\beta R_E}{r_\pi + R_E + R_B \parallel R_{sig}}\right)$$

Common Base:



$$A_v = g_m(r_o \parallel R_C \parallel R_L) = \frac{r_o \parallel R_C \parallel R_L}{r_e}$$

$$R_i = R_E \parallel r_\pi \parallel [1/g_m + (R_C \parallel R_L)/(g_m r_o)]$$

$$R_o = r_o \qquad R'_o = R_C \parallel R_o$$

$$f_{p2} = 1/[2\pi C_{c2}(R_L + R_C \parallel R_{out})] \qquad R_{out} = r_o\left(1 + \frac{\beta R_E}{r_\pi + R_E + R_B \parallel R_{sig}}\right)$$

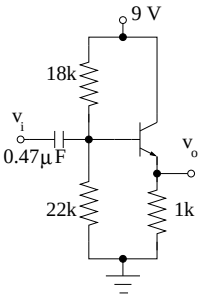
$$f_{pb} = 1/[2\pi C_b R_{CB}] \qquad R_{CB} \equiv R_B \parallel [r_\pi + (1+\beta)(R_{sig} \parallel R_E)]$$

5.8 Exercise Problems

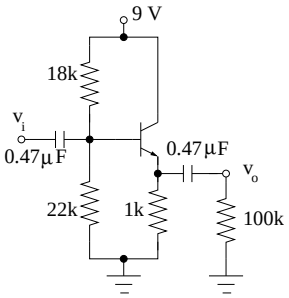
Problem 1 to 3: Find the bias point and amplifier parameters of this circuit (Si BJT with $n = 2$, $\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations).

Problem 4: If $v_i = V_i \cos(\omega t)$ in the circuit of Problem 3, what is the maximum value of V_i for this circuit to work properly?

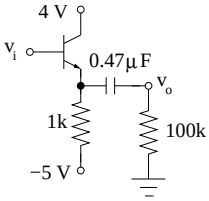
Problem 5 to 14: Find the bias point and amplifier parameters of this circuit (Si BJT with $n = 2$, $\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations). Find the maximum amplitude of v_i for the circuit to work properly.



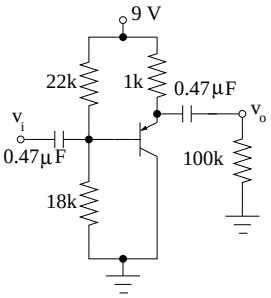
Problem 1



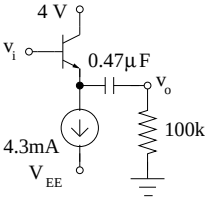
Problem 2



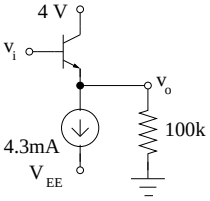
Problem 3



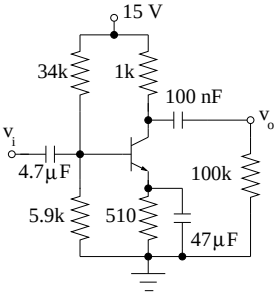
Problem 5



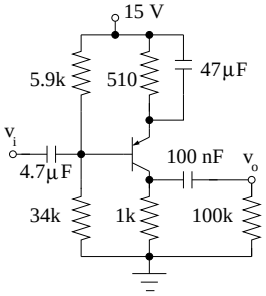
Problem 6



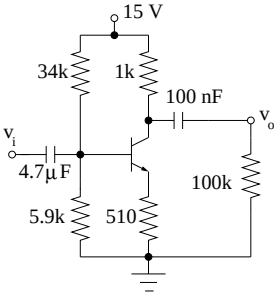
Problem 7



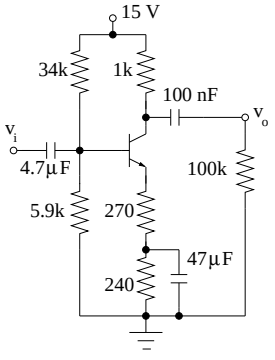
Problem 8



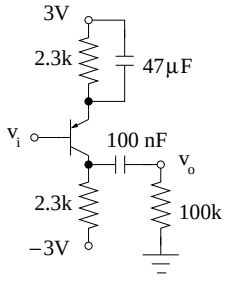
Problem 9



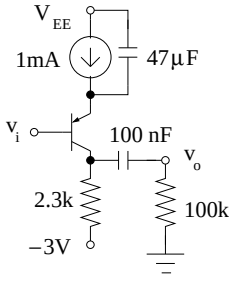
Problem 10



Problem 11



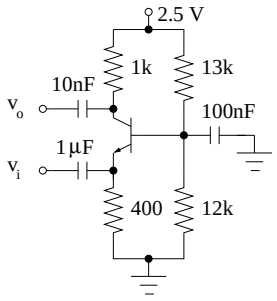
Problem 12



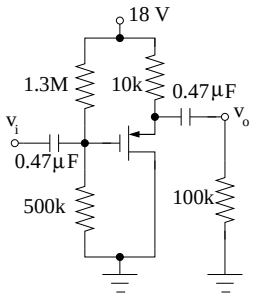
Problem 13

Problem 15-18. Find the bias point and amplifier parameters of this circuit ($V_{tn} = 4$ V, $V_{tp} = -4$ V, $k'(W/L) = 0.4$ mA/V^2, Ignore the channel-width modulation effect in biasing calculations. Find the saturation voltages for this amplifier.

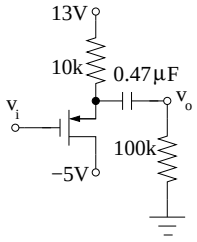
Problem 19-26. Find the bias point and amplifier parameters of this circuit ($V_{tn} = 1$ V, $V_{tp} = -1$ V, $k'_p(W/L) = k'_n(W/L) = 0.8$ mA/V^2, $\lambda = 0.01$ V^{-1}). Ignore the channel-width modulation effect in biasing calculations. Find the saturation voltages for this amplifier.



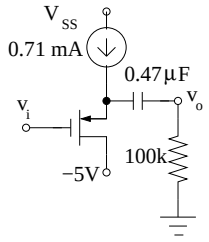
Problem 14



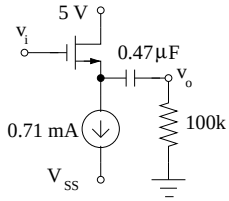
Problem 15



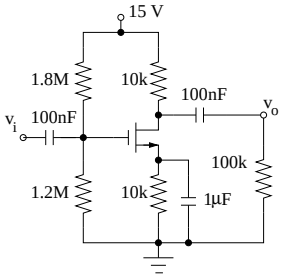
Problem 16



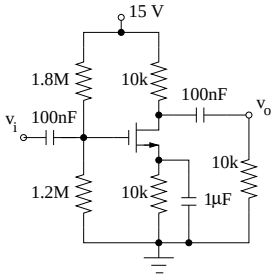
Problem 17



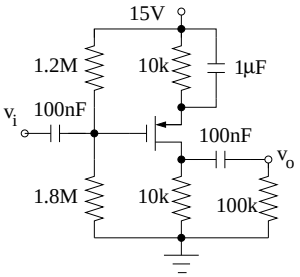
Problem 18



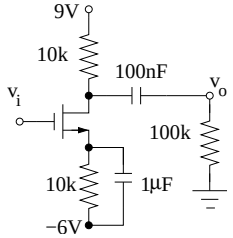
Problem 19



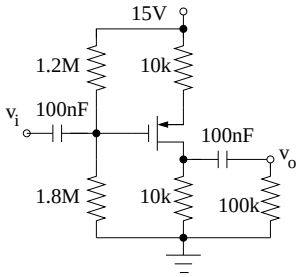
Problem 20



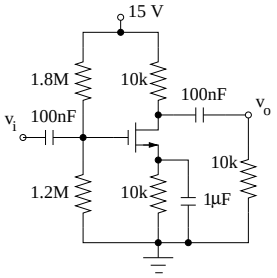
Problem 21



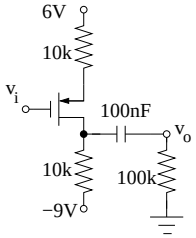
Problem 22



Problem 23

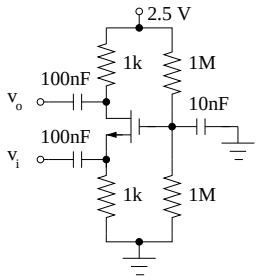


Problem 24

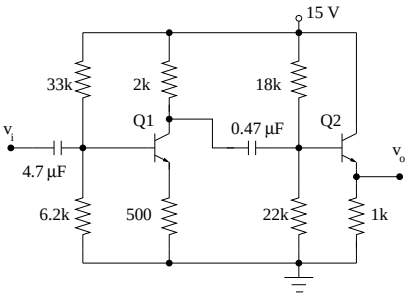


Problem 25

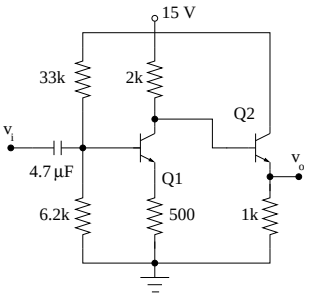
Problems 27 to 29: Find the bias point of each BJT, the overall gain (v_o/v_i), and the lower cut-off frequency of this amplifier parameters (Si BJT with $n = 2$, $\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations).



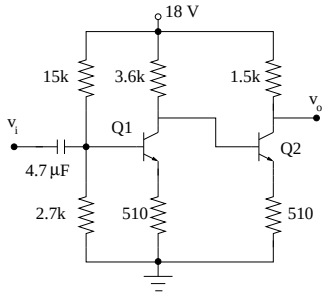
Problem 26



Problem 27



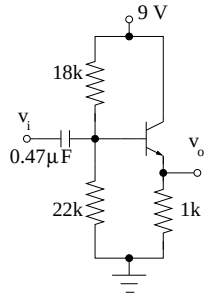
Problem 28



Problem 29

5.9 Solution to Selected Exercise Problems

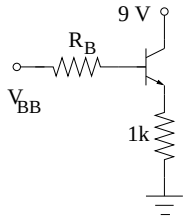
Problem 1. Find the bias point and amplifier parameters of this circuit (Si BJT with $n = 2$, $\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations).



Bias:

Set $v_i = 0$ and capacitors open. Replace R_1 and R_2 with their Thevenin equivalent:

$$R_B = 18 \text{ k} \parallel 22 \text{ k} = 9.9 \text{ k}\Omega \qquad V_{BB} = \frac{22}{18+22} \times 9 = 4.95 \text{ V}$$



KVL: $\quad V_{BB} = R_B I_B + V_{BE} + 10^3 I_E \qquad I_B = \dfrac{I_E}{1+\beta} = \dfrac{I_E}{201}$

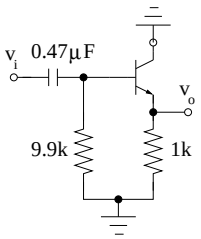
$$4.95 - 0.7 = I_E \left(\frac{9.9 \times 10^3}{201} + 10^3 \right)$$

$$I_E = 4 \text{ mA} \approx I_C, \qquad I_B = \frac{I_C}{\beta} = 20 \ \mu\text{A}$$

KVL: $\quad 9 = V_{CE} + 10^3 I_E$

$$V_{CE} = 9 - 10^3 \times 4 \times 10^{-3} = 5 \text{ V}$$

Bias summary: $\quad I_E \approx I_C = 4 \text{ mA}, \quad I_B = 20 \ \mu\text{A}, \quad V_{CE} = 5 \text{ V}$



Small-Signal: First we calculate the small-signal parameters:

$$g_m = \frac{I_C}{nV_T} = \frac{4 \times 10^{-3}}{2 \times 26 \times 10^{-3}} = 7.69 \times 10^{-2} \qquad r_e = \frac{1}{g_m} = 13 \ \Omega$$

$$r_\pi = \frac{\beta}{g_m} = 2.60 \text{ k} \qquad r_o = \frac{V_A + V_{CE}}{I_C} = \frac{150+5}{4 \times 10^{-3}} = 38.8 \text{ k}$$

Note that we could have ignored V_{CE} compared to V_A in the above expression for r_o. Proceeding with the small signal analysis, we zero bias sources (see circuit). As the input is at the base and output is at the emitter, this is a common-collector amplifier (emitter follower). Using formulas of page 5-21 and noting $R_L \to \infty$, $R_E \ll r_o$, and $R_E \gg r_e$:

$$A_v = \frac{R_E \parallel R_L}{R_E \parallel R_L + r_e} \approx \frac{R_E}{R_E + r_e} \approx 1$$

$$R_i \approx R_B \parallel [r_\pi + (1+\beta) R_E] = (9.9 \text{ k}) \parallel (203.6 \text{ k}) \approx 9.9 \text{ k} = R_B$$

$$R_o = r_e = 13 \ \Omega$$

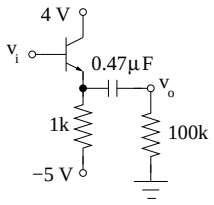
$$f_l = f_{p1} = \frac{1}{2\pi C_{c1}(R_i + R_{sig})} = \frac{1}{2\pi \times 0.47 \times 10^{-6} \times 9.9 \times 10^3} = 34 \text{ Hz}$$

Problem 2. Find the bias point and amplifier parameters of this circuit (Si BJT with $n = 2$, $\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations).

This is the same circuit as Problem 1 with exception of C_{c2} and R_L. The bias point is exactly the same. As $R_E \ll R_L$, the amplifier parameters are the same except $f_l = f_{p1} + f_{p2} = 37$ Hz.

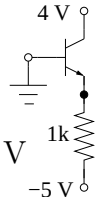
Problem 3. Find the bias point and amplifier parameters of this circuit (Si BJT with $n = 2$, $\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations).

This circuit is similar to Problem 1 expect that the transistor is biased with two voltage sources (values are chosen to give the same bias point).



Bias:

Set $v_i = 0$ and capacitors open:



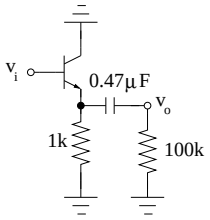
BE-KVL: $\quad 0 = V_{BE} + 10^3 I_E - 5$

$$I_E = 4.3\text{mA} \approx I_C, \qquad I_B = \frac{I_C}{\beta} = 21.5\ \mu\text{A}$$

CE-KVL: $\quad 4 = V_{CE} + 10^3 I_E - 5 \quad \rightarrow \quad V_{CE} = 9 - 10^3 \times 4.3 \times 10^{-3} = 4.7$ V

Bias summary: $\quad I_E \approx I_C = 4.3$ mA, $\quad I_B = 21.5\ \mu$A, $\quad V_{CE} = 4.7$ V

Small-Signal: First we calculate the small-signal parameters:



$$g_m = \frac{I_C}{nV_T} = \frac{4.3 \times 10^{-3}}{2 \times 26 \times 10^{-3}} = 8.27 \times 10^{-2} \qquad r_e = \frac{1}{g_m} = 12.1\ \Omega$$

$$r_\pi = \frac{\beta}{g_m} = 2.42\text{ k} \qquad r_o = \frac{V_A + V_{CE}}{I_C} = \frac{150 + 5}{4.3 \times 10^{-3}} = 36.0\text{ k}$$

Proceeding with the small signal analysis, we zero bias sources (see circuit). As the input is at the base and output is at the emitter, this is a common-collector amplifier (emitter follower). Using formulas of page 5-21 and noting $R_E \ll R_L$, $R_E \ll r_o$, and $R_E \gg r_e$:

$$A_v = \frac{R_E \parallel R_L}{R_E \parallel R_L + r_e} = \frac{R_E}{R_E + r_e} \approx 1$$

$$R_i \approx R_B \parallel [r_\pi + (1+\beta)R_E] = r_\pi + (1+\beta)R_E = 2.42 + 201 = 203\text{ k}$$

$$R_o = r_e = 12\ \Omega$$

$$f_l = f_{p2} = \frac{1}{2\pi C_{c2}(R_L + R_E \parallel r_e)} \approx \frac{1}{2\pi C_{c2}(R_L + r_e)} \approx \frac{1}{2\pi C_{c2} R_L} = 3.4\text{ Hz}$$

Problem 4: If $v_i = V_i \cos(\omega t)$ in the circuit of Problem 3, what is the maximum value of V_i for this circuit to work properly?

For the amplifier to work properly, the BJT has to remain in the active state, *i.e,* $i_E = I_E + i_e > 0$ and $v_{CE} = V_{CE} + v_{ce} > V_{D0} = 0.7$ V. The first equation gives a minimum value for i_e (or $i_C > 0$ gives a minimum value for i_c). Combination of the 2nd equation and CE-KVL gives a maximum value for i_e (or i_c). Limits on v_o can be found from the two limits for i_e (*e.g.,* in this problem $v_o = 10^3 i_e$ as $R_L \gg R_E$). $v_i = v_o/A_v$ then gives the range for v_i:

$$i_E = I_E + i_e > 0 \quad \rightarrow \quad i_e > -I_E = -4.3 \text{ mA} \quad \rightarrow \quad v_o = 10^3 i_e > -4.3 \text{ V}$$

$$\text{CE-KVL} \quad 4 = v_{CE} + 10^3 i_E - 5 \quad \rightarrow \quad 10^3 i_E < 9 - v_{CE}$$

$$v_{CE} > V_{D0} = 0.7 \quad \rightarrow \quad 10^3 i_E = 10^3 (I_E + i_e) < 8.3 \text{ V} \quad \rightarrow \quad v_o = 10^3 i_e < 4.0 \text{ V}$$

$$-4.3 < v_o = A_v v_i < 4.0 \text{ V} \quad \rightarrow \quad -4.3 < v_i < 4.0 \text{ V} \quad \rightarrow \quad V_i < 4.0 \text{ V}$$

Problem 5. Find the bias point and amplifier parameters of this circuit (Si BJT with $n = 2$, $\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations). Find the maximum amplitude of v_i for the circuit to work properly).

This is the PNP analog of circuit of Problem 2.

Bias summary: $I_E \approx I_C = 4$ mA, $I_B = 20$ μA, $V_{EC} = 5$ V

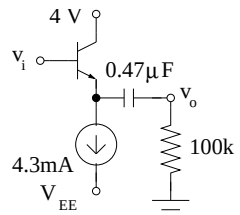
Small-Signal: $g_m = 7.69 \times 10^{-2}$ 1/Ω, $r_e = 13$ Ω, $r_\pi = 2.60$k, and $r_o = 38.8$ k.

Amp response: $A_v = 1$, $R_i = 9.9$ k, $R_o = 13$ Ω, and $f_l = f_{p1} + f_{p2} = 37$ Hz.

Max signal: $-4.3 < v_o = A_v v_i < 4.0 \quad \rightarrow \quad -4.3 < v_i < 4.0 \quad \rightarrow \quad V_i < 4.0$ V

Problem 6. Find the bias point and amplifier parameters of this circuit (Si BJT with $n = 2$, $\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations). Find the maximum amplitude of v_i for the circuit to work properly.

This circuit is similar to the circuit of Problem 3 except that the transistor is biased with a current source.

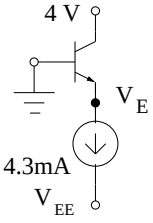


Bias: Set $v_i = 0$ and capacitors open.

$$I_E = 4.3 \text{ mA} \approx I_C, \qquad I_B = \frac{I_C}{\beta} = 21.5 \text{ } \mu\text{A}$$

$$\text{BE-KVL:} \quad 0 = V_{BE} + V_E \quad \rightarrow \quad V_E = -0.7 \text{ V}$$

$$\text{CE-KVL:} \quad 4 = V_{CE} + V_E \quad \rightarrow \quad V_{CE} = 4.7 \text{ V}$$

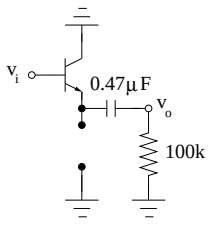


Bias summary: $I_E \approx I_C = 4.3$ mA, $I_B = 21.5$ μA, $V_{CE} = 4.7$ V

Small-Signal: First we calculate the small-signal parameters:

$$g_m = \frac{I_C}{nV_T} = \frac{4.3\times10^{-3}}{2\times26\times10^{-3}} = 8.27\times10^{-2} \qquad r_e = \frac{1}{g_m} = 12.1\ \Omega$$

$$r_\pi = \frac{\beta}{g_m} = 2.42\ \text{k} \qquad r_o = \frac{V_A + V_{CE}}{I_C} = \frac{150+5}{4.3\times10^{-3}} = 36.0\ \text{k}$$



Amplifier Response: we zero bias sources (the current source becomes an open circuit. As the input is at the base and output is at the emitter, this is a common-collector amplifier (emitter follower) with $R_E \to \infty$. Using formulas of page 5-21 and noting $R_E \parallel R_L = R_L \gg r_e$

$$A_v = \frac{R_E \parallel R_L}{R_E \parallel R_L + r_e} = \frac{R_L}{R_L + r_e} \approx 1$$

$$R_i = R_B \parallel [r_\pi + (1+\beta)R_E] \to \infty \qquad R_o = r_e = 12\ \Omega$$

$$f_l = f_{p2} = \frac{1}{2\pi C_{c2}(R_L + R_E \parallel r_e)} \approx \frac{1}{2\pi C_{c2}(R_L + r_e)} \approx \frac{1}{2\pi C_{c2}R_L} = 3.4\ \text{Hz}$$

BJT is in active if $i_C \approx i_E > 0$ and $v_{CE} > V_{D0}$. The current source makes the problem slightly complicated (i_e flows through the 100 k resistor while I_E is fed by the current source). As such, CE-KVL degenerates into two equations, one for small signal and one for biasing:

CE-KVL (SS) $\quad 0 = v_{ce} + 10^5 i_e \quad$ and $\quad v_{CE} = V_{CE} + v_{ce} > V_{D0} = 0.7$

$$v_{ce} = -10^5 i_e > 0.7 - V_{CE} = -4.0\ \text{V} \quad \to \quad v_o = 10^5 i_e < 4.0\ \text{V}$$

$$i_E = I_E + i_e > 0 \quad \to \quad i_e > -I_E = -4.3\ \text{mA} \quad \to \quad v_o = 10^5 i_e > -430\ \text{V}$$

$$-430 < v_o = A_v v_i < 4.0\ \text{V} \quad \to \quad -430 < v_i < 4\ \text{V} \quad \to \quad V_i < 4.0\ \text{V}$$

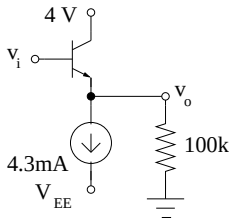
Note that the above limit is correct ONLY for an ideal current source (that is why the lower limit for v_i is so large). In practical applications, the current source will impose a condition on v_E (*e.g.,* minimum voltage on the collector of a current mirror).

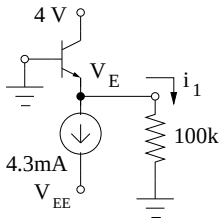
Problem 7. Find the bias point and amplifier parameters of this circuit (Si BJT with $n = 2$, $\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations). Find the maximum amplitude of v_i for the circuit to work properly.

This circuit is similar to the circuit of Problem 6 except that C_{c2} is removed.

Bias: Set $v_i = 0$ and capacitors open.

BE-KVL: $\quad 0 = V_{BE} + V_E \quad \to \quad V_E = -0.7\ \text{V}$





$$i_1 = \frac{V_E}{100 \times 10^3} = -7\ \mu\text{A}$$

KCL $\quad I_E = 3 \times 10^{-3} + i_1 \approx 3\ \text{mA}$

$$I_E = 3\ \text{mA} \approx I_C, \qquad I_B = \frac{I_C}{\beta} = 15\ \mu\text{A}$$

CE-KVL: $\quad 4 = V_{CE} + V_E \quad \rightarrow \quad V_{CE} = 4.7\ \text{V}$

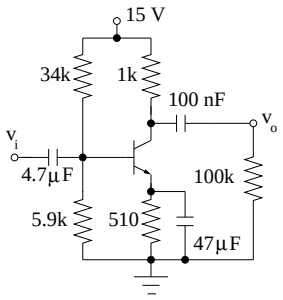
Bias summary: $I_E \approx I_C = 4.3$ mA, $I_B = 21.5\ \mu$A, $V_{CE} = 4.7$ V which is the exactly the same as of that of Problem 6.

The small-signal, amplifier parameters, and maximum v_o and v_i are exactly the same as those of Problem 6 expect $f_l = 0$ (*i.e.,* this amplifier can amplify DC signals).

Problem 8. Find the bias point and amplifier parameters of this circuit (Si BJT with $n = 2$, $\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations). Find the maximum amplitude of v_i for the circuit to work properly.

Bias:

Set $v_i = 0$ and capacitors open.
Replace R_1 and R_2 with their Thevenin equivalent:

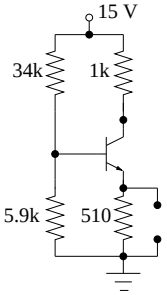


$$R_B = 5.9\ \text{k} \parallel 34\ \text{k} = 5.0\ \text{k},$$

$$V_{BB} = \frac{5.9}{5.9 + 34} \times 15 = 2.22\ \text{V}$$

BE-KVL: $\quad V_{BB} = R_B I_B + V_{BE} + 510 I_E \qquad I_B = \dfrac{I_E}{1+\beta} = \dfrac{I_E}{201}$

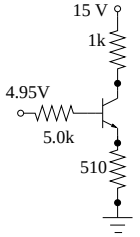
$$2.22 - 0.7 = I_E \left(\frac{5.0 \times 10^3}{201} + 510 \right)$$



$$I_E = 3\ \text{mA} \approx I_C, \qquad I_B = \frac{I_C}{\beta} = 15\ \mu\text{A}$$

CE-KVL: $\quad V_{CC} = 1000 I_C + V_{CE} + 510 I_E$

$$V_{CE} = 15 - 1,510 \times 3 \times 10^{-3} = 10.5\ \text{V}$$



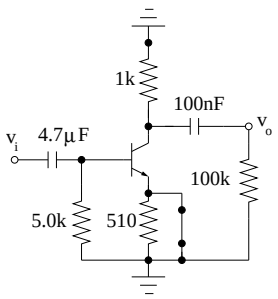
Bias summary: $I_E \approx I_C = 3$ mA, $I_B = 15\ \mu$A, $V_{CE} = 10.5$ V

Small-Signal: First we calculate the small-signal parameters:

$$g_m = \frac{I_C}{nV_T} = \frac{3 \times 10^{-3}}{2 \times 26 \times 10^{-3}} = 5.77 \times 10^{-2} \qquad r_e = \frac{1}{g_m} = 17.3\ \Omega$$

$$r_\pi = \frac{\beta}{g_m} = 3.47\ \text{k} \qquad r_o = \frac{V_A + V_{CE}}{I_C} = \frac{150 + 10.5}{3 \times 10^{-3}} = 53.5\ \text{k}$$

Proceeding with the small signal analysis, we zero bias sources (see circuit). As the input is at the base and output is at the collector, this is a common-emitter amplifier (with NO emitter resistor). Using formulas of page 5-21 and noting $R_C \ll R_L$, $R_C \ll r_o$, $R_E \gg r_e$, and $R_{sig} = 0$:



$$A_v = -\frac{r_o \parallel R_C \parallel R_L}{r_e} \approx -\frac{R_C}{r_e} = -58$$

$$R_i = R_B \parallel r_\pi = 5.0 \parallel 3.47 = 2.05 \text{ k}$$

$$R_{out} = R_o = r_o = 53.5 \text{ k}$$

$$f_{p1} = \frac{1}{2\pi C_{c1}(R_i + R_{sig})} = \frac{1}{2\pi \times 4.7 \times 10^{-6} \times 2.05 \times 10^3} = 16.5 \text{ Hz}$$

$$f_{p2} = \frac{1}{2\pi C_{c2}(R_L + R_C \parallel R_{out})} \approx \frac{1}{2\pi C_{c2}(R_L + R_c)} \approx \frac{1}{2\pi C_{c2} R_L} = 15.9 \text{ Hz}$$

$$f_{pb} = \frac{1}{2\pi C_b[R_E \parallel (r_e + (R_B \parallel R_{sig})/\beta)]} = \frac{1}{2\pi C_b[R_E \parallel 17.3]} = 202 \text{ Hz}$$

$$f_l = f_{p1} + f_{p2} + f_{pb} = 16.5 + 15.9 + 202 = 235 \text{ Hz}$$

To find the maximum amplitude for v_i, we note that $v_o = i_c R_C = 10^3 i_c$ (as $R_L \gg R_C$):

$$\text{CE-KVL} \quad 15 = 10^3(I_C + i_C) + v_{CE} + 510 I_E$$

As i_e does not flow in the $R_E = 510\ \Omega$ resistor because of the 47 μF by-pass capacitor,

$$\text{CE-KVL} \quad v_{CE} = 15 - 1,510 I_C - 10^3 i_c = 10.5 - 10^3 i_c$$

$$v_{CE} > V_{D0} = 0.7 \quad \rightarrow \quad i_c < 9.8 \text{ mA} \quad \rightarrow \quad v_o = 10^3 i_c < 9.8 \text{ V}$$

$$i_C = I_C + i_c > 0 \quad \rightarrow \quad i_c > -I_C = -3 \text{ mA} \quad \rightarrow \quad v_o = 10^3 i_c > -3 \text{ V}$$

$$-3 < v_o = -58 v_i < 9.8 \text{ V} \quad \rightarrow \quad -0.17 < v_i < 0.052 \text{ V}$$

Problem 9. Find the bias point and amplifier parameters of this circuit (Si BJT with $n = 2$, $\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations). Find the maximum amplitude of v_i for the circuit to work properly.

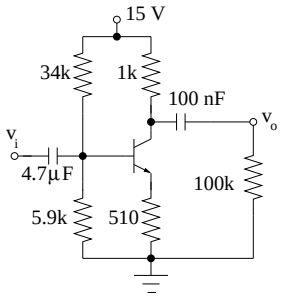
This is the PNP analog of circuit of Problem 8.

Bias summary: $I_E \approx I_C = 3$ mA, $I_B = 15\ \mu$A, $V_{EC} = 10.5$ V

Small-Signal: $g_m = 5.77 \times 10^{-2}\ 1/\Omega$, $r_e = 17.3\ \Omega$. $r_\pi = 3.47$k, and $r_o = 53.5$ k.

Amp response: $A_v = -58$, $R_i = 2.05$ k, $R_o = 53.5$ k, and $f_l = f_{p1} + f_{p2} + f_{pb} = 113$ Hz.

Problem 10. Find the bias point and amplifier parameters of this circuit (Si BJT with $n = 2$, $\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations). Find the maximum amplitude of v_i for the circuit to work properly.

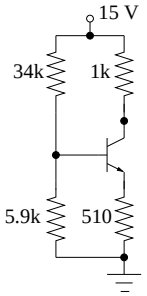


Bias:

Set $v_i = 0$ and capacitors open. The bias circuit is exactly that of Problem 8 with $R_B = 5.0$ k.

Bias summary: $I_E \approx I_C = 3$ mA, $I_B = 15$ μA, $V_{CE} = 10.5$ V.

Small-Signal: The small-signal parameters are also the same as those of Problem 8: $g_m = 5.77 \times 10^{-2}$ 1/Ω, $r_e = 17.3$ Ω. $r_\pi = 3.47$k, and $r_o = 53.5$ k.



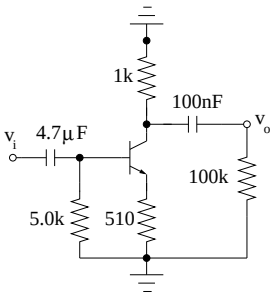
Proceeding with the small signal analysis, we zero bias sources (see circuit). As the input is at the base and output is at the collector, this is a degenerated common-emitter amplifier (*i.e,* with a emitter resistor). Using formulas of page 5-21 and noting $R_C \ll R_L$, $R_C \ll r_o$, and $R_E \gg r_e$:

$$A_v = -\frac{R_C \parallel R_L}{R_E + r_e} \approx -\frac{R_C}{R_E + r_e} = 1.90$$

$$R_i = R_B \parallel [r_\pi + (1+\beta)R_E] \approx R_B \parallel [(1+\beta)R_E] \approx R_B = 5.0 \text{ k}$$

$$R_o = r_o[1 + g_m(R_E \parallel r_\pi)] = r_o[1 + 5.77 \times 10^{-2}(510 \parallel 3,470)]$$
$$= 53.5 \times 10^3 \times 26.7 = 1.4 \text{ M}$$

$$R_{out} = r_o\left(1 + \frac{\beta R_E}{r_\pi + R_E + R_B \parallel R_{sig}}\right) = 26.6 r_o = 1.4 \text{ M}$$



$$f_{p1} = \frac{1}{2\pi C_{c1}(R_i + R_{sig})} = \frac{1}{2\pi \times 4.7 \times 10^{-6} \times 5.0 \times 10^3} = 6.8 \text{ Hz}$$

$$f_{p2} = \frac{1}{2\pi C_{c2}(R_L + R_C \parallel R_{out})} \approx \frac{1}{2\pi C_{c2}(R_L + R_c)} \approx \frac{1}{2\pi C_{c2} R_L} = 15.9 \text{ Hz}$$

$$f_l = f_{p1} + f_{p2} = 6.8 + 15.9 = 23 \text{ Hz}$$

To find the maximum amplitude for v_i, we need to find i_c as $v_o = i_c R_C = 10^3 i_c$ (as $R_L \gg R_C$). Then, (note compared to Problem 8, i_e now flows in the $R_E = 510$ Ω resistor:)

CE-KVL $\quad 15 = 10^3(I_C + i_C) + v_{CE} + 510(I_E + i_e)$

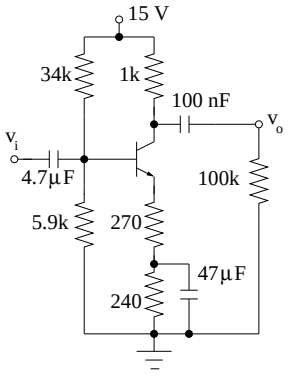
$$v_{CE} = 15 - 1,510 I_C - 1,510 i_c = 10.5 - 1,510 i_c$$

$$v_{CE} > V_{D0} = 0.7 \quad \rightarrow \quad i_c < 6.5 \text{ mA} \quad \rightarrow \quad v_o = 10^3 i_c < 6.5 \text{ V}$$

$$i_C = I_C + i_c > 0 \quad \rightarrow \quad i_c > -I_C = -3 \text{ mA} \quad \rightarrow \quad v_o = 10^3 i_c > -3 \text{ V}$$

$$-3 < v_o = -1.9 v_i < 6.5 \text{ V} \quad \rightarrow \quad -3.42 < v_i < 1.58 \text{ V}$$

Problem 11. Find the bias point and amplifier parameters of this circuit (Si BJT with $n = 2$, $\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations). Find the maximum amplitude of v_i for the circuit to work properly.

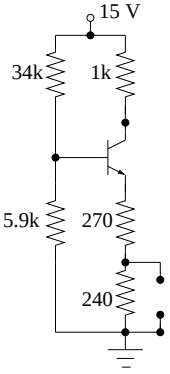


Bias:

Set $v_i = 0$ and capacitors open. Because the 47 μF capacitor across the 240 Ω resistor becomes an open circuit, the total R_E for bias is $270 + 240 = 510$ Ω and the bias circuit is exactly that of Problem 8 with $R_B = 5.0$ k.

Bias summary: $I_E \approx I_C = 3$ mA, $I_B = 15$ μA, $V_{CE} = 10.5$ V.

Small-Signal: The small-signal parameters are also the same as those of Problem 8: $g_m = 5.77 \times 10^{-2}$ $1/\Omega$, $r_e = 17.3$ Ω. $r_\pi = 3.47$k, and $r_o = 53.5$ k.



Proceeding with the small signal analysis, we zero bias sources (see circuit). In this case, the 47 μF capacitor across the 240 Ω resistor becomes a short circuit and the total R_E for small-signal is 270 Ω. As the input is at the base and output is at the collector, this is a degenerated common-emitter amplifier (*i.e,* with a emitter resistor). Using formulas of page 5-21 and noting $R_C \ll R_L$, $R_C \ll r_o$, and $R_E \gg r_e$:

$$A_v = -\frac{R_C \parallel R_L}{R_E + r_e} \approx -\frac{R_C}{R_E + r_e} = -3.48$$

$$R_i = R_B \parallel [r_\pi + (1+\beta)R_E] \approx R_B \parallel [(1+\beta)R_E] \approx R_B = 5.0 \text{ k}$$

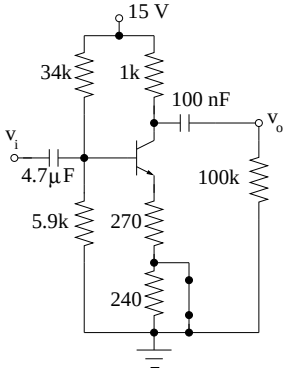
$$R_o = r_o[1 + g_m(R_E \parallel r_\pi)] = r_o[1 + 5.77 \times 10^{-2}(270 \parallel 3,470)]$$

$$= 53.5 \times 10^3 \times 15.5 = 830 \text{ k}$$

$$R_{out} = r_o\left(1 + \frac{\beta R_E}{r_\pi + R_E + R_B \parallel R_{sig}}\right) = 15.4 r_o = 826 \text{ k}$$

$$f_{p1} = \frac{1}{2\pi C_{c1}(R_i + R_{sig})} = \frac{1}{2\pi \times 4.7 \times 10^{-6} \times 5.0 \times 10^3} = 6.8 \text{ Hz}$$

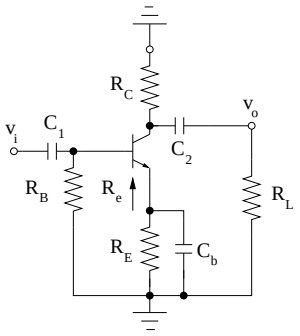
$$f_{p2} = \frac{1}{2\pi C_{c2}(R_L + R_C \parallel R_{out})} \approx \frac{1}{2\pi C_{c2}(R_L + R_c)} \approx \frac{1}{2\pi C_{c2} R_L} = 15.9 \text{ Hz}$$



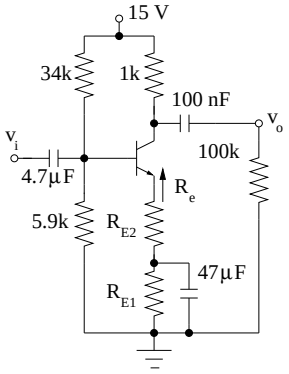
We need to find the pole introduced by the 47 μF by-pass capacitor, f_{pb}. Although this configuration was not included in the formulas for BJT elementary configuration of page 5-21, we can extend those formulas to cover this case.

The pole introduced by the by-pass capacitor in the common emitter case is (see figure)

$$f_{pb} = \frac{1}{2\pi C_b[R_E \parallel (r_e + (R_B \parallel R_{sig})/\beta)]}$$



Per our discussion of page 5-19 on how to find poles introduced by each capacitor, $R_E \parallel (r_e + (R_B \parallel R_{sig})/\beta)]$ is the total resistance seen across the terminal of C_b. As can be seen from the circuit, the resistance across C_b terminals consists of two resistors in parallel, R_E and R_e, the resistance seen through the emitter of the BJT: $R_e \equiv r_e + (R_B \parallel R_{sig})/\beta)$ from the formula above.



For the circuit here (defined $R_{E1} = 240\ \Omega$ and $R_{E2} = 270\ \Omega$), the resistance across C_b is made of two resistances in parallel: R_{E1} and the combination of R_{E2} and R_e, the resistance seen through the emitter of BJT in series. Thus:

$$f_{pb} = \frac{1}{2\pi C_b[R_{E1} \parallel (R_{E2} + r_e + (R_B \parallel R_{sig})/\beta)]}$$

$$f_{pb} = \frac{1}{2\pi C_b[240 \parallel (270 + 17]} = \frac{1}{2\pi \times 47 \times 10^{-6} \times 131} = 25.8 \text{ Hz}$$

$$f_l = f_{p1} + f_{p2} = 6.8 + 15.9 + 25.8 = 48.5 \text{ Hz}$$

To find the maximum amplitude for v_i, we need to find i_c as $v_o = i_c R_C = 10^3 i_c$ (as $R_L \gg R_C$). Then, (note i_e now flows in 270 Ω resistor while I_E flows in a 510 Ω resistor):

CE-KVL $\quad 15 = 10^3(I_C + i_C) + v_{CE} + 510 I_E + 270 i_e$

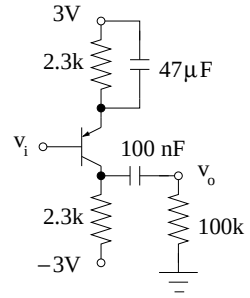
$$v_{CE} = 15 - 1,510 I_C - 1,270 i_c = 10.5 - 1,270 i_c$$

$$v_{CE} > V_{D0} = 0.7 \quad \rightarrow \quad i_c < 7.7 \text{ mA} \quad \rightarrow \quad v_o = 10^3 i_c < 7.7 \text{ V}$$

$$i_C = I_C + i_c > 0 \quad \rightarrow \quad i_c > -I_C = -3 \text{ mA} \quad \rightarrow \quad v_o = 10^3 i_c > -3 \text{ V}$$

$$-3 < v_o = -3.5 v_i < 7.7 \text{ V} \quad \rightarrow \quad -2.2 < v_i < 0.86 \text{ V}$$

Problem 12. Find the bias point and amplifier parameters of this circuit (Si BJT with $n = 2$, $\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations). Find the maximum amplitude of v_i for the circuit to work properly.



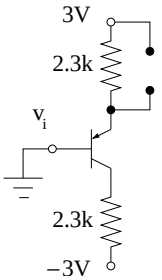
Bias: Set $v_i = 0$ and capacitors open.

BE-KVL: $3 = 2.3I_E + V_{EB}$

$$I_E = 1 \text{ mA} \approx I_C, I_B = \frac{I_E}{1+\beta} = 5\ \mu\text{A}$$

CE-KVL: $3 = 2.3 \times 10^3 I_E + V_{EC} + 2.3 \times 10^3 I_C - 3$

$$V_{EC} = 6 - 4.6 \times 10^3 \times 1 \times 10^{-3} = 1.4 \text{ V}$$



Bias summary: $I_E \approx I_C = 1$ mA, $I_B = 50\ \mu$A, $V_{CE} = 1.4$ V

Small-Signal: First we calculate the small-signal parameters:

$$g_m = \frac{I_C}{nV_T} = \frac{1 \times 10^{-3}}{2 \times 26 \times 10^{-3}} = 1.92 \times 10^{-2} \qquad r_e = \frac{1}{g_m} = 52\ \Omega$$

$$r_\pi = \frac{\beta}{g_m} = 10.4 \text{ k} \qquad r_o = \frac{V_A + V_{CE}}{I_C} = \frac{150 + 1.4}{1 \times 10^{-3}} = 151 \text{ k}$$

Proceeding with the small signal analysis, we zero bias sources. As the input is at the base and output is at the collector, this is a common-emitter amplifier. It does not have an emitter resistor as 47 μF capacitor shorts out R_E for small signals. Using formulas of page 5-21 and noting $R_C \ll R_L$, $R_C \ll r_o$, and $R_E \gg r_e$:

$$A_v = -\frac{r_o \parallel R_C \parallel R_L}{r_e} \approx -\frac{R_C}{r_e} = -44.2$$

$$R_i = R_B \parallel r_\pi = 10.4 \text{ k}$$

$$R_{out} = R_o = r_o = 151 \text{ k}$$

$$f_{p1} = 0$$

$$f_{p2} = \frac{1}{2\pi C_{c2}(R_L + R_C \parallel R_{out})} \approx \frac{1}{2\pi C_{c2}(R_L + R_c)} = 15.9 \text{ Hz}$$

$$f_{pb} = \frac{1}{2\pi C_b[R_E \parallel (r_e + (R_B \parallel R_{sig})/\beta)]} = \frac{1}{2\pi C_b[R_E \parallel 52]} = 66.6\text{Hz}$$

$$f_l = f_{p1} + f_{p2} + f_{pb} = 0 + 15.9 + 66.6 = 82.5 \text{ Hz}$$

To find the maximum amplitude for v_i, we need to find i_c as $v_o = i_c R_C = 2.7 \times 10^3 i_c$ (as $R_L \gg R_C$). Then, (note only I_E flows in $R_E = 2.3$ k resistor):

CE-KVL $\quad 3 = 2.3 \times 10^3 (I_C + i_C) + v_{CE} + 2.3 \times 10^3 I_E - 3$

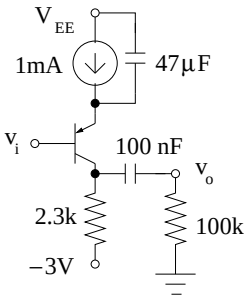
$$v_{CE} = 6 - 4.6 \times 10^3 I_C - 2.3 \times 10^3 i_c = 1.4 - 2.3 \times 10^3 i_c$$

$$v_{CE} > V_{D0} = 0.7 \quad \rightarrow \quad i_c < 0.3 \text{ mA} \quad \rightarrow \quad v_o = 2.3 \times 10^3 i_c < 0.7 \text{ V}$$

$$i_C = I_C + i_c > 0 \quad \rightarrow \quad i_c > -I_C = -1 \text{ mA} \quad \rightarrow \quad v_o = 2.3 \times 10^3 i_c > -2.3 \text{ V}$$

$$-2.3 < v_o = -44.2 v_i < 0.7 \text{ V} \quad \rightarrow \quad -0.016 < v_i < 0.052 \text{ V}$$

Problem 13. Find the bias point and amplifier parameters of this circuit (Si BJT with $n = 2$, $\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations). Find the maximum amplitude of v_i for the circuit to work properly.



This is the same circuit as that of Problem 13 expect that the transistor is biased with a current source

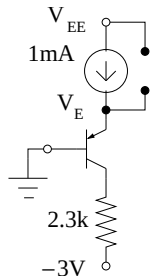
Bias: Set $v_i = 0$ and capacitors open. From the circuit $I_E = 1$ mA

$$I_E = 1 \text{ mA} \approx I_C, \qquad I_B = \frac{I_C}{\beta} = 5 \ \mu\text{A}$$

BE-KVL: $\quad V_E = V_{EB} = 0.7$ V

CE-KVL: $\quad V_E = V_{CE} + 2.3 \times 10^3 I_C - 3 = V_{CE} - 0.7$

$$V_{CE} = 1.4 \text{ V}$$



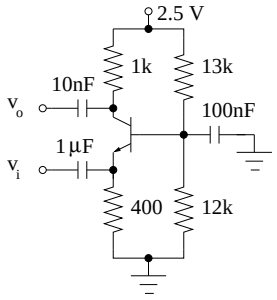
Bias summary: $\quad I_E \approx I_C = 1$ mA, $\quad I_B = 50 \ \mu$A, $\quad V_{CE} = 1.4$ V.

Small-Signal: As the bias point is exactly the same as that of problem 12, we have: $\quad g_m = 1.92 \times 10^{-2}$ 1/Ω, $r_e = 52$ Ω, $r_\pi = 10.4$k, and $r_o = 151$ k.

Amplifier response: The only difference with problem 12 is that $R_E \rightarrow \infty$ in this circuit: $A_v = -44.2$, $R_i = 10.4$ k, $R_o = 151$ k, and $f_l = 0 + 15.9 + 66.6 = 82.5$ Hz.

Maximum amplitude for v_i: note only I_E flows in the current source while i_e flows through the by-pass capacitor. As such, the results are similar to those of problem 12: $-2.3 < v_o = -44.2 v_i < 0.7$ V or $-0.016 < v_i < 0.052$ V.

Problem 14. Find the bias point and amplifier parameters of this circuit (Si BJT with $n = 2$, $\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations). Find the maximum amplitude of v_i for the circuit to work properly.



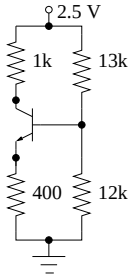
Bias: Set $v_i = 0$ and capacitors open.

$$R_B = 12 \text{ k} \parallel 13 \text{ k} = 6.24 \text{ k},$$

$$V_{BB} = \frac{12}{12+13} \times 2.5 = 1.2 \text{ V}$$

BE-KVL: $V_{BB} = R_B I_B + V_{BE} + 510 I_E \qquad I_B = \dfrac{I_E}{1+\beta} = \dfrac{I_E}{201}$

$$1.2 - 0.7 = I_E \left(\frac{6.24 \times 10^3}{201} + 400 \right)$$



$$I_E = 1.16 \text{ mA} \approx I_C, \qquad I_B = \frac{I_C}{\beta} = 5.8 \ \mu\text{A}$$

CE-KVL: $2.5 = 1000 I_C + V_{CE} + 400 I_E$

$$V_{CE} = 2.5 - 1,400 \times 1.16 \times 10^{-3} = 0.88 \text{ V}$$

Bias summary: $I_E \approx I_C = 1.16$ mA, $\quad I_B = 5.8$ μA, $\quad V_{CE} = 0.88$ V

Small-Signal: First we calculate the small-signal parameters:

$$g_m = \frac{I_C}{nV_T} = \frac{1.16 \times 10^{-3}}{2 \times 26 \times 10^{-3}} = 2.23 \times 10^{-2} \qquad r_e = \frac{1}{g_m} = 44.8 \ \Omega$$

$$r_\pi = \frac{\beta}{g_m} = 8.97 \text{ k} \qquad r_o = \frac{V_A + V_{CE}}{I_C} = \frac{150 + 0.88}{1.16 \times 10^{-3}} = 129 \text{ k}$$

Proceeding with the small signal analysis, we zero bias sources. As the input is at the emitter and output is at the collector, this is a common-base amplifier. Using formulas of page 5-21 and noting $R_L \to \infty$, and $R_C \ll r_o$:

$$A_v = g_m(r_o \parallel R_C \parallel R_L) \approx g_m R_C = 22.3$$

$$R_i = R_E \parallel r_\pi \parallel [1/g_m + (R_C \parallel R_L)/(g_m r_o)] \approx R_E \parallel r_\pi \parallel (1/g_m)$$

$$R_i = 400 \parallel 8,970 \parallel 44.8 \approx 400 \parallel 44.8 = 40.3 \ \Omega \qquad R_o = r_o = 129 \text{ k}$$

$$R_{out} = r_o \left(1 + \frac{\beta R_E}{r_\pi + R_E + R_B \parallel R_{sig}} \right)$$

$$R_{out} = r_o[1 + 200 \times 400/(8,970 + 400)] = 9.54 r_o = 1.2 \text{ M}$$

$$f_{p1} = 1/[2\pi C_{c1}(R_i + R_{sig})] = 3.95 \text{ kHz}$$

$$f_{p2} = \frac{1}{2\pi C_{c2}(R_L + R_C \parallel R_{out})} = 0$$

$$R_{CB} \equiv R_B \parallel [r_\pi + (1+\beta)(R_{sig} \parallel R_E)] = 6.24 \text{ k} \parallel 8.97 \text{ k} \approx 3.68 \text{ k}$$

$$f_{pb} = \frac{1}{2\pi C_b R_{CB}} = 432 \text{ Hz}$$

$$f_l = f_{p1} + f_{p2} + f_{pb} = 3,950 + 0 + 432 = 4.38 \text{ kHz}$$

Note the small input resistance of this amplifier and corresponding large f_{p1}.

To find the maximum amplitude for v_i, we need to find i_c as $v_o = i_c R_C = 10^3 i_c$ (as $R_L \gg R_C$):

CE-KVL $\quad 2.5 = 10^3(I_C + i_C) + v_{CE} + 400(I_E + i_e)$

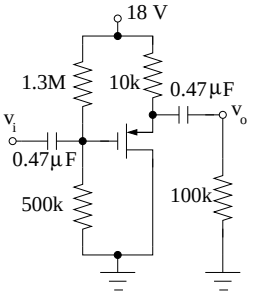
$$v_{CE} = 2.5 - 1,400 I_C - 1,400 i_c = 0.88 - 1,400 i_c$$

$$v_{CE} > V_{D0} = 0.7 \quad \rightarrow \quad i_c < 0.13 \text{ mA} \quad \rightarrow \quad v_o = 10^3 i_c < 0.18 \text{ V}$$

$$i_C = I_C + i_c > 0 \quad \rightarrow \quad i_c > -I_C = -1.16 \text{ mA} \quad \rightarrow \quad v_o = 10^3 i_c > -1.16 \text{ V}$$

$$-1.16 < v_o = 22.3 v_i < 0.18 \text{ V} \quad \rightarrow \quad -52 < v_i < 8 \text{ mV}$$

Problem 15. Find the bias point and amplifier parameters of this circuit ($V_{tp} = -4$ V, $k'_p(W/L) = 0.4$ mA/V^2, $\lambda = 0.01$ V^{-1}). Ignore the channel-width modulation effect in biasing calculations. Find the saturation voltages for this amplifier.



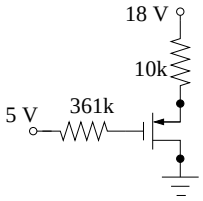
Replacing R_1/R_2 voltage divider with its Thevenin equivalent, we get:

$$R_G = 1.3 \text{ M} \parallel 500 \text{ k} = 361 \text{ k}, \qquad V_{GG} = \frac{0.5}{1.3 + 0.5} \times 18 = 5 \text{ V}$$

Assume PMOS is in the active state,

$$I_D = 0.5k'_n(W/L)(V_{SG} - |V_{tp}|)^2 = 0.5 \times 0.4 \times 10^{-3}(V_{SG} - 4)^2$$

SG-KVL: $\quad 18 = 10^4 I_D + V_{SG} + 5$



Substituting for I_D in SG-KVL, we get:

$$13 = V_{SG} + 2(V_{SG} - 4)^2 \quad \rightarrow \quad 2V_{SG}^2 - 15V_{SG} + 19 = 0$$

Two roots: -5.9 and -1.6. Since $V_{SG} = 1.6 < |V_{tp}| = 4$ V required for NMOS to be ON, this root is unphysical. So, $V_{SG} = 5.9$ V.

SG-KVL: $\quad 13 = V_{SG} + 10^4 I_D = 5.9 + 10^4 I_D \quad \rightarrow \quad I_D = 0.71$ mA

SD-KVL: $\quad 18 = V_{SD} + 10^4 I_D \quad \rightarrow \quad V_{SD} = 18 - 10^4 \times 0.71 \times 10^{-3} = 10.9$ V

Since $V_{SD} = 10.9 \geq V_{SG} - |V_{tp}| = 5.9 - 4 = 1.9$ V, our assumption of PMOS in active is justified.

Bias summary: $V_{SG} = 5.9$ V, $V_{SD} = 10.9$ V, and $I_D = 0.71$ mA.

Small-Signal: First we calculate the small-signal parameters ($V_A = 1/\lambda = 100$ V):

$$g_m = \frac{2I_D}{V_{SG} - |V_{tp}|} = \frac{2 \times 0.71 \times 10^{-3}}{5.9 - 4} = 7.47 \times 10^{-4}$$

$$r_o = \frac{V_A + V_{SD}}{I_D} = \frac{100 + 10.9}{0.71 \times 10^{-3}} = 156 \text{ k}$$

Proceeding with the small signal analysis, we zero bias sources. As the input is at the gate and output is at the source, this is a common-drain amplifier (source follower). Using

formulas of page 5-22 and noting $R_S \ll R_L$, and $R_S \ll r_o$:

$$A_v = \frac{g_m(R_S \parallel R_L)}{1 + g_m(R_S \parallel R_L)} \approx \frac{g_m R_S}{1 + g_m R_S} = \frac{7.47}{8.47} = 0.88$$

$$R_i = R_G = 361 \text{ k}$$

$$R_{out} = R_o \approx \frac{1}{g_m} = 1.34 \text{ k}$$

$$f_{p1} = 1/[2\pi C_{c1}(R_i + R_{sig})] = 0.94 \text{ Hz}$$

$$f_{p2} = 1/[2\pi C_{c2}(R_L + R_S \parallel R_{out})] \approx 1/[2\pi C_{c2} R_L] = 3.39 \text{ Hz}$$

$$f_l = f_{p1} + f_{p2} = 4.33 \text{ Hz}$$

PMOS remains in saturation as long as $i_D = i_S > 0$, $v_{SG} > V_{tp}|$, and $v_{SD} > v_{SG} - |V_{tp}|$. Similar to the BJT case, $i_S = I_S + i_s > 0$ gives the minimum value for i_s (or i_d) and one limit for v_o and v_i. For this problem that $v_o = -(R_S \parallel R_L)i_s = -(10^4 \parallel 10^5)i_s = 9.1 \times 10^3 i_s$ (You can ignore R_L in the above as $R_S \ll R_L$ and write $v_o \approx 10^4 R_L$. I have kept R_L to show its impact on saturation limits.)

$$i_S = I_S + i_s > 0 \quad \rightarrow \quad i_s > -I_S = -0.71 \text{ mA} \quad \rightarrow \quad v_o = -9.1 \times 10^3 i_s < 6.45 \text{ V}$$

Finding the second limit is more complicated than the comparable BJT case because the limit on v_{SD} depends on v_{SG} and v_i! We need to combine $v_{SD} > v_{SG} - |V_{tp}|$ with DS-KVL and GS-KVL to find a limit on v_i. Noting that the voltage at the gate of the transistor is the sum of v_i and the 5-V bias:

$$\text{DS-KVL} \qquad 18 = R_S I_S + (R_S \parallel R_L)i_s + v_{SD}$$

$$\text{GS-KVL} \qquad 18 = R_S I_S + (R_S \parallel R_L)i_s + v_{SG} + v_i + 5$$

$$v_{SD} = v_{SG} + v_i + 5 > v_{SG} - |V_{tp}| \quad \rightarrow \quad v_i > -5 - |V_{tp}| = -9 \text{ V}$$

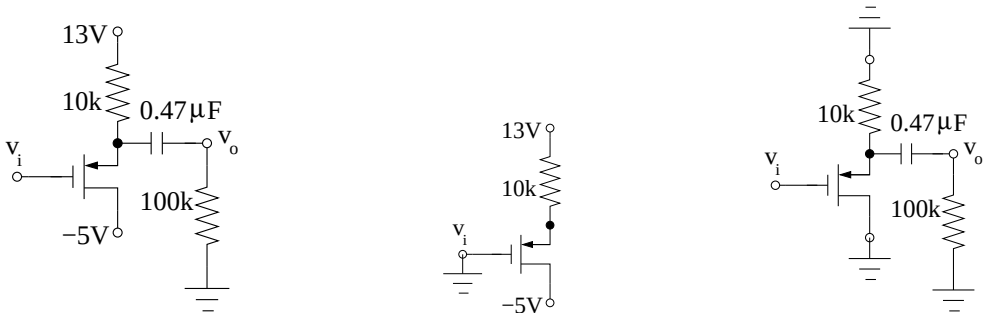
where the 3rd equation is found by summing DS-KVL and GS-KVL. Combining the two limits:

$$v_o = A_v v_i < 6.45 \text{ V} \quad \rightarrow \quad v_i < 7.33 \text{ V}$$

$$v_i = v_o/A_v > -9 \text{ V} \quad \rightarrow \quad v_o > -7.92 \text{ V}$$

Therefore, the limits for this amplifiers are $-9 < v_i < 7.33$ V and $-7.92 < v_o < 6.45$ V. The amplifier will saturate when v_o exceeds these values.

Problem 16. Find the bias point and amplifier parameters of this circuit ($V_{tp} = -4$ V, $k'_p(W/L) = 0.4$ mA/V^2, $\lambda = 0.01$ V^{-1}). Ignore the channel-width modulation effect in biasing calculations. Find the saturation voltages for this amplifier.



Bias Small-signal

This circuit is similar to that of problem 15 expect it is biased with two voltage sources. Note:

SG-KVL: $13 = 10^4 I_D + V_{SG}$

which is the same as that of Problem 16. Thus, we should get the Bias point and the same small-signal parameters:

Bias summary: $V_{SG} = 5.9$ V, $V_{SD} = 10.9$ V, and $I_D = 0.71$ mA.

Small-Signal: $g_m = 7.47 \times 10^{-4}$ $1/\Omega$ and $r_o = 156$ k.

For the amplifier response (see small-signal circuit above) $R_G \to \infty$ and C_{c1} is not present ($f_{l1} = 0$). Thus:

$$A_v = \frac{g_m(R_S \parallel R_L)}{1 + g_m(R_S \parallel R_L)} \approx \frac{g_m R_S}{1 + g_m R_S} = \frac{7.47}{8.47} = 0.88$$

$$R_i = R_G \to \infty$$

$$R_{out} = R_o \approx \frac{1}{g_m} = 1.34 \text{ k}$$

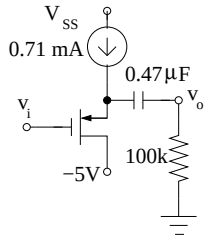
$$f_{p1} = 0$$

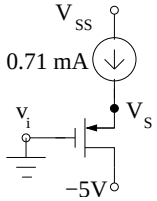
$$f_{p2} = 1/[2\pi C_{c2}(R_L + R_S \parallel R_{out})] \approx 1/[2\pi C_{c2} R_L] = 3.39 \text{ Hz}$$

$$f_l = f_{p1} + f_{p2} = 3.39 \text{ Hz}$$

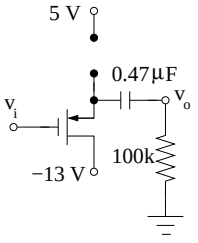
Saturation voltages are the same as those of problem 15 (Same bias, same A_v)

Problem 17. Find the bias point and amplifier parameters of this circuit ($V_{tp} = -4$ V, $k'_p(W/L) = 0.4$ mA/V^2, $\lambda = 0.01$ V^{-1}). Ignore the channel-width modulation effect in biasing calculations. Find the saturation voltages for this amplifier.





Bias



Small-signal

This circuit is also similar to that of problem 15 expect that it is biased with a current source:

$$\text{SD-KVL:} \quad 18 = V_{SD} + 10^4 I_D \quad \rightarrow \quad V_{SD} = 18 - 10^4 \times 0.71 \times 10^{-3} = 10.9 \text{ V}$$

$$0.71 \times 10^{-3} I_D = 0.5 k'_n (W/L)(V_{SG} - |V_{tp}|)^2 = 0.5 \times 0.4 \times 10^{-3}(V_{SG} - 4)^2$$

The second equation two roots for V_{SG}. Negative root is unphysical. So, $V_{SG} = 5.9$ V.

Bias summary: $V_{SG} = 5.9$ V, $V_{SD} = 10.9$ V, and $I_D = 0.71$ mA.

Since Bias values are the same as that of Problem 15, we should get the same small-signal parameters:

Small-Signal: $g_m = 7.47 \times 10^{-4}$ 1/Ω and $r_o = 156$ k.

For the amplifier response (see small-signal circuit above) $R_G \rightarrow \infty$, $R_s \rightarrow \infty$ and C_{c1} is not present ($f_{l1} = 0$). Thus:

$$A_v = \frac{g_m(R_S \parallel R_L)}{1 + g_m(R_S \parallel R_L)} = \frac{g_m R_L}{1 + g_m R_L} = 0.999$$

$$R_i = R_G \rightarrow \infty$$

$$R_{out} = R_o \approx \frac{1}{g_m} = 1.34 \text{ k}$$

$$f_{p1} = 0$$

$$f_{p2} = 1/[2\pi C_{c2}(R_L + R_S \parallel R_{out})] = 1/[2\pi C_{c2} R_L] = 3.39 \text{ Hz}$$

$$f_l = f_{p1} + f_{p2} = 3.39 \text{ Hz}$$

PMOS remains in saturation as long as $i_D = i_S > 0$, $v_{SG} > V_{tp}|$, and $v_{SD} > v_{SG} - |V_{tp}|$. Since $v_o = -(R_S \parallel R_L)i_s = -10^5 i_s$:

$$i_S = I_S + i_s > 0 \quad \rightarrow \quad i_s > -I_S = -0.71 \text{ mA} \quad \rightarrow \quad v_o = -10^5 i_s < 71 \text{ V}$$

Finding the second limit:

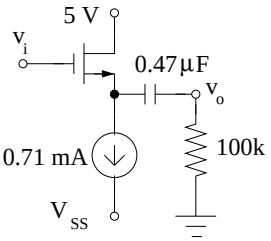
$$\begin{aligned}
&\text{DS-KVL} \quad && v_S = v_{SD} - 5 \\
&\text{GS-KVL} \quad && v_S = v_{SG} + v_i \\
& && v_{SD} + 5 = v_{SG} + v_i \quad \rightarrow \quad v_{SD} = v_{SG} + v_i + 5 \\
& && v_{SD} > v_{SG} - |V_{tp}| \quad \rightarrow \quad v_i > -5 - |V_{tp}| = -9 \text{ V}
\end{aligned}$$

where the 3rd equation is found by summing DS-KVL and GS-KVL. Combining the two limits:

$$\begin{aligned}
&v_o = A_v v_i < 71 \text{ V} \quad \rightarrow \quad v_i < 71 \text{ V} \\
&v_i = v_o / A_v > -9 \text{ V} \quad \rightarrow \quad v_o > -7.92 \text{ V}
\end{aligned}$$

Therefore, the limits for this amplifiers are $-9 < v_i < 71$ V and $-7.92 < v_o < 71$ V. The amplifier will saturate when v_o exceeds these values. The above values, of course, are for an IDEAL current source.

Problem 18. Find the bias point and amplifier parameters of this circuit ($V_{tn} = 3$ V, $k'_n(W/L) = 0.4$ mA/V^2, $\lambda = 0.01$ V^{-1}). Ignore the channel-width modulation effect in biasing calculations. Find the saturation voltages for this amplifier.



This is the NMOS version of problem 17. You should get the same answers:

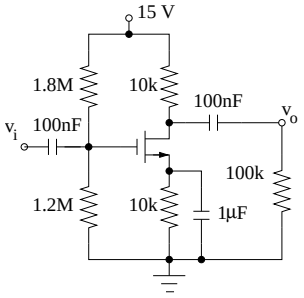
Bias summary: $V_{SG} = 5.9$ V, $V_{SD} = 10.9$ V, and $I_D = 0.71$ mA.

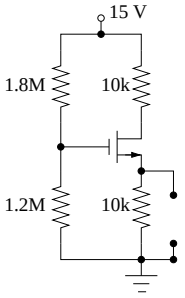
Small-Signal: $g_m = 7.47 \times 10^{-4}$ 1/Ω and $r_o = 156$ k.

Amp Response: $A_v = 0.999$, $R_i \rightarrow \infty$, $R_o = 1.34$ k, and $f_l = 3.39$ Hz.

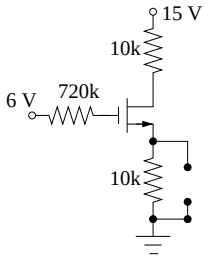
Saturation voltages: $-9 < v_i < 71$ V and $-7.92 < v_o < 71$ V.

Problem 19. Find the bias point and amplifier parameters of this circuit ($V_{tn} = 1$ V, $k'_n(W/L) = 0.8$ mA/V^2, $\lambda = 0.01$ V^{-1}). Ignore the channel-width modulation effect in biasing calculations. Find the saturation voltages for this amplifier.

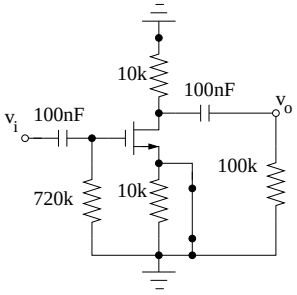




Bias



Bias



Small-signal

Bias: ($v_i = 0$ and capacitors open) Replacing R_1/R_2 voltage divider with its Thevenin equivalent:

$$R_G = 1.2 \text{ M} \parallel 1.8 \text{ M} = 720 \text{ k}, \qquad V_{GG} = \frac{1.2}{1.2 + 11.8} \times 15 = 6 \text{ V}$$

Assume NMOS is in the active state,

$$I_D = 0.5k'_n(W/L)(V_{GS} - V_{tn})^2 = 0.5 \times 0.8 \times 10^{-3}(V_{GS} - 1)^2$$

$$\text{GS-KVL:} \quad 6 = V_{GS} + 10^4 I_D = V_{GS} + 4(V_{GS} - 1)^2 \quad \rightarrow \quad 4V_{GS}^2 - 7V_{GS} - 2 = 0$$

Two roots: $+2$ and -0.25. As the negative root is unphysical, $V_{GS} = 2$.

$$\text{GS-KVL:} \quad 6 = 2 + 10^4 I_D \quad \rightarrow \quad I_D = 0.4 \text{ mA}$$

$$\text{DS-KVL:} \quad 15 = 10^4 I_D + V_{DS} + 10^4 I_D \quad \rightarrow \quad V_{DS} = 15 - 2 \times 10^4 \times 0.4 \times 10^{-3} = 7 \text{ V}$$

Since $V_{DS} = 7 \geq V_{GS} - V_{tn} = 2 - 1 = 12$ V, our assumption of NMOS in active state is justified.

Bias summary: $V_{GS} = 2$ V, $V_{DS} = 7$ V, and $I_D = 0.4$ mA

Small-Signal: First we calculate the small-signal parameters ($V_A = 1/\lambda = 100$ V):

$$g_m = \frac{2I_D}{V_{GS} - V_{tn}} = \frac{2 \times 0.4 \times 10^{-3}}{2 - 1} = 0.8 \times 10^{-3}$$

$$r_o = \frac{V_A + V_{DS}}{I_D} = \frac{100 + 7}{0.4 \times 10^{-3}} = 268 \text{ k}$$

Proceeding with the small signal analysis, we zero bias sources (see circuit). As the input is at the gate and output is at the collector, this is a common-source amplifier. There is no R_S because of the by-pass capacitor. Using formulas of page 5-22 and noting $R_D \ll R_L$, and $R_D \ll r_o$:

$$A_v = -g_m(r_o \parallel R_D \parallel R_L) \approx -g_m R_D = -8$$

$$R_i = R_G = 720 \text{ k} \qquad R_{out} = R_o = r_o = 268 \text{ k}$$

$$f_{p1} = 1/[2\pi C_{c1}(R_i + R_{sig})] = 2.21 \text{ Hz}$$

$$f_{p2} = 1/[2\pi C_{c2}(R_L + R_D \parallel R_{out})] \approx 1/[2\pi C_{c2}(R_L + R_D)] = 14.5 \text{ Hz}$$

$$f_{pb} = \frac{1}{2\pi C_b[R_S \parallel (1/g_m)]} = \frac{1}{2\pi C_b[10^4 \parallel 1.25 \times 10^3]} = \frac{1}{2\pi C_b \times 1.11 \times 10^3]} = 143 \text{ Hz}$$

$$f_l = f_{p1} + f_{p2} + f_{pb} = 2.21 + 14.5 + 143 = 160 \text{ Hz}$$

NMOS remains in saturation as long as $i_D = i_S > 0$, $v_{GS} > V_{tn}$, and $v_{DS} > v_{GS} - V_{tn}$. For this problem that $v_o = +(R_D \parallel R_L)i_d = (10^4 \parallel 10^5)i_d = 9.1 \times 10^3 i_d$:

$$i_D = I_D + i_d > 0 \quad \rightarrow \quad i_d > -I_D = -0.4 \text{ mA} \quad \rightarrow \quad v_o = 9.1 \times 10^3 i_d > -3.64 \text{ V}$$

Since the voltage at the gate of the transistor is the sum of v_i and the 6-V bias:

$$\text{DS-KVL} \qquad 15 = R_D I_D + (R_D \parallel R_L)i_d + v_{DS} + R_S I_S$$

$$\text{GS-KVL} \qquad 6 + v_i = v_{GS} + R_S I_S$$

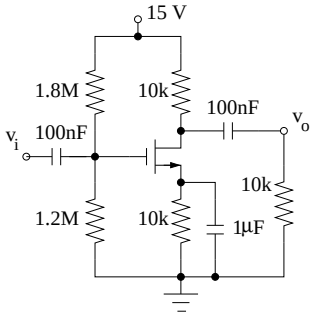
$$9 - v_i = R_D I_D + v_o + v_{DS} - v_{GS} \quad \rightarrow \quad v_{DS} - v_{GS} = 9 - 4 - v_i - v_o$$

$$v_{DS} - v_{GS} > V_{tn} = 1 \quad \rightarrow \quad v_i + v_o = v_o(1 + 1/A_v) < 6$$

$$(1 - 1/8)v_o < 6 \quad \rightarrow \quad v_o < 6.86 \text{ V}$$

where the 3rd equation is found by subtracting GS-KVL from GS-KVL. Therefore, the limits for this amplifiers are $-3.64 < v_o < 6.86$ V and $-0.86 < v_i = -v_o/8 < 0.46$ V. The amplifier will saturate when v_o exceeds the above values.

Problem 20. Find the bias point and amplifier parameters of this circuit ($V_{tn} = 1$ V, $k'_n(W/L) = 0.8$ mA/V^2, $\lambda = 0.01$ V^{-1}). Ignore the channel-width modulation effect in biasing calculations. Find the saturation voltages for this amplifier.



This is the same circuit as that of Problem 20 except that $R_L = 10$ k (instead of 100 k). As R_L in this circuit does not affect the bias points, we can use results from Problem 20:

Bias summary: $V_{GS} = 2$ V, $V_{DS} = 7$ V, and $I_D = 0.4$ mA

Small-Signal parameters: $g_m = 0.8 \times 10^{-3}$ and $r_o = 268$ k.

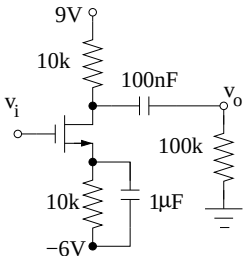
Amp. Response: $A_v = -4$, $R_i = 720$ k, $R_{out} = R_o = 268$ k, $f_{p1} = 2.21$ Hz, $f_{p2} = 7.25$ Hz, $f_{pb} = 143$ Hz, and $f_l = 152.5$ Hz. (Only A_v and f_{p2} depend on R_L)

Saturation voltage: limits on v_o does not on R_L (understand why). Thus, $-3.64 < v_o < 6.86$ V and $-1.72 < v_i = -v_o/4 < 0.92$ V.

Problem 21. Find the bias point and amplifier parameters of this circuit ($V_{tp} = -1$ V, $k'_p(W/L) = 0.8$ mA/V^2, $\lambda = 0.01$ V^{-1}). Ignore the channel-width modulation effect in biasing calculations. Find the saturation voltages for this amplifier.

This is the PMOS version of Problem 19.

Problem 22. Find the bias point and amplifier parameters of this circuit ($V_{tn} = 1$ V, $k'_n(W/L) = 0.8$ mA/V^2, $\lambda = 0.01$ V^{-1}). Ignore the channel-width modulation effect in biasing calculations. Find the saturation voltages for this amplifier.



This is the same circuit as that of Problem 19 except that is biased with two voltage sources (and $R_G \to \infty$).

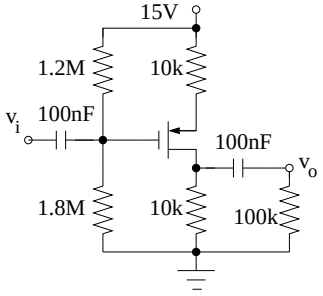
Bias summary: $V_{GS} = 2$ V, $V_{DS} = 7$ V, and $I_D = 0.4$ mA

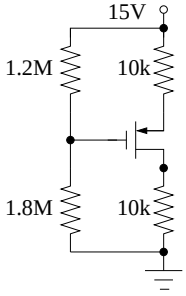
Small-Signal parameters: $g_m = 0.8 \times 10^{-3}$ and $r_o = 268$ k.

Amp. Response: $A_v = -8$, $R_i \to \infty$, $R_{out} = R_o = 268$ k, $f_{p1} = 0$ Hz, $f_{p2} = 14.5$ Hz, $f_{pb} = 143$ Hz, and $f_l = 158$ Hz. (only R_i and f_{p1} change

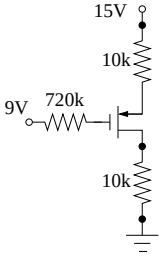
Saturation voltage: $-3.64 < v_o < 6.86$ V and $-0.86 < v_i = -v_o/8 < 0.46$ V.

Problem 23. Find the bias point and amplifier parameters of this circuit ($V_{tp} = -4$ V, $k'_p(W/L) = 0.4$ mA/V^2, $\lambda = 0.01$ V^{-1}). Ignore the channel-width modulation effect in biasing calculations. Find the saturation voltages for this amplifier.





Bias



Bias

Bias: ($v_i = 0$ and capacitors open) Replacing R_1/R_2 voltage divider with its Thevenin equivalent:

$$R_G = 1.2 \text{ M} \parallel 1.8 \text{ M} = 720 \text{ k}, \qquad V_{GG} = \frac{1.8}{1.2 + 11.8} \times 15 = 9 \text{ V}$$

Assume PMOS is in the active state,

$$I_D = 0.5k'_n(W/L)(V_{SG} - |V_{tp}|)^2 = 0.5 \times 0.8 \times 10^{-3}(V_{SG} - 1)^2$$

SG-KVL: $\quad 6 = V_{SG} + 10^4 I_D = V_{SG} + 4(V_{SG} - 1)^2 \quad \rightarrow \quad 4V_{SG}^2 - 7V_{SG} - 2 = 0$

Two roots: $+2$ and -0.25. As the negative root is unphysical, $V_{SG} = 2$.

SG-KVL: $\quad 6 = 2 + 10^4 I_D \quad \rightarrow \quad I_D = 0.4$ mA

SD-KVL: $\quad 15 = 10^4 I_D + V_{SD} + 10^4 I_D \quad \rightarrow \quad V_{SD} = 15 - 2 \times 10^4 \times 0.4 \times 10^{-3} = 7$ V

Since $V_{SD} = 7 \geq V_{SG} - |V_{tp}| = 2 - 1 = 12$ V, our assumption of PMOS in active state is justified.

Bias summary: $V_{SG} = 2$ V, $V_{SD} = 7$ V, and $I_D = 0.4$ mA

Small-Signal: First we calculate the small-signal parameters ($V_A = 1/\lambda = 100$ V):

$$g_m = \frac{2I_D}{V_{SG} - |V_{tp}|} = \frac{2 \times 0.4 \times 10^{-3}}{2 - 1} = 0.8 \times 10^{-3}$$

$$r_o = \frac{V_A + V_{SD}}{I_D} = \frac{100 + 7}{0.4 \times 10^{-3}} = 268 \text{ k}$$

Proceeding with the small signal analysis, we zero bias sources (see circuit). As the input is at the gate and output is at the collector and there is a R_S, this is degenerated common-source amplifier. Using formulas of page 5-22 and noting $R_D \ll R_L$ and $R_D \ll r_o$:

$$A_v = -\frac{g_m(R_D \parallel R_L)}{1 + g_m R_S + (R_D \parallel R_L)/r_o} \approx -\frac{g_m R_D}{1 + g_m R_S} = -0.89$$

$$R_i = R_G = 720 \text{ k}$$

$$R_{out} = R_o = r_o(1 + g_m R_S) = 2.4\ M$$

$$f_{p1} = 1/[2\pi C_{c1}(R_i + R_{sig})] = 2.21 \text{ Hz}$$

$$f_{p2} = 1/[2\pi C_{c2}(R_L + R_D \parallel R_{out})] \approx 1/[2\pi C_{c2}(R_L + R_D] \approx 1/[2\pi C_{c2} R_L] = 0.16 \text{ Hz}$$

$$f_l = f_{p1} + f_{p2} = 2.4 \text{ Hz}$$

Note one needs to choose R_D to be several times R_S for this amplifier to have a gain larger than unity.

NMOS remains in saturation as long as $i_D = i_S > 0$, $v_{GS} > V_{tn}$, and $v_{DS} > v_{GS} - V_{tn}$. For this problem that $v_o = +(R_D \parallel R_L) i_d \approx R_D i_d = 10^4 i_d$:

$$i_D = I_D + i_d > 0 \quad \rightarrow \quad i_d > -I_D = -0.4 \text{ mA} \quad \rightarrow \quad v_o = 10^5 i_d > -4 \text{ V}$$

Since the voltage at the gate of the transistor is the sum of v_i and the 6-V bias:

DS-KVL $\quad 15 = R_S I_D + R_S i_d + v_{SD} + R_D I_D + R_D i_d$

GS-KVL $\quad 15 = R_S I_D + R_S i_d + v_{SG} + 9 + v_i$

$$v_{SD} - v_{SG} = 5 + v_i - v_o > V_{tn} = 1 \quad \rightarrow \quad v_o - v_i = v_o(1 - 1/A_v) < 6$$

$$(1 + 1/0.89) v_o < 6 \quad \rightarrow \quad v_o < 2.83 \text{ V}$$

where the 3rd equation is found by subtracting GS-KVL from GS-KVL. Therefore, limits for this amplifiers are $-4 < v_o < 2.83$ V and $-3.18 < v_i = -v_o/8 < 4.49$ V. The amplifier will saturate when v_o exceeds the above values.

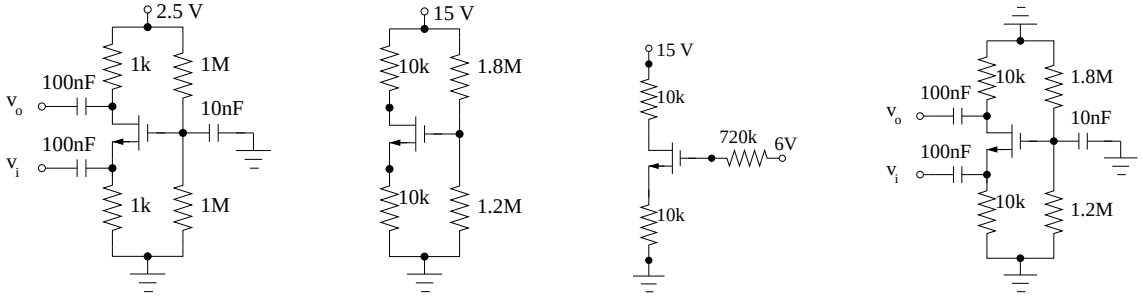
Problem 24. Find the bias point and amplifier parameters of this circuit ($V_{tp} = -4$ V, $k'_p(W/L) = 0.4$ mA/V^2, $\lambda = 0.01$ V^{-1}). Ignore the channel-width modulation effect in biasing calculations. Find the saturation voltages for this amplifier.

This is the PMOS version of Problem 23.

Problem 25. Find the bias point and amplifier parameters of this circuit ($V_{tn} = 4$ V, $k_n'(W/L) = 0.4$ mA/V^2, $\lambda = 0.01$ V^{-1}). Ignore the channel-width modulation effect in biasing calculations. Find the saturation voltages for this amplifier.

This circuit is similar to that of Problem 23 except that the NMOS is biased with two voltage sources and $R_G \to \infty$ and no pole from C_{c1}. Answers are the same as those of problem 23 except $R_i \to \infty$ and $f_l = 0.16$ Hz.

Problem 26. Find the bias point and amplifier parameters of this circuit ($V_{tp} = -4$ V, $k_p'(W/L) = 0.4$ mA/V^2, $\lambda = 0.01$ V^{-1}). Ignore the channel-width modulation effect in biasing calculations. Find the saturation voltages for this amplifier.



Bias Bias Small-signal

Bias: ($v_i = 0$ and capacitors open) Replacing R_1/R_2 voltage divider with its Thevenin equivalent:

$$R_G = 1.2 \text{ M} \parallel 1.8 \text{ M} = 720 \text{ k}, \qquad V_{GG} = \frac{1.2}{1.2 + 11.8} \times 15 = 6 \text{ V}$$

Assume NMOS is in the active state,

$$I_D = 0.5 k_n'(W/L)(V_{GS} - V_{tn})^2 = 0.5 \times 0.8 \times 10^{-3}(V_{GS} - 1)^2$$

GS-KVL: $\quad 6 = V_{GS} + 10^4 I_D = V_{GS} + 4(V_{GS} - 1)^2 \quad \to \quad 4V_{GS}^2 - 7V_{GS} - 2 = 0$

Two roots: $+2$ and -0.25. As the negative root is unphysical, $V_{GS} = 2$.

GS-KVL: $\quad 6 = 2 + 10^4 I_D \quad \to \quad I_D = 0.4$ mA

DS-KVL: $\quad 15 = 10^4 I_D + V_{DS} + 10^4 I_D \quad \to \quad V_{DS} = 15 - 2 \times 10^4 \times 0.4 \times 10^{-3} = 7$ V

Since $V_{DS} = 7 \geq V_{GS} - V_{tn} = 2 - 1 = 12$ V, our assumption of NMOS in active state is justified.

Bias summary: $V_{GS} = 2$ V, $V_{DS} = 7$ V, and $I_D = 0.4$ mA

Small-Signal: First we calculate the small-signal parameters ($V_A = 1/\lambda = 100$ V):

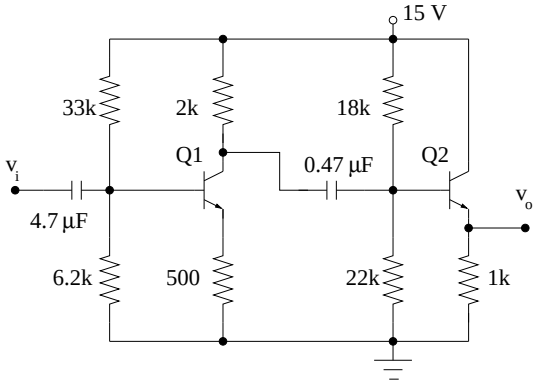
$$g_m = \frac{2I_D}{V_{GS} - V_{tn}} = \frac{2 \times 0.4 \times 10^{-3}}{2 - 1} = 0.8 \times 10^{-3}$$
$$r_o = \frac{V_A + V_{DS}}{I_D} = \frac{100 + 7}{0.4 \times 10^{-3}} = 268 \text{ k}$$

Proceeding with the small signal analysis, we zero bias sources (see circuit). As the input is at the source and output is at the collector, this is a common-gate amplifier. Using formulas of page 5-22 and noting $R_L \to \infty$ and $R_D \ll r_o$:

$$A_v = g_m(r_o \parallel R_D \parallel R_L) \approx g_m R_D = 8$$
$$R_i = R_S \parallel [1/g_m + (R_D \parallel R_L)/g_m r_o] = R_S \parallel [(1/g_m)(1 + R_D/r_o)] \approx R_S \parallel 1/g_m$$
$$R_i = 10^4 \parallel (1.25 \times 10^3) = 1.1 \text{ k}$$
$$R_o = r_o = 268 \text{ k} \qquad R_{out} = r_o(1 + g_m R_S) = 2.4 \text{ M}$$
$$f_{p1} = 1/[2\pi C_{c1}(R_i + R_{sig})] = 1.45 \text{ kHz}$$
$$f_{p2} = 1/[2\pi C_{c2}(R_L + R_D \parallel R_{out})] = 0$$
$$f_{pb} = 1/[2\pi C_b R_G] = 22 \text{ Hz}$$
$$f_l = f_{p1} + f_{p2} + f_{pb} = 1.47 \text{ kHz}$$

Problem 27. Find the bias point of each BJT, the overall gain (v_o/v_i), and the lower cut-off frequency of this amplifier parameters (Si BJT with $n = 2$, $\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations).

This is a two-stage amplifier. The first stage (Q1) is a common emitter amplifier and the second stage (Q2) is an emitter follower. The two stages are coupled by a coupling capacitor (0.47 μF).



Bias: When we replace the coupling capacitors with open circuits, we see the that bias circuits for the two transistors are independent of each other. Each bias circuit can be solved separately.

For Q1, we replace the bias resistors (6.2k and 33k) with their Thevenin equivalent and proceed with DC analysis:

$$R_{B1} = 6.2 \text{ k} \parallel 33 \text{ k} = 5.22 \text{ k}\Omega \qquad \text{and} \qquad V_{BB1} = \frac{6.2}{6.2+33}\,15 = 2.37 \text{ V}$$

$$\text{BE-KVL:} \quad V_{BB1} = R_{B1}I_{B1} + V_{BE1} + 500I_{E1} \qquad I_{B1} = \frac{I_{E1}}{1+\beta} = \frac{I_{E1}}{201}$$

$$2.37 - 0.7 = I_{E1}\left(\frac{5.22\times 10^3}{201} + 500\right)$$

$$I_{E1} = 3.17 \text{ mA} \approx I_{C1}, \qquad I_{B1} = \frac{I_{C1}}{\beta} = 16\ \mu\text{A}$$

$$\text{CE-KVL:} \quad V_{CC} = 2\times 10^3 I_{C1} + V_{CE1} + 500I_{E1}$$

$$V_{CE1} = 15 - 2.5\times 10^3 \times 3.17\times 10^{-3} = 7.1 \text{ V}$$

Following similar procedure for Q2, we get:

$$R_{B2} = 18 \text{ k} \parallel 22 \text{ k} = 9.9 \text{ k}\Omega \qquad \text{and} \qquad V_{BB2} = \frac{22}{18+22}\,15 = 8.25 \text{ V}$$

$$\text{BE-KVL:} \quad V_{BB2} = R_{B2}I_{B2} + V_{BE2} + 10^3 I_{E2} \qquad I_{B2} = \frac{I_{E2}}{1+\beta} = \frac{I_{E2}}{201}$$

$$8.25 - 0.7 = I_{E2}\left(\frac{9.9\times 10^3}{201} + 10^3\right)$$

$$I_{E2} = 7.2 \text{ mA} \approx I_{C2}, \qquad I_{B2} = \frac{I_{C2}}{\beta} = 36\ \mu\text{A}$$

$$\text{CE-KVL:} \quad V_{CC} = V_{CE2} + 10^3 I_{E2}$$

$$V_{CE2} = 15 - 10^3 \times 7.2\times 10^{-3} = 7.8 \text{ V}$$

Bias summary for Q1: $I_{E1} \approx I_{C1} = 3.17\text{mA}$, $I_{B1} = 16\ \mu\text{A}$, $V_{CE1} = 7.1$ V.

Bias summary for Q2: $I_{E2} \approx I_{C2} = 7.2\text{mA}$, $I_{B2} = 36\ \mu\text{A}$, $V_{CE2} = 7.8$ V.

Small Signal: First we calculate the small-signal parameters:

$$g_{m1} = \frac{I_{C1}}{nV_T} = \frac{3.17 \times 10^{-3}}{2 \times 26 \times 10^{-3}} = 6.10 \times 10^{-2} \qquad r_{e1} = \frac{1}{g_{m1}} = 16.4\ \Omega$$

$$r_{\pi 1} = \frac{\beta}{g_{m1}} = 3.28\text{ k} \qquad r_{o1} = \frac{V_A + V_{CE1}}{I_{C1}} = \frac{150 + 7.1}{3.17 \times 10^{-3}} = 49.6\text{ k}$$

$$g_{m2} = \frac{I_{C2}}{nV_T} = \frac{7.2 \times 10^{-3}}{2 \times 26 \times 10^{-3}} = 1.38 \times 10^{-1} \qquad r_{e2} = \frac{1}{g_{m2}} = 7.22\ \Omega$$

$$r_{\pi 2} = \frac{\beta}{g_{m2}} = 1.44\text{ k} \qquad r_{o2} = \frac{V_A + V_{CE2}}{I_{C2}} = \frac{150 + 7.8}{7.2 \times 10^{-3}} = 21.9\text{ k}$$

We should always start from the last stage as the input resistance of that stage appears as the load for the previous stage, *etc.* Second stage (Q2) is a emitter follower as its input is as the base and output is at the emitter. Using is in the emitter follower circuit (Q2) as the input resistance of this circuit will appear as the load for the common emitter amplifier (Q1). Using formulas of page 5-21 and noting $R_{L2} \to \infty$ and $R_E \gg r_e$:

$$A_{v2} = \frac{R_E \parallel R_L}{R_E \parallel R_L + r_e} = \frac{1,000}{1,000 + 16.4} \approx 1$$

$$R_{i2} = R_B \parallel [r_\pi + (1+\beta)(r_o \parallel R_E \parallel R_L)] \approx R_{B2} = 9.9\ k\Omega$$

The first stage (Q1) is a common emitter amplifier with R_E. The load for this stage is $R_{L1} = R_{i2}$. Using formulas of page 5-21:

$$A_{v1} = -\frac{R_C \parallel R_L}{R_E + r_e} = -\frac{(2k) \parallel (9.9k)}{500k} = -3.33$$

$$R_{i1} = R_B \parallel [r_\pi + (1+\beta)R_E] \approx R_B = 5.22\text{k}$$

$$A_v = \frac{v_o}{v_i} = A_{v1} \times A_{v2} = -3.33$$

The input resistance of the two-stage amplifier is the input resistance of the first-stage (Q1), $R_i = 5.2$ kΩ.

frequency Response: The 4.7 μF capacitor is C_{c1} for the first stage. Thus:

$$f_{p1} = 1/[2\pi C_{c1}(R_i + R_{sig})] = 1/[2\pi \times 4.7 \times 10^{-6} \times 5.22 \times 10^3] = 6.5\text{ Hz}$$

The 0.47 μF capacitor can be viewed is C_{c2} for the first stage which is common-emitter with R_E: Then:

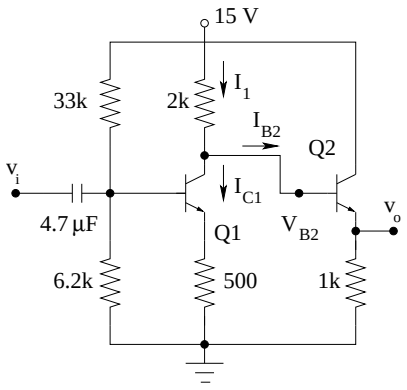
$$f_{p2} = 1/[2\pi C_{c2}(R_L + R_C \parallel R_{out})] = 1/[2\pi C_{c2}(R_{i2} + R_{C1} \parallel R_{out,1})]$$
$$f_{p2} \approx 1/[2\pi C_{c2}(R_{i2} + R_{C1}] = 28.5 \text{ Hz}$$

Note that we could have taken the 0.47 μF capacitor to be the C_{c1} for the second stage with $R_{sig} = R_{C1} \parallel R_{out,1}$, arriving at the same value for f_{p2}.

Then, $f_l = f_{p1} + f_{p2} = 35$ Hz.

Problem 28. Find the bias point of each BJT, the overall gain (v_o/v_i), and the lower cut-off frequency of this amplifier parameters (Si BJT with $n = 2$, $\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations).

This is a two-stage amplifier. The first stage (Q1) is a common emitter amplifier and the second stage (Q2) is an emitter follower. The circuit is similar to the two-stage amplifier of Problem 27. The only difference is that Q2 is directly biased from Q1 and there is no coupling capacitor between the two stages. This approach has its own advantages and disadvantages that are discussed at the end of this problem.



Bias: Since the base current in BJTs is typically much smaller that the collector current, we start by assuming $I_{C1} \gg I_{B2}$. In this case, $I_1 = I_{C1} + I_{B2} \approx I_{C1} \approx I_{E1}$ (the bias current I_{B2} has no effect on bias parameters of Q1). This assumption simplifies the analysis considerably and we will check the validity of this assumption later.

For Q1, we replace the bias resistors (6.2k and 33k) with their Thevenin equivalent:

$$R_{B1} = 6.2 \text{ k} \parallel 33 \text{ k} = 5.22 \text{ k}\Omega \qquad \text{and} \qquad V_{BB1} = \frac{6.2}{6.2 + 33} 15 = 2.37 \text{ V}$$

$$\text{BE-KVL:} \quad V_{BB1} = R_{B1} I_{B1} + V_{BE1} + 10^3 I_{E1} \qquad I_{B1} = \frac{I_{E1}}{1 + \beta} = \frac{I_{E1}}{201}$$

$$2.37 - 0.7 = I_{E1} \left(\frac{5.22 \times 10^3}{201} + 500 \right)$$

$$I_{E1} = 3.17 \text{ mA} \approx I_{C1}, \qquad I_{B1} = \frac{I_{C1}}{\beta} = 16 \ \mu\text{A}$$

$$\text{CE-KVL:} \quad V_{CC} = 2 \times 10^3 I_{C1} + V_{CE1} + 500 I_{E1}$$

$$V_{CE1} = 15 - 2.5 \times 10^3 \times 3.17 \times 10^{-3} = 7.1 \text{ V}$$

To find the bias point of Q2, we note:

$$V_{B2} = V_{CE1} + 500 \times I_{E1} = 7.1 + 500 \times 3.17 \times 10^{-3} = 8.68 \text{ V}$$

BE-KVL: $V_{B2} = V_{BE2} + 10^3 I_{E2}$

$$8.68 - 0.7 = 10^3 I_{E2}$$

$$I_{E2} = 8.0 \text{ mA} \approx I_{C2}, \qquad I_{B2} = \frac{I_{C2}}{\beta} = 40 \ \mu\text{A}$$

KVL: $V_{CC} = V_{CE2} + 10^3 I_{E2}$

$$V_{CE2} = 15 - 10^3 \times 8.0 \times 10^{-3} = 7.0 \text{ V}$$

We now check our assumption of $I_{C1} \gg I_{B2}$. We find $I_{C1} = 3.17$ mA$\gg I_{B2} = 41$ μA. So, our assumption was justified.

It should be noted that this bias arrangement is also stable to variation in transistor β. The bias resistors in the first stage will ensure that I_{C1} ($\approx I_{E1}$) and V_{CE1} is stable to variation of Q1 β. Since $V_{B2} = V_{CE1} + R_{E1} \times I_{E1}$, V_{B2} will also be stable to variation in transistor β. Finally, $V_{B2} = V_{BE2} + R_{E2} I_{E2}$. Thus, I_{C2} ($\approx I_{E2}$) will also be stable (and V_{CE2} because of CE-KVL).

Bias summary for Q1: $I_{E1} \approx I_{C1} = 3.17$ mA, $I_{B1} = 16$ μA, and $V_{CE1} = 7.1$ V

Bias summary for Q2: $I_{E2} \approx I_{C2} = 8.0$ mA, $I_{B2} = 40$ μA, and $V_{CE2} = 7.0$ V.

Small Signal: First we calculate the small-signal parameters:

$$g_{m1} = \frac{I_{C1}}{nV_T} = \frac{3.17 \times 10^{-3}}{2 \times 26 \times 10^{-3}} = 6.10 \times 10^{-2} \qquad r_{e1} = \frac{1}{g_{m1}} = 16.4 \ \Omega$$

$$r_{\pi 1} = \frac{\beta}{g_{m1}} = 3.28 \text{ k} \qquad r_{o1} = \frac{V_A + V_{CE1}}{I_{C1}} = \frac{150 + 7.1}{3.17 \times 10^{-3}} = 49.6 \text{ k}$$

$$g_{m2} = \frac{I_{C2}}{nV_T} = \frac{8.0 \times 10^{-3}}{2 \times 26 \times 10^{-3}} = 1.54 \times 10^{-1} \qquad r_{e2} = \frac{1}{g_{m2}} = 6.50 \ \Omega$$

$$r_{\pi 2} = \frac{\beta}{g_{m2}} = 1.30 \text{ k} \qquad r_{o2} = \frac{V_A + V_{CE2}}{I_{C2}} = \frac{150 + 7.0}{8 \times 10^{-3}} = 19.6 \text{ k}$$

As in problem 27, we start with the emitter follower circuit (Q2) as the input resistance of this circuit will appear as the load for the common emitter amplifier (Q1). Using formulas

of page 5-21 and noting $R_{L2} \to \infty$, $R_E \gg r_e$, and $R_{B1} \to \infty$:

$$A_{v2} = \frac{R_E \parallel R_L}{R_E \parallel R_L + r_e} = \frac{1,000}{1,000 + 16.4} \approx 1$$
$$R_{i2} = R_B \parallel [r_\pi + (1+\beta)(r_o \parallel R_E \parallel R_L)]$$
$$R_{i2} = r_\pi + (1+\beta)(r_o \parallel R_E) = 3.28 \times 10^3 + 201 \times 10^3 = 204 \text{ k}\Omega$$

Note that because of the absence of the bias resistors, the input resistance of the second stage is now quite large.

The first stage (Q1) is a common emitter amplifier with R_E. The load for this stage is $R_{L1} = R_{i2} = 204$ k. Using formulas of page 5-21, and noting $R_C \ll R_L$:

$$A_{v1} = -\frac{R_C \parallel R_L}{R_E + r_e} \approx -\frac{R_C}{R_E} = -4$$
$$R_{i1} \approx R_{B1} = 5.22 \; k\Omega$$
$$A_v = \frac{v_o}{v_i} = A_{v1} \times A_{v2} = -4$$

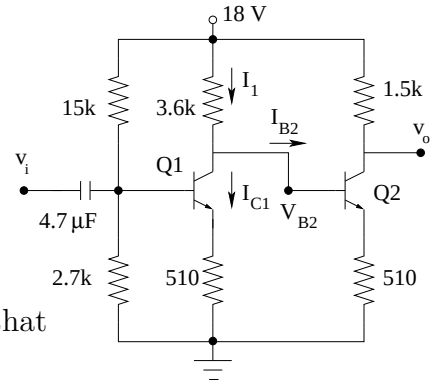
The input resistance of the two-stage amplifier is the input resistance of the first-stage (Q1), $R_i = 5.2$ kΩ.

frequency Response: The 4.7 μF capacitor is C_{c1} for the first stage. Thus:

$$f_l = f_{p1} = 1/[2\pi C_{c1}(R_i + R_{sig})] = 1/[2\pi \times 4.7 \times 10^{-6} \times 5.22 \times 10^3] = 6.5 \text{ Hz}$$

This two-stage amplifier has many advantages over that of problem 27. It has three less elements. Because of the absence of bias resistors, the second-stage does not load the first stage and the overall gain is higher. Also because of the absence of a coupling capacitor between the two-stages, the overall cut-off frequency of the circuit is lower. Some of these issues can be resolved by design, *e.g.,* use a large capacitor for coupling the two stages, use a large R_{E2}, *etc.*. The drawback of this circuit is that the bias circuit is more complicated and, as such, it is harder to design.

Problem 29. Find the bias point of each BJT, the overall gain (v_o/v_i), and the lower cut-off frequency of this amplifier parameters (Si BJT with $n = 2$, $\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations).



Bias: We start with replacing 2.7 k and 15 kΩ voltage divider with its Thevenin equivalent

$$R_B = 2.7 \parallel 15 = 2.29 \text{ k}\Omega$$

$$V_{BB} = \frac{2.7 \text{ k}}{2.7 \text{ k} + 15 \text{ k}} \times 18 = 2.75 \text{ V}$$

Writing a KVL through BE terminals of Q1 and assuming that Q1 is in the active state ($I_{C1} \approx I_{E1} = \beta I_{B1}$), we get:

$$V_{BB} = R_B I_{B1} + V_{BE1} + 510 I_{E1} = 2.29 \times 10^3 \frac{I_{C1}}{100} + 0.7 + 510 I_{C1}$$

$$I_{C1} \approx I_{E1} = 3.85 \text{ mA} \quad \rightarrow \quad I_{B1} = I_{C1}/\beta = 14.3 \ \mu\text{A}$$

CE1-KVL: $\quad 18 = 3.6 \times 10^3 I_1 + V_{CE1} + 510 I_{E1} \qquad I_1 = I_{C1} + I_{B2}$

We assume $I_{B2} \ll I_{C1}$. Then, from KCL above, $I_1 \approx I_{C1} = 3.85$ mA. Substituting for I_1 and I_{E1} in CE1-KVL, we find $V_{CE1} = 2.18$ V. Since $V_{CE1} > V_{D0} = 0.7$ V, our assumption of Q1 being in the active state is justified.

To find the bias point of Q2, we first calculate the voltage at the collector of Q1:

$$V_{C1} = V_{B2} = V_{CE1} + 510 I_{E1} = 2.18 + 1.96 = 4.14 \text{ V}$$

We assume that Q2 is in the active state. We can calculate $I_{C2} \approx I_{E2}$ from a KVL:

$$V_{C1} = V_{B2} = V_{BE2} + 510 I_{E2} \qquad \rightarrow \qquad 4.14 = 0.7 + 510 I_{E2}$$

$$I_{E2} \approx I_{C2} = 6.75 \text{ mA} \qquad \rightarrow \qquad I_{B2} = \frac{I_{C2}}{\beta} = 33.8 \ \mu\text{A}$$

Since $I_{B2} = 33.8 \ \mu\text{A} \ll I_{C1} = 3.85$ mA, our assumption of $I_{B2} \ll I_{C1}$ is justified. Lastly, we can find V_{CE2} from a KVL through CE terminals of Q2:

$$18 = 1.5 \times 10^3 I_{C2} + V_{CE2} + 510 I_{E2} \qquad \rightarrow \qquad V_{CE2} = 4.43 \text{ V}$$

And since $V_{CE2} = 4.43 \text{ V} > V_{D0} = 0.7$ V, our assumption of Q2 being in the active state is justified.

Bias summary for Q1: $I_{E1} \approx I_{C1} = 3.85\text{mA}$, $I_{B1} = 14.3\ \mu\text{A}$, $V_{CE1} = 2.18$ V.

Bias summary for Q2: $I_{E2} \approx I_{C2} = 6.75\text{mA}$, $I_{B2} = 33.8\ \mu\text{A}$, $V_{CE2} = 4.43$ V.

Small Signal: First we calculate the small-signal parameters:

$$g_{m1} = \frac{I_{C1}}{nV_T} = \frac{3.85 \times 10^{-3}}{2 \times 26 \times 10^{-3}} = 7.40 \times 10^{-2} \qquad r_{e1} = \frac{1}{g_{m1}} = 13.5\ \Omega$$

$$r_{\pi 1} = \frac{\beta}{g_{m1}} = 2.70\text{ k} \qquad r_{o1} = \frac{V_A + V_{CE1}}{I_{C1}} = \frac{150 + 2.2}{3.85 \times 10^{-3}} = 39.5\text{ k}$$

$$g_{m2} = \frac{I_{C2}}{nV_T} = \frac{6.75 \times 10^{-3}}{2 \times 26 \times 10^{-3}} = 1.30 \times 10^{-1} \qquad r_{e2} = \frac{1}{g_{m2}} = 7.70\ \Omega$$

$$r_{\pi 2} = \frac{\beta}{g_{m2}} = 1.54\text{ k} \qquad r_{o2} = \frac{V_A + V_{CE2}}{I_{C2}} = \frac{150 + 4.43}{6.75 \times 10^{-3}} = 22.8\text{ k}$$

We start with the second stage (Q2). As the input is at the base and the put is at collector, this is common-emitter amplifier with R_E. Using formulas of page 5-21 and noting $R_{L2} \to \infty$, and $R_E \gg r_e$:

$$A_{v2} = -\frac{R_C \parallel R_L}{R_E + r_e} \approx -\frac{R_C}{R_E} = -2.94$$

$$R_{i2} = R_B \parallel [r_\pi + (1+\beta)(r_o \parallel R_E \parallel R_L)]$$

$$R_{i2} = r_\pi + (1+\beta)(r_o \parallel R_E) = 2.70 \times 10^3 + 201 \times 510 = 106\ \text{k}\Omega$$

The first stage (Q1) is also a common emitter amplifier with R_E. The load for this stage is $R_{L1} = R_{i2} = 103$ k. Using formulas of page 5-21, and noting $R_C \ll R_L$:

$$A_{v1} = -\frac{R_C \parallel R_L}{R_E + r_e} \approx -\frac{R_C}{R_E} = -7.06$$

$$R_{i1} \approx R_{B1} = 2.29\ k\Omega$$

$$R_{i2} = r_\pi + (1+\beta)(r_o \parallel R_E) = 1.54 \times 10^3 + 201 \times 510 = 105\ \text{k}\Omega$$

$$A_v = \frac{v_o}{v_i} = A_{v1} \times A_{v2} = (-7.06)(-2.94) = 20.8$$

The input resistance of the two-stage amplifier is the input resistance of the first-stage (Q1), $R_i = 5.2\ \text{k}\Omega$.

frequency Response: The 4.7 μF capacitor is C_{c1} for the first stage. Thus:

$$f_l = f_{p1} = 1/[2\pi C_{c1}(R_i + R_{sig})] = 1/[2\pi \times 4.7 \times 10^{-6} \times 2.29 \times 10^3] = 14.8\text{ Hz}$$