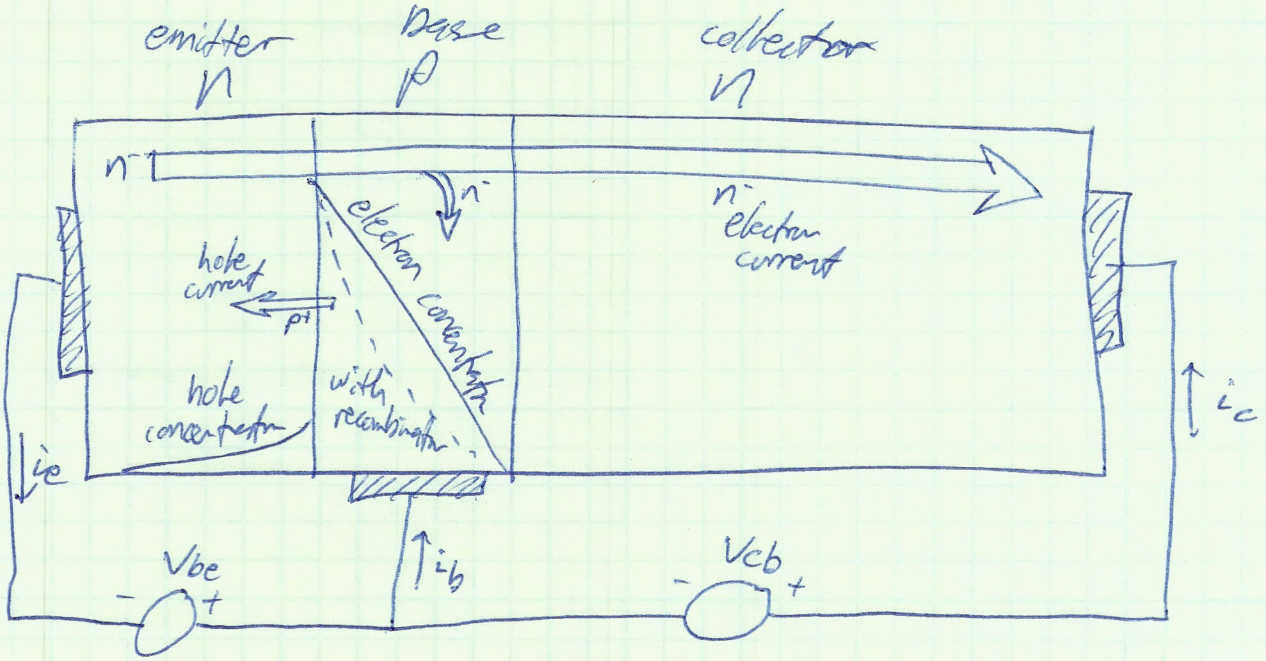
Bipolar Junction Transistors (BJTs)



six parameters: $i_b, i_e, i_c, v_{be}, v_{ce}, v_{bc}$

using KVL, KCL: $i_e = i_c + i_b$, $v_{bc} = v_{be} - v_{ce}$

only four independent parameters: i_b, i_c, v_{be}, v_{ce}

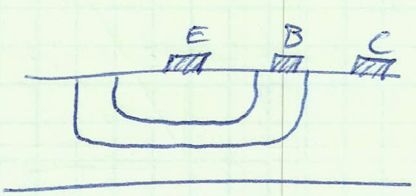
→ these specify iv characteristics of transistor

Principle of operation:

- In active mode: emitter base junction is forward-biased
  collector base junction is reverse-biased
- Level of doping in emitter is much higher than in the base
  → electron current is much greater than hole current into emitter
- Bias conditions set up a concentration gradient across base
  → very high near emitter, very low near collector
  → causes diffusion current across base
  → electrons that reach collector are swept over to collector contact

- Emitter current is primarily electrons, and a small hole current into base
- Base current is small hole current and small electron recombination current
- Collector current is most of the electrons from the emitter

Typical design: Base is thin, and lightly doped
Emitter is heavily doped



- Note that current flows across base-collector junction even though it is reverse-biased. It is caused by concentration gradient in base, set up by base emitter junction
- Number of holes going into emitter (proportional to i_B) is a constant fraction of number of electrons going into base (proportional to i_C). This ratio depends on doping and design

$\frac{i_C}{i_B} = \beta$ - defined as common emitter current gain

typical value is ~ 200

(about 200 electrons traveling for each hole)

Mode	E-B Junction	C-B junction
cutoff	reverse	reverse
active	forward	reverse
saturation	forward	forward

cutoff mode

B-E junction reverse biased, $i_B = 0 \rightarrow i_C = 0$

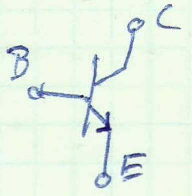
active mode

most of the current flows to the collector

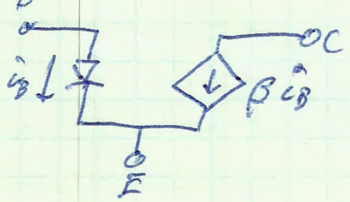
$$i_C = I_S\left(e^{v_{BE}/nV_T} - 1\right) \approx I_S e^{v_{BE}/nV_T}$$

$$i_B = \frac{I_S}{\beta}\left(e^{v_{BE}/nV_T} - 1\right) \approx \frac{I_S}{\beta} e^{v_{BE}/nV_T}$$

model for cutoff and active circuits:



npn



saturation mode

when $V_{CE} \lessapprox V_{D0}$, B-C junction becomes forward biased

extra holes injected into base from collector recombine with electrons

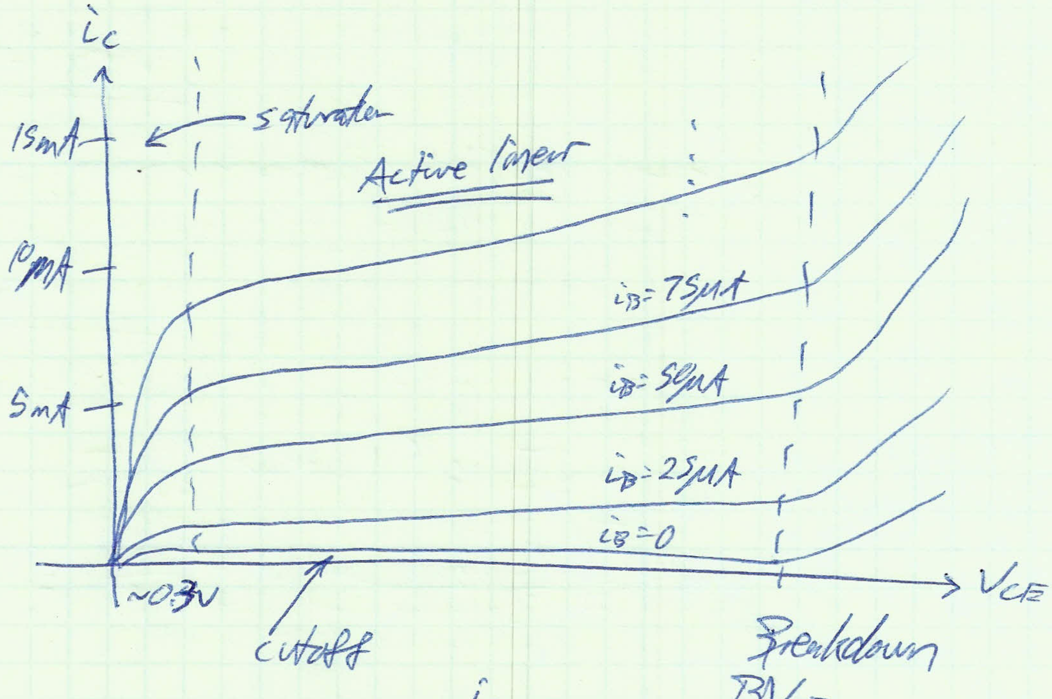
→ reduce collector current

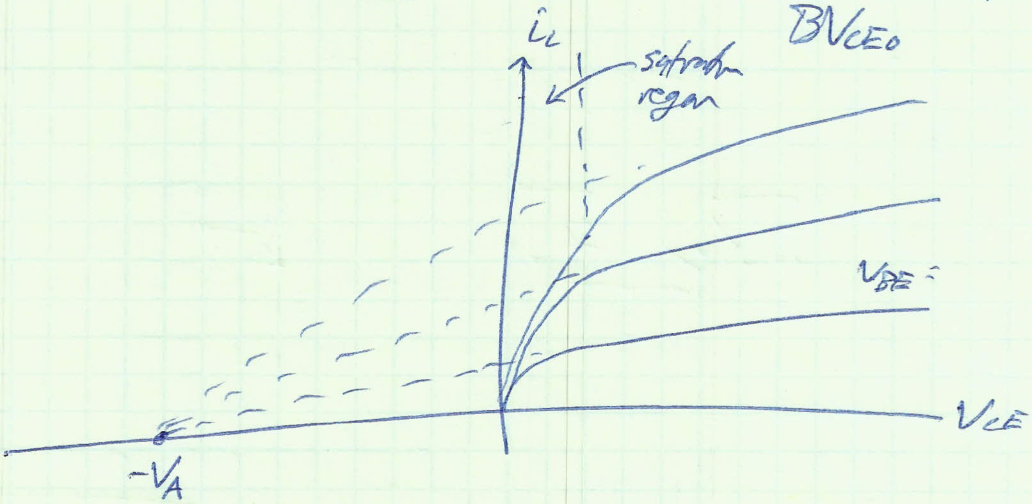
$i_C / i_B < \beta$

"soft saturation" may be considered as around $v_{CE} = 0.4V$ ($V_{BC} = 0.3V$)

as transistor behaves similarly to active mode, $\frac{i_C}{i_B}$ not yet reduced significantly

→ slightly forward biased, but not yet to turn-on



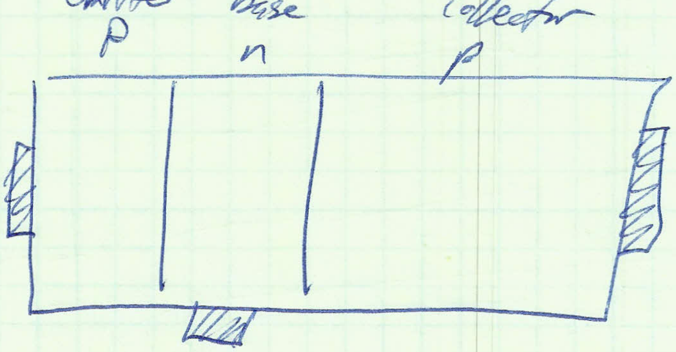


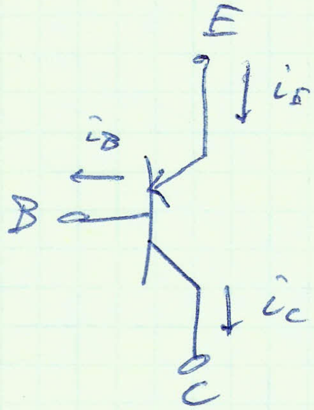
- The slope of the iv curves in the active region is due to the dependence of the depletion region width on V_{BC}
- wider depletion region → narrower effective base width
- V_A known as "Early voltage"
  - typically 50–100 V

$$i_C = I_S e^{V_{BE}/nV_T}\left(1 + \frac{V_{CE}}{V_A}\right)$$

$$i_B = \frac{I_S}{\beta} e^{V_{BE}/nV_T}$$ note i_B equation doesn't change

PNP transistor





- holes move slower than electrons (lower mobility) so pnp transistors are typically slower
- usually used in pairs with npn transistors

Summary

cutoff: $i_B = 0,\ i_C = 0$

active: $i_B = \frac{I_S}{\beta} e^{V_{BE}/nV_T}$, $i_C = I_S e^{V_{BE}/nV_T}\left(1 + \frac{V_{CE}}{V_A}\right)$

saturation: $i_B = \frac{I_S}{\beta} e^{V_{BE}/nV_T}$, $i_C < \beta i_B$, $V_{CE} = 0.1 - 0.3V$

- known as "large signal model"
- low frequency model - does not include capacitance