Piecewise Linear, Large Signal model for BJT

Cut-off

$i_B = 0$, $v_{BE} < V_{D0}$

$i_C = i_E = 0$

for PNP transistors
$V_{BE} \rightarrow V_{EB}$
$V_{CE} \rightarrow V_{EC}$

Active

$v_{BE} = V_{D0}$, $i_B \geq 0$

$i_C = \beta i_B$, $v_{CE} > V_{D0}$

can ignore Early effect (5% error)
if necessary to include it, use $i_C = \beta i_B \left(1 + \frac{v_{CE}}{V_A}\right)$

for soft saturation, ($v_{CE} \geq 0.4v$) $i_C \simeq \beta i_B$
we can use $v_{CE} \geq 0.4v$ instead of $v_{CE} \geq V_{D0}$

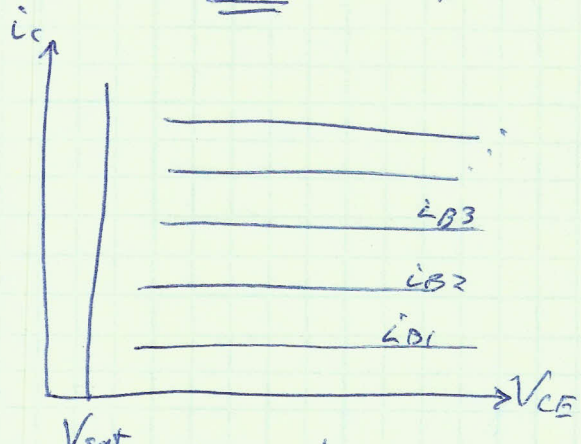
However - difficult to design in this region
- we will still use $v_{CE} \geq V_{D0}$ in this course

Model for saturation mode is complicated - we will use piecewise linear

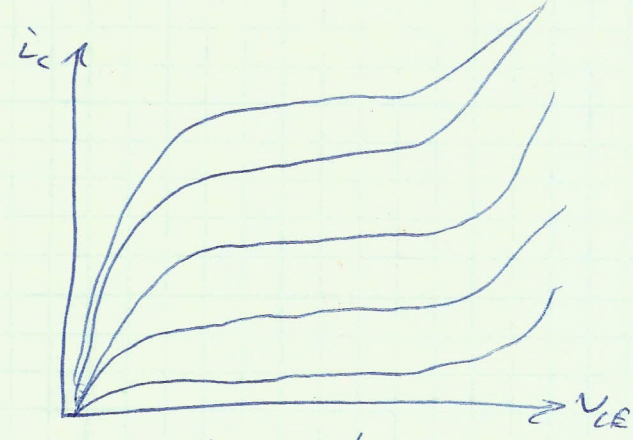
Saturation mode ($0.1 \leq v_{CE} \leq 0.3v$)

$v_{BE} = V_{D0}$, $i_B > 0$

$v_{CE} \simeq V_{sat}$, $i_C < \beta i_B$ use $0.2v$ for V_{sat}



piecewise linear model



real i-v characteristic

How to solve BJT circuits

Just like diode - assume a state, then check assumptions

- write KVL for BE terminals
- write KVL for CE terminals
- assume cut-off (simplest)
  - set $i_B = 0$
  - calculate V_{BE} from BE-KVL
  - ✱ - if $V_{BE} < V_{D0}$, BJT is in cut-off
    - set $i_C = i_E = 0$
    - calculate V_{CE} from CE-KVL → you are done
  - ✱ - if $V_{BE} > V_{D0}$, BJT is not in cut-off
- assume linear mode
  - set $i_E \simeq i_C = \beta i_B$
  - calculate V_{CE} from CE-KVL
- ✱ - if $V_{CE} > V_{D0}$, BJT is in active mode → you are done
- ✱ - if $V_{CE} < V_{D0}$, BJT is not in active mode - it is in saturation
  - set $V_{CE} = V_{sat}$
  - calculate i_C from CE-KVL
  - check that $i_C < \beta i_B$

For PNP transistors, substitute V_{BE} with V_{EB}
V_{CE} with V_{EC}

Note that V_{BE} not used

In active mode $i_E = i_C + i_B = (\beta+1) i_B$ and $i_E = \frac{\beta+1}{\beta} i_C$

since $\beta \gg 1$, use $i_E = i_C$ for simplicity

Even in saturation mode, $i_C \gg i_B$, $i_E \simeq i_C$