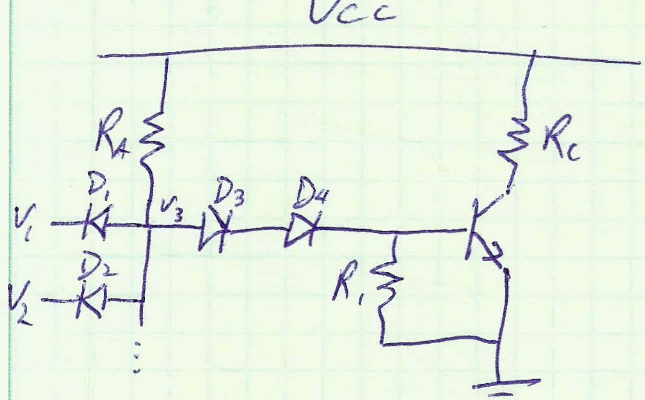
Wrap-up of DTL from last lecture

DTL NAND gate



If V_1 or V_2 are low ($V_{sat} = 0.2v$) that diode is ON and V_3 will be 0.7 volts higher. D_3 and D_4 will be OFF.

As both are raised to X, V_3 remains at $X+0.7$

The voltage V_3 required to switch the inverter is

$$V_3 = \underset{D_3}{0.7} + \underset{D_4}{0.7} + \underset{V_{BE}}{0.7} = 2.1$$

So the gate will start to switch at $X + 0.7 = 2.1_v$

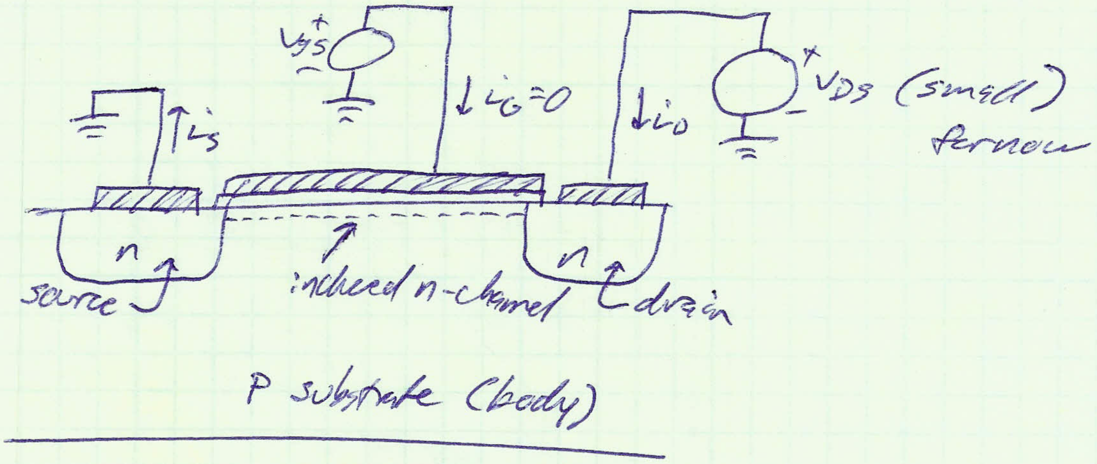
or $\underline{\underline{X = 1.4v}}$ → $\underline{V_{IL} = 1.4v}$

Solving for V_{IH} takes longer

- determine the edge of saturation for the transistor
- assume saturation, find i_C and i_B
- determine what input voltage gives $i_B > \frac{i_C}{\beta}$
- must consider currents going out through gate input and through resister R_1

Field Effect Transistors (FETs)

MOSFET = Metal Oxide Semiconductor Field Effect Transistor



- Two n regions deposited within p type substrate
- Gate applied between them, seperated by thin oxide layer (one of the reasons Si is important – forms high quality oxide)

- When voltage is applied to Gate, thin region under gate is depleted
- With higher voltage, thin inversion layer forms – behaves as n-type
  - forms conductive channel between source and drain
  - thickness depends on V_{GS} – proportional to $V_{GS} - V_T$

threshold voltage

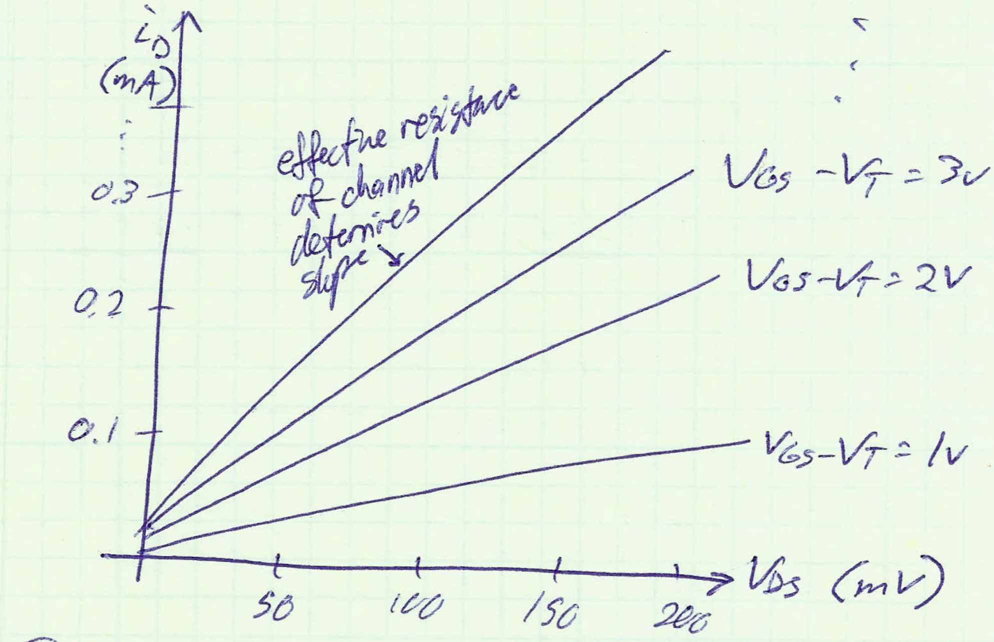
- This is called enhancement type NMOS

- there is also depletion type
- there is also PMOS

For $V_{GS} > V_T$ (so that channel is formed)

apply positive voltage to V_{DS}

acts as resistor – value depends on geometry of channel



Conductivity increases as $V_{GS} - V_T$ increases

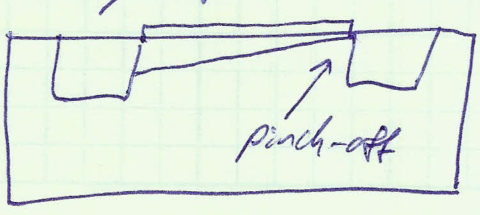
- Now apply larger Drain voltage

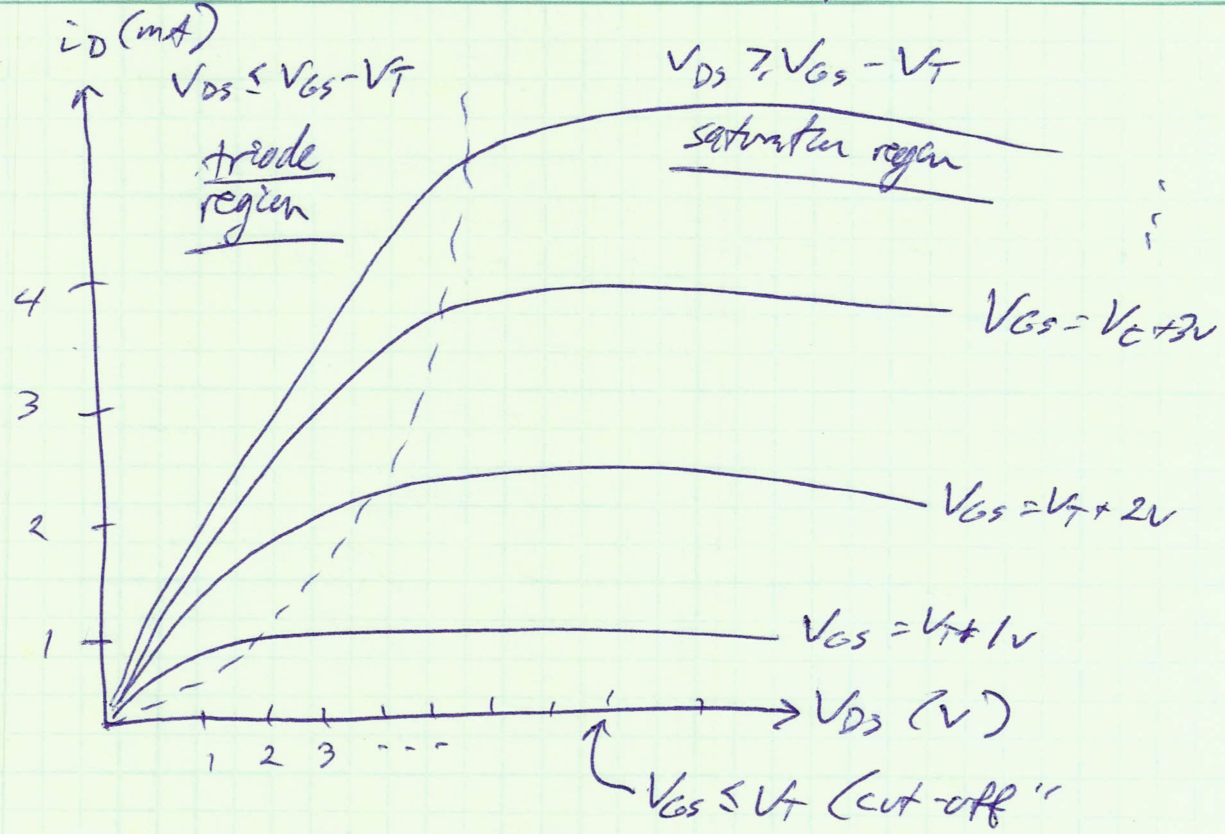
$$V_{GD} = V_{GS} - V_{DS} \; (< V_{GS})$$

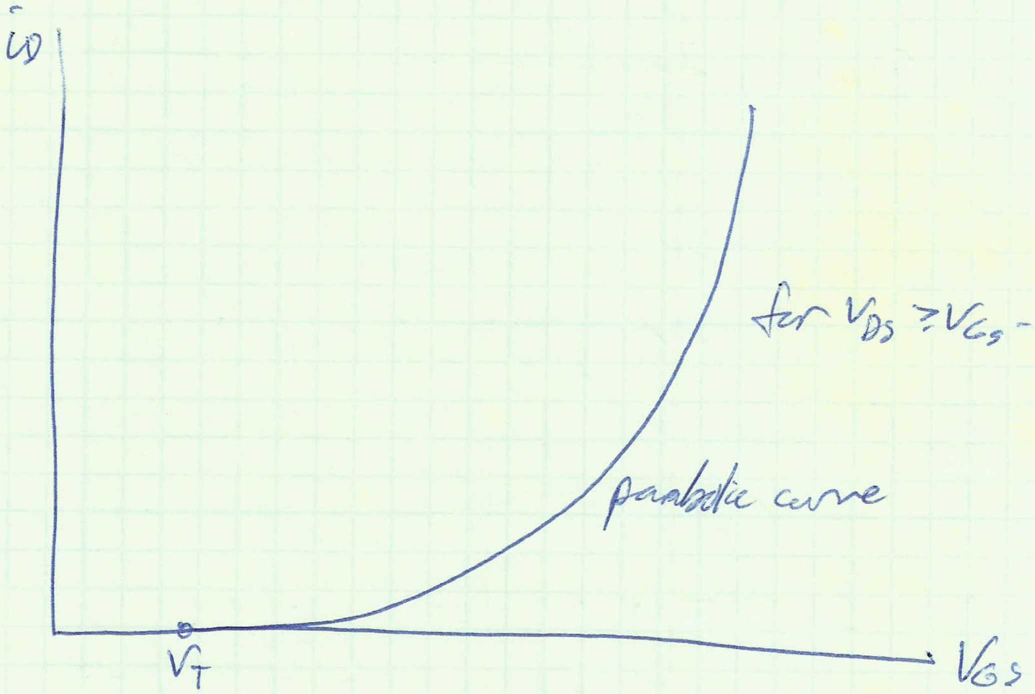
- channel near drain is smaller than near source
- when $V_{GD} = V_T$ (or $V_{DS} = V_{GS} - V_T$)

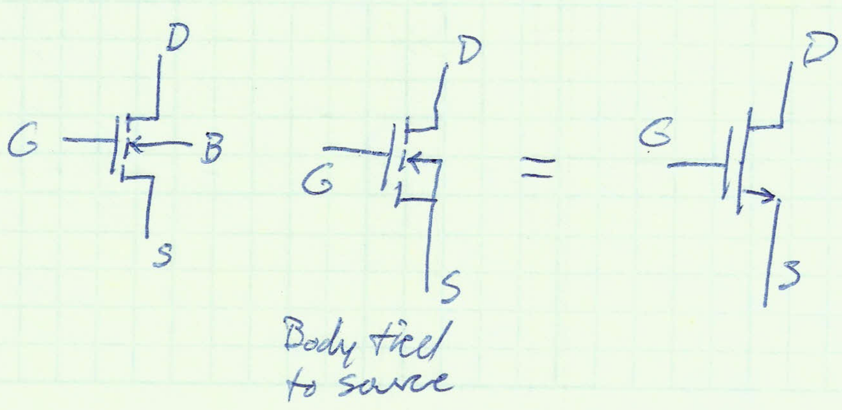
  the channel width approaches zero ("pinch-off")
- Current is constant after that point
  - i_D only depends on V_{GS}
- There is a small effect "channel width modulation"

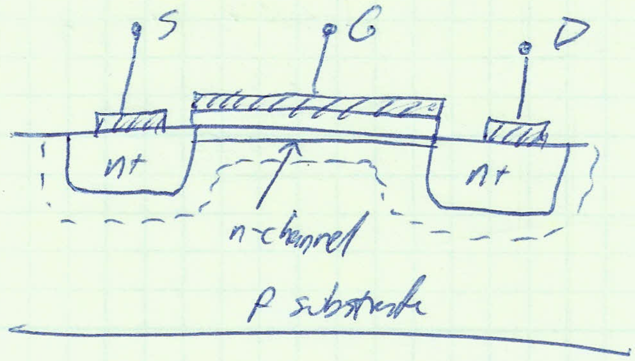
  similar to Early effect in BJTs




i_D (mA)
$V_{DS} \le V_{GS} - V_T$
triode region
$V_{DS} \ge V_{GS} - V_T$
saturation region
$V_{GS} = V_T + 3V$
$V_{GS} = V_T + 2V$
$V_{GS} = V_T + 1V$
4
3
2
1
1 2 3 ...
V_{DS} (V)
$V_{GS} \le V_T$ ("cut-off")


i_D
for $V_{DS} \ge V_{GS} - V_T$
parabolic curve
V_T
V_{GS}


D
G
B
S
D
G
S
=
D
G
S
Body tied to source



inversion layer (channel) starts to form at $V_{GS} = V_T$

charge in channel $|Q| = \underbrace{C_{ox}}_{\text{capacitance per area}} \underbrace{W L}_{\text{area}} (V_{GS} - V_T)$

capacitance is typically ~fF

Q per unit length

$$= \frac{|Q|}{L} = C_{ox} W (V_{GS} - V_T)$$

electric field $|E| = \dfrac{V_{DS}}{L}$

electron drift velocity $= \mu_n |E| = \mu_n \dfrac{V_{DS}}{L}$

current i_D = charge per unit length × drift velocity

$$i_D = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T) \cdot V_{DS}$$

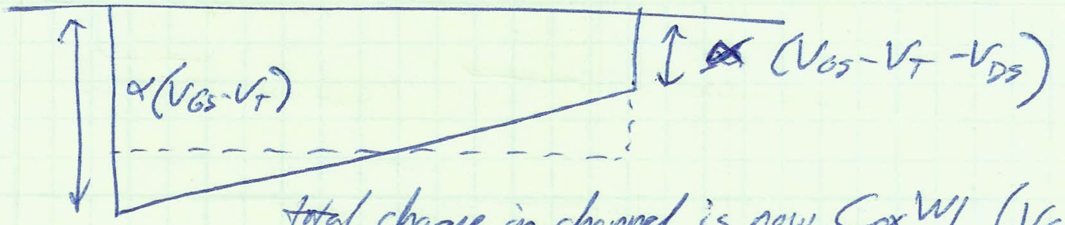
conductance of channel $g_{DS} = \dfrac{i_D}{V_{DS}} = \mu_n C_{ox} \dfrac{W}{L} (V_{GS} - V_T)$

some books use $k_n = \mu_n C_{ox} \dfrac{W}{L}$

we call $\mu_n C_{ox}$ the process transconductance parameter $k_n' = \mu_n C_{ox}$

resistance of channel $r_{DS} = \dfrac{1}{g_{DS}} = \dfrac{1}{k_n' \frac{W}{L} (V_{GS} - V_T)}$

Now apply larger V_{DS}:

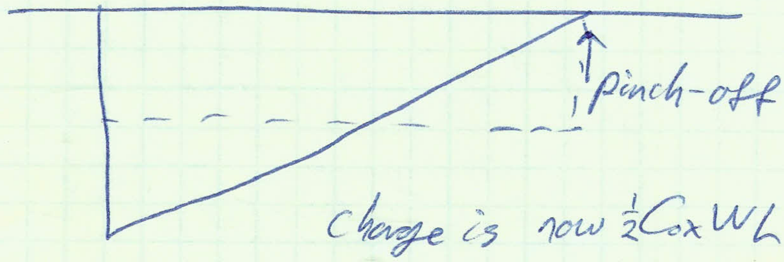


total charge in channel is now $C_{ox} W L \left(V_{GS} - V_T - \frac{1}{2} V_{DS}\right)$

current $$i_D = k' \frac{W}{L} \left(V_{GS} - V_T - \frac{1}{2} V_{DS}\right) V_{DS}$$

$$i_D = k' \frac{W}{L} \left((V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right)$$

when $V_{DS} > V_{GS} - V_T$:



Charge is now $\frac{1}{2} C_{ox} W L \, V_{GS}$

$$i_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_T)^2$$