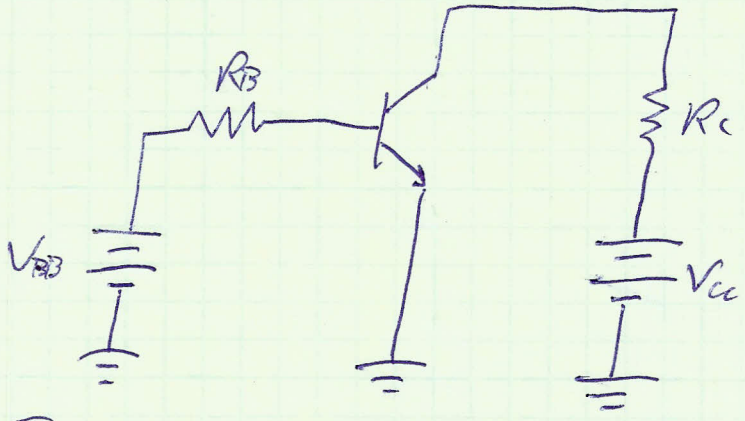
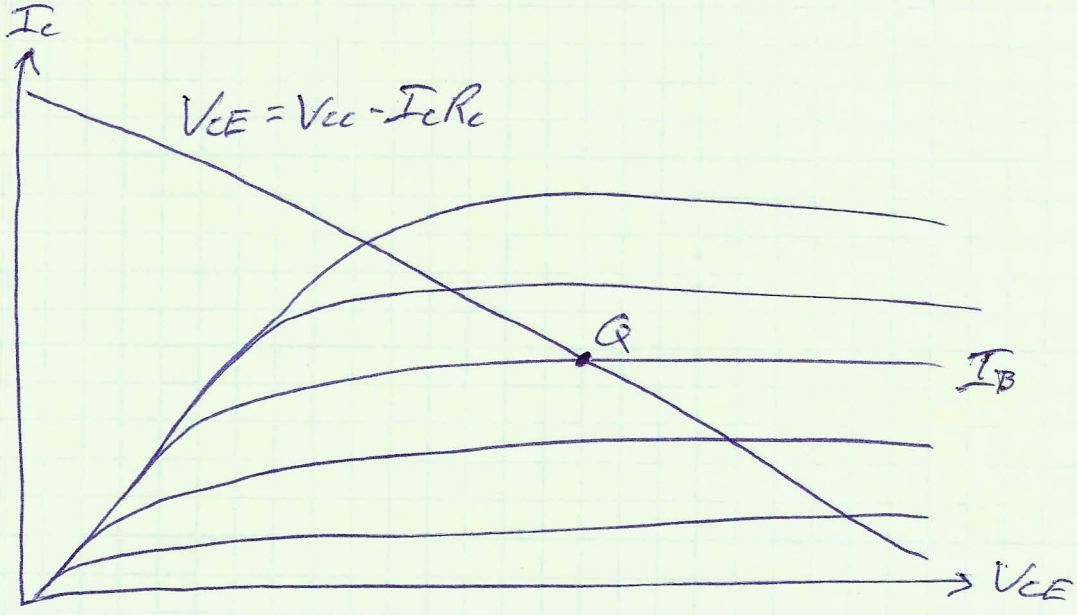
Amplifiers

- Basic component of analog circuits - including op amps
(switches are basic component of digital circuits)



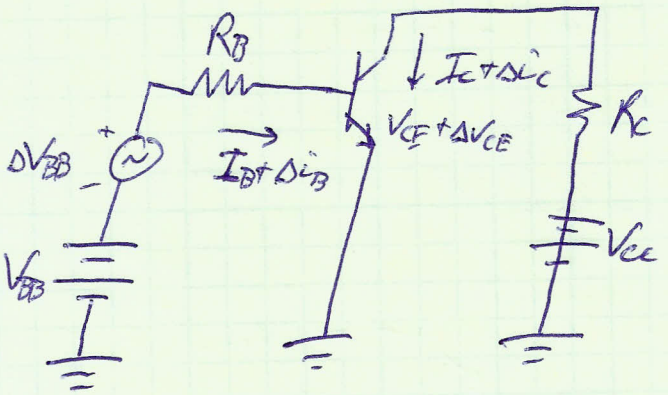


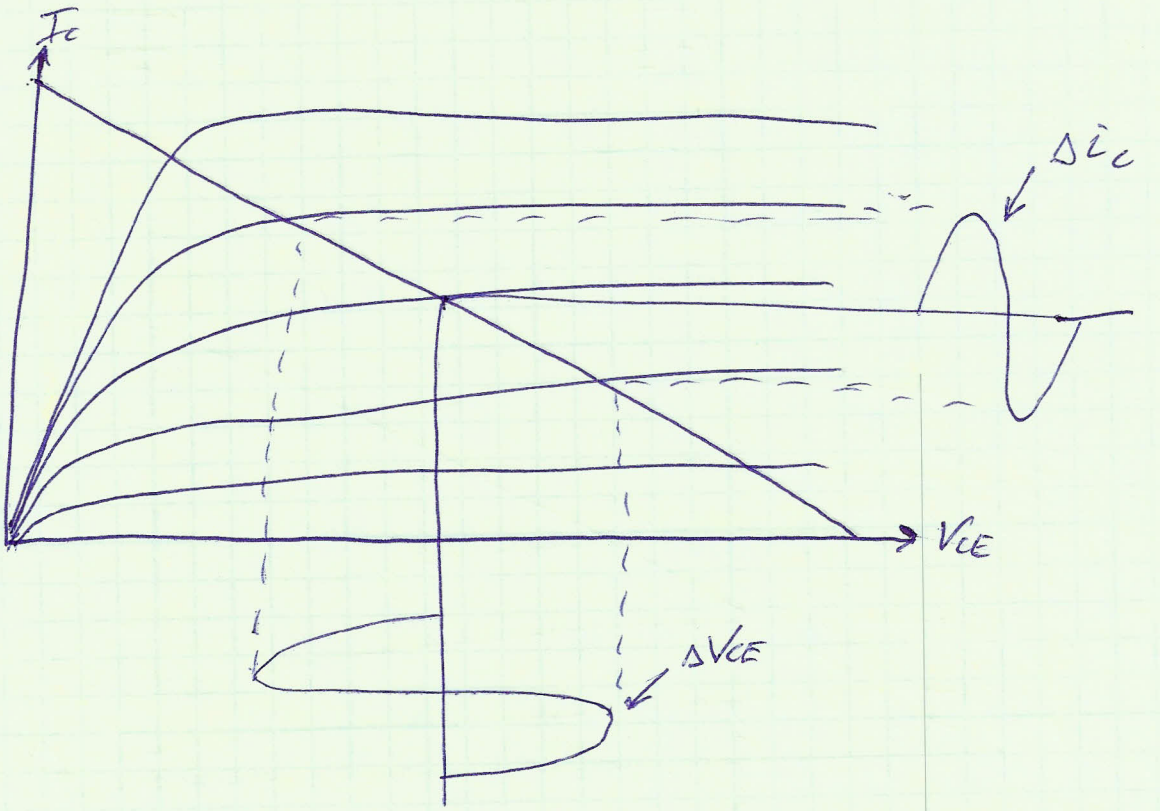
Load Line (Graphical analysis)

Q = quiescent point (operating point)

Q changes as I_B changes

Add sinusoidal source ΔV_{BB} in series with V_{BB}





- Δi_B causes Δi_C, which causes ΔV_{CE}
- I_B may be ~100μA
- Δi_B may be ~10μA
- I_C may be ~10mA (βI_B)
- ΔV_{CE} will be ~ $R_C \Delta i_C$
- Δi_C may be ~1mA

- Output (ΔV_{CE}) is amplified form of ΔV_{BB}
- β, R_C, and R_B all play a role

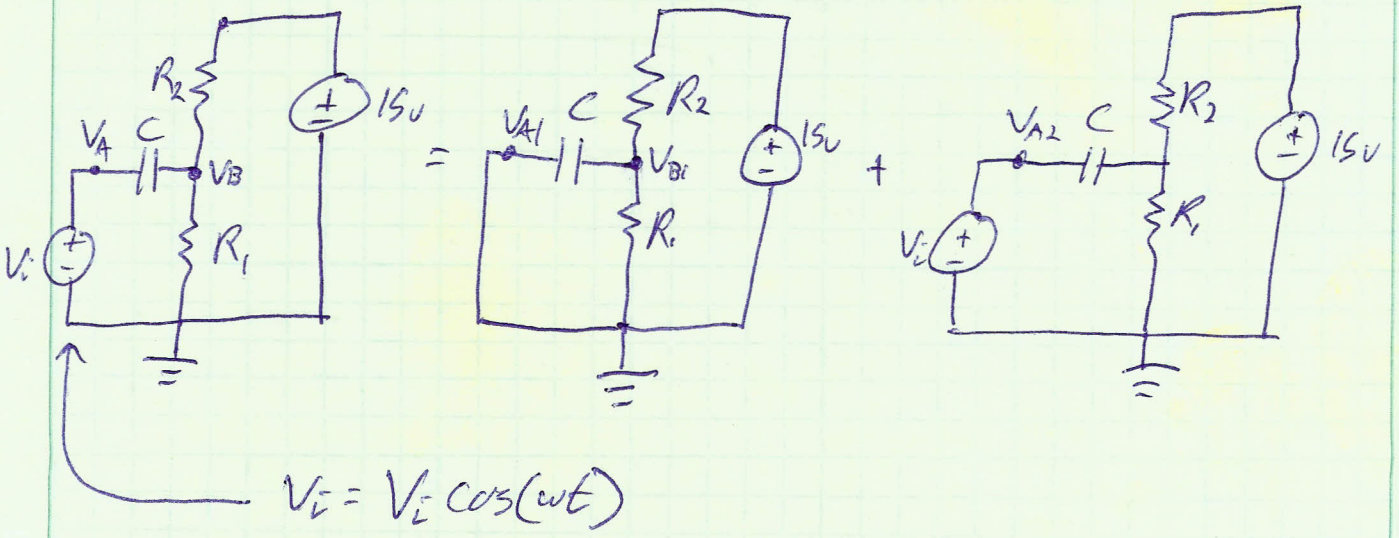
Issues with amplifiers

- BJT must remain in active state
  - if $I_B + \Delta i_B < 0$, it reaches cut-off
  - at high current, it will reach saturation
- The inputs and outputs have unwanted DC components
  - eliminate by capacitive coupling
- The amplifier must be linear
  - trade-off between linearity and power consumption

Capacitive Coupling

- Capacitors are open circuits for DC
- for higher frequencies, $Z = \frac{1}{j\omega C}$
  - we can choose value of C so that impedance is small

Importance of superposition



Solve the circuit by superposition
- kill each source, and analyze the circuit with just the other source

Circuit #1

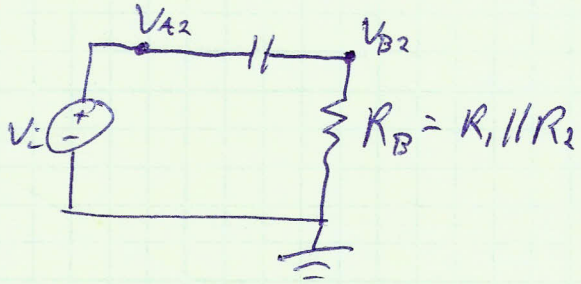
- Only DC source → capacitor is open circuit

$$V_{A1} = 0 \quad , \quad V_{B1} = 15 \frac{R_1}{R_1 + R_2}$$

Circuit #2

- R_1 and R_2 are in parallel

equivalent to :



This is a high-pass filter

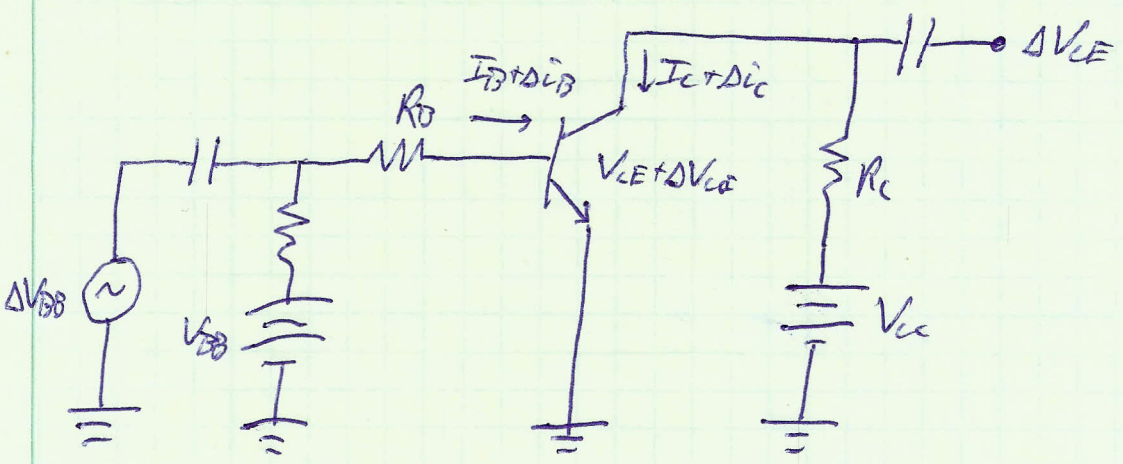
$$V_{B2} = V_i \frac{R_B}{R_B + \frac{1}{j\omega C}} = V_i \frac{j\omega R_B C}{j\omega R_B C + 1}$$

if $\omega R_B C \gg 1$, $V_{B2} \simeq V_i$

$$V_A = V_{A1} + V_{A2} = 0 + V_i \cos(\omega t)$$

$$V_B = V_{B1} + V_{B2} = 15 \times \frac{R_1}{R_1 + R_2} + V_i \cos(\omega t)$$

- capacitor prevents DC voltage from appearing at point A
- Point B contains sum of both voltages



- Use capacitors at both the input and output to separate the signals

Notation

- Bias components: V_{BE}, I_B, etc — Upper upper
- signal components: v_{be}, i_b, etc — lower lower
- Total: v_{BE}, i_B — lower Upper

Superposition

- Can only really be used for linear circuits, and these are nonlinear
- with small signal model, we treat the transistor as approximately linear
- we extract the signals in the linear part of the circuit (not inside the transistor)

Fourier analysis

- We used sine waves in our analysis
- signals can always be decomposed into sine waves

DC Amplifiers (vs AC)

- With capacitive coupling we have an AC amplifier
- lower frequency cutoff determined by value of coupling capacitors
- different design needed for DC

Biasing

total = DC + signal

$$v_{CE} = V_{CE} + v_{ce} \geq V_{DD}$$

$$\rightarrow v_{ce} \geq -(V_{CE} - V_{DD})$$

- this limits the negative values of v_{ce}
- transistor will enter saturation beyond that point

$i_C > 0$ and CE-KVL

$$\rightarrow v_{CE} = V_{CE} + v_{ce} < V_{cc} \rightarrow v_{ce} < V_{cc} - V_{CE}$$

- this limits the positive values of v_{ce}
- transistor will enter cut-off beyond that point

For FETs

$$v_{DS} \geq V_{GS} - V_t \rightarrow v_{ds} > v_{gs} - (V_{DS} - V_{GS} + V_t) \simeq -(V_{DS} - V_{GS} + V_t)$$

limits negative values, otherwise enters triode state

$i_D > 0$ and DS-KVL $\rightarrow v_{ds} < \ldots$

depends on DS-KVL, limits positive values, otherwise enters cut-off

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usually choose Q point in the middle of load line

$V_{CE} \simeq 0.5 V_{cc}$ for BJT

Power dissipation is also a consideration

$P = V_{CE} I_C$