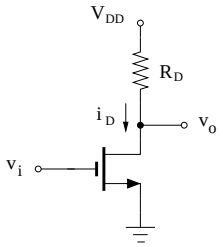
# V. Introduction to Transistors Amplifiers: Bias & Signal Circuits

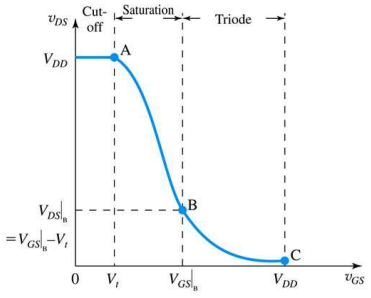
## 5.1 Introduction

Amplifiers are the main component of any analog circuit. Not only they can amplify a signal, they can be configured into may other useful circuits with a proper "feedback" (you will see this in ECE100 for OpAmps). In this course, we focus on simple transistor amplifiers. As simple BJT amplifiers are similar in design to MOS amplifiers, we discuss them together.

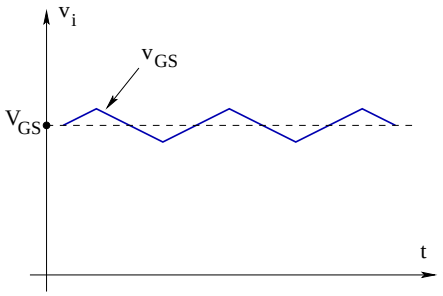
The transfer function of a linear amplifier is in the form, $v_o = A_v v_i$ where $A_v$ is the amplifier gain (its transfer function plot is a straight line that goes through the origin). Note that $A_v$ can be negative indicating a "180° phase shift in the output (in the frequency domain)

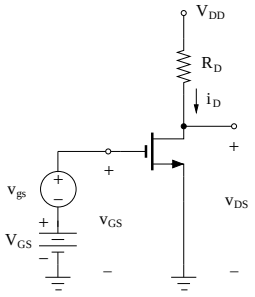
We have discussed the transfer function of BJT and MOS transistors before (NMOS circuit and its transfer function are shown). As can be seen, the MOS transfer function is non-linear. For example, if we apply a signal, $v_i = V_i \cos(\omega t)$ to the NMOS, $v_o = V_{DD}$ for all $v_i \leq V_t$.




We note, however, that the MOS transfer function in the saturation region is approximately linear, *i.e.,* is a straight line (although the transfer function is not going through the origin). This "approximate" linear behavior can be utilized to build transistor amplifiers. To see this, let's assume that we add a DC component to the input signal such that the NMOS remains in saturation at all times. For example, figures below show that a DC value, $V_{GS}$, is added to the signal of interest, $v_{gs}$, which is triangular in this case. The input voltage to the NMOS circuit is $v_i = v_{GS} = V_{GS} + v_{gs}$.

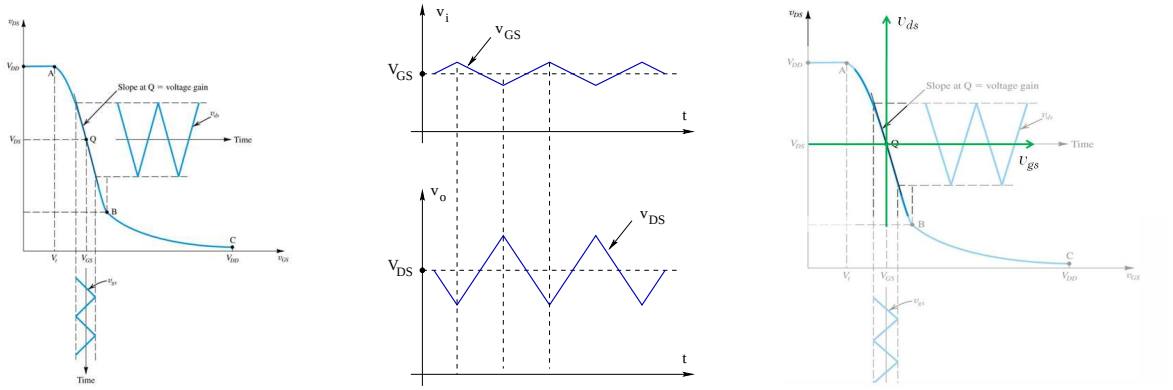



We can find the response of the MOS to this input signal by utilizing the MOS transfer function. At any given time, we find the input voltage $v_{GS}$ (from $v_{GS}$ vs time figure) and use the transfer function to find the related $v_{DS}$ for that time. We repeat this procedure at different times and construct a plot of $v_{DS}$ as a function of time as is shown.

We see that the output voltage $v_o = v_{DS}$ is also made of two components: a DC value $V_{DS}$ and a time-varying part, $v_{ds}$: $v_{DS} = V_{DS} + v_{ds}$. More importantly, $v_{ds}$ has the same "shape" as the input signal, $v_{gs}$ (which is possible only if $v_{ds}/v_{gs}$ is a constant). Therefore, although the overall response of the MOS ($v_{DS}$ vs $v_{GS}$) is non-linear, the response to the signal ($v_{ds}$ vs $v_{gs}$) appears to be linear.

We can find the signal transfer function ($v_{ds}$ vs $v_{gs}$) from the NMOS transfer function($v_{DS}$ vs $v_{GS}$). We note $v_{gs} = v_{GS} - V_{GS}$ and $v_{ds} = v_{DS} - V_{DS}$, *i.e.,* the signal transfer function is the same as the NMOS transfer function but with the origin located at the point $(V_{GS}, V_{DS})$ as is shown below right. This figures shows that the signal transfer function ($v_{ds}$ vs $v_{gs}$) is indeed linear as long as MOS remains in saturation.




In sum:

1. In order to arrive at a linear response from a MOS, we need to add a DC value to the input signal such that MOS would be in saturation at all times. The output consists of a DC value and a "signal output".

2. The "total" voltages/currents in the circuit are all sum of two components, a DC value (called the bias) and a signal value.

   Notation: Upper case letters with upper case subscripts (*e.g.* $V_{GS}, I_D$, voltage and current in a resistor: $V_R$ and $I_R$) denote the bias components. Lower case letters with lower case subscripts (*e.g.* $v_{gs}, i_d, v_r, i_r$) denote the signal components. Lower case letters with upper case subscripts (*e.g.* $v_{GS}, i_D, v_R, i_R$) denote the total value: $v_{GS} = V_{GS} + v_{gs}$, $i_R = I_R + i_r$, *etc.*

3. Bias is the state system (currents and voltages in all elements) when there is no signal. Bias is constant in time (it may vary very slowly compared to the signal). In general, bias is NOT the DC component of the total voltage/current as the signal may have a DC component!

The purpose of bias is to ensure that MOS is in saturation at all times. We will use transistor models developed in Sections 3 and 4 to find the bias point of a transistor. However, special circuits are necessary in order to ensure that MOS remains in saturation at all times. These bias circuits are discussed in Section 5.2.

4. The "total" voltages and currents follow the *iv* equation of each respective elements. Similarly the bias voltages and currents follow the *iv* equation of each respective elements.

5. Signal voltages and currents are the difference between the total value and the bias value (*e.g.*, $v_{gs} = v_{GS} - V_{GS}$, $i_d = i_D - I_D$, $v_r = v_R - V_R$). "Signal" voltages and currents do NOT necessarily follow the *iv* equation of elements.

   In Section 3, we will compute the the *iv* equation for each element with respect to signal voltages/currents (*e.g.*, $i_d$ in terms $v_{gs}$ and $v_{ds}$). As these "signal" *iv* equations may be different than the original *iv* equation of that element, the signal circuit will look different than the original circuit. This is discussed in Section 5.3.

6. **The above observations and conclusions equally apply to a BJT in the active mode.**

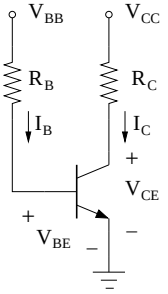
## 5.2 Biasing

The purpose of biasing is to ensure that the BJT remains in the active state (or MOS in saturation) at all times. The major issue faced in biasing is that the location of the bias point can be very sensitive to transistor parameters which may change due to temperature, manufacturing, *etc.*. As such, we need to develop circuits that "force" the bias point to be mostly independent of the transistor parameters.

Bias analysis is similar to the DC analysis of transistors discussed in Sections 3 & 4. Usually, the Early effect in BJTs and Channel-width modulation effect in MOS are ignored in biasing calculations.

### 5.2.1 BJT Fixed Bias

This is the simplest bias circuit and is usually referred to as "fixed bias" as a fixed voltage is applied to the base of the BJT. Assuming that the BJT is in active, we have:




$$\text{BE-KVL:} \quad V_{BB} = I_B R_B + V_{BE} \quad \rightarrow \quad I_B = \frac{V_{BB} - V_{BE}}{R_B}$$

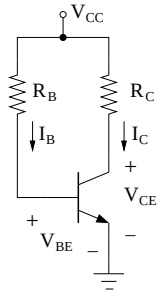
$$I_C = \beta I_B = \beta \frac{V_{BB} - V_{BE}}{R_B}$$

$$\text{CE-KVL:} \quad V_{CC} = I_C R_C + V_{CE} \quad \rightarrow \quad V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = V_{CC} - \beta \frac{R_C}{R_B}(V_{BB} - V_{BE})$$

For a given circuit (known $R_C$, $R_B$, $V_{BB}$, $V_{CC}$, and BJT $\beta$) the above equations can be solved to find the bias point ($I_B$, $I_C$, and $V_{CE}$). Alternatively, one can use the above equations to design a BJT circuit to operate at a certain bias point. (Note: Do not memorize the above equations or use them as formulas, they can be easily derived from simple KVLs).

**Example 1:** Find values of $R_C$, $R_B$ in the above circuit with $\beta = 100$ and $V_{CC} = 15$ V so that the bias point is at $I_C = 25$ mA and $V_{CE} = 7.5$ V.




Since $V_{CE} = 7.5 > V_{D0}$, BJT is in active and $I_B = I_C/\beta = 0.25$ mA:

$$\text{BE-KVL:} \quad V_{CC} + R_B I_B + V_{BE} = 0 \quad \rightarrow \quad R_B = \frac{15 - 0.7}{0.250} = 57.2 \text{ k}\Omega$$

$$\text{CE-KVL:} \quad V_{CC} = I_C R_C + V_{CE}$$

$$15 = 25 \times 10^{-3} R_C + 7.5 \quad \rightarrow \quad R_C = 300 \ \Omega$$

**Example 2:** Consider the circuit designed in example 1. Compute the bias values if $\beta = 200$.

We have $R_B = 57.2$ k$\Omega$, $R_C = 300$ $\Omega$, and $V_{CC} = 15$ V but $I_B$, $I_C$, and $V_{CE}$ are unknown. Assuming that the BJT is in the active mode:

$$\text{BE-KVL:} \quad V_{CC} + R_B I_B + V_{BE} = 0 \quad \rightarrow \quad I_B = \frac{V_{CC} - V_{BE}}{R_B} = 0.25 \text{ mA}$$

$$I_C = \beta \, I_B = 50 \text{ mA}$$

$$\text{CE-KVL:} \quad V_{CC} = I_C R_C + V_{CE} \quad \rightarrow \quad V_{CE} = 15 - 300 \times 50 \times 10^{-3} = 0$$

As $V_{CE} < V_{D0}$ the BJT is not in the active state (since $I_C > 0$, it should be in saturation).

The above examples show the problem with the fixed-bias circuit as the $\beta$ of a commercial BJT can depart substantially from its average value (*e.g.,* due to temperature change). In a given BJT, $I_C$ increases by 9% per °C for a fixed $V_{BE}$ (because of the change in $\beta$). Consider a circuit which is designed to operate perfectly at 25°C. At 35°C, $\beta$ and $I_C$ will be roughly doubled and the BJT can be in saturation!

The problem is that our biasing circuit fixes the value of $I_B$ and, as a result, both $I_C$ and $V_{CE}$ are directly proportional to $\beta$ (see formulas in the previous page). As conditions for a BJT to be in active are $V_{CE} \geq V_{D0}$ and $I_C > 0$, changes in the BJT $\beta$ would change the bias point.

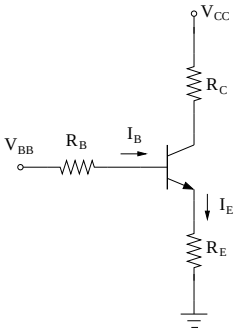
The solution is to design the circuit such that it would "force" $I_C$ to be a certain value (such that $V_{CE} \geq V_{D0}$ through CE-KCL). Then, even if $\beta$ changes, $I_C$ and $V_{CE}$ will remain fixed (BJT changes its $I_B$ to match the new $\beta$ value).

There are two main techniques to achieve this as are discussed below.

### 5.2.2 BJT Bias with Emitter Degeneration

**Bias Arrangement**

The key to this biasing scheme is the emitter resistor which provides negative feedback. It is called "emitter degeneration" as the presence of $R_E$ makes the circuit to behave very differently than when $R_E$ is not present.




$$I_C = \beta I_B, \qquad I_E = (\beta+1) I_B$$

BE-KVL: $$V_{BB} = R_B I_B + V_{BE} + I_E R_E \quad \rightarrow \quad I_B = \frac{V_{BB} - V_{BE}}{R_B + (1+\beta) R_E}$$

CE-KVL: $$V_{CC} = R_C I_C + V_{CE} + I_E R_E \quad \rightarrow \quad V_{CE} = V_{CC} - I_C \left[ R_C + \frac{1+\beta}{\beta} R_E \right]$$

If we choose $R_B$ such that $\underline{R_B \ll (1+\beta) R_E}$ (condition for the feedback to be effective):

$$I_B \approx \frac{V_{BB} - V_{BE}}{(1+\beta) R_E}, \qquad I_C \approx I_E \approx \frac{V_{BB} - V_{BE}}{R_E}$$

$$V_{CE} \approx V_{CC} - \frac{R_C + R_E}{R_E} (V_{BB} - V_{BE})$$

where we have used $(1+\beta)/\beta \approx 1$. Note that now both $I_C$ and $V_{CE}$ are independent of $\beta$.

To see how this circuit works, consider BE-KVL: $V_{BB} = R_B I_B + V_{BE} + I_E R_E$. If we choose $R_B \ll (1+\beta)R_E \approx (I_E/I_B)R_E$, then $R_B I_B \ll I_E R_E$. KVL reduces to $V_{BB} \approx V_{BE} + I_E R_E$. which forces a constant $I_E \approx I_C$ independent of the $\beta$. If BJT $\beta$ changes (*e.g.,* a change in temperature), the circuit forces $I_E \approx I_C$ to remain fixed and BJT changes $I_B$.

As $\beta$ varies due to temperature, manufacturing, *etc.*, we need to ensure that the above condition is satisfied for all possible values of $\beta$. As such, we need to set $R_B \ll (1+\beta_{min})R_E$.

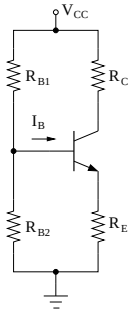
Another important point follows from $V_{BB} \approx V_{BE} + I_E R_E$. As $V_{BE}$ is not a constant and can change slightly (can drop to 0.6 or increase to 0.8 V for a Si BJT), we need to ensure that $I_E R_E$ is much larger than these possible changes in $V_{BE}$. As changes in $V_{BE}$ is about 0.1 V, we need to ensure that $I_E R_E \gg 0.1$ or $I_E R_E > 10 \times 0.1 = 1$ V.

The condition of $R_B \leq (1+\beta_{min})R_E$ implies that we should choose the smallest possible value for $R_B$. In fact, eliminating $R_B$ completely ($R_B = 0$) results in a great flexibility in choosing $R_E$. However, in some cases (such as biasing with a voltage divider, below), $R_B$ is necessary. In these cases, we want $R_B$ to be as large possible as $R_B$ affects the amplifier input resistance (discussed in Section 6). A very good compromise between these two conflicting requirements is to set $R_B = 0.1(1+\beta_{min})R_E$.

Therefore, the stable bias conditions are:

$$R_B = 0 \qquad \text{or} \qquad R_B = 0.1(1+\beta_{min})R_E \approx 0.1\beta_{min}R_E$$
$$I_E R_E \geq 1 \text{ V}$$

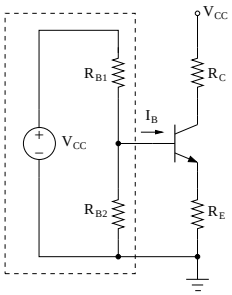
**Bias with one power supply (Voltage divider)**

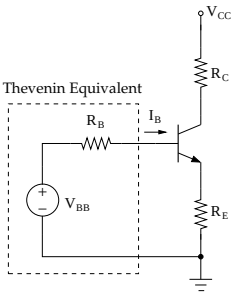



The basic arrangement for bias with emitter degeneration requires a power supply at the base ($V_{BB}$). The base bias voltage can be provided by a voltage divider as is shown, resulting in a circuit that requires only one power supply.

This arrangement is exactly the same as the the bias arrangement if we replace the voltage divider (portion in the dashed box) with its Thevenin equivalent as is shown below with

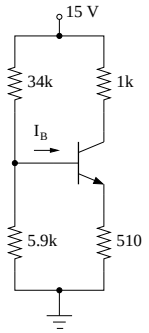
$$V_{BB} = \frac{R_{B2}}{R_{B1}+R_{B2}} V_{CC}$$
$$R_B = R_{B1} \parallel R_{B2}$$



**Example:** Find the bias point of the BJT (Si BJT with $\beta = 200$ and $V_A = \infty$).

Assume BJT in active. Replace the voltage divider by its Thevenin equivalent:




$$R_B = R_{B1} \parallel R_{B2} = 34 \text{ k} \parallel 5.9 \text{ k} = 5.03 \text{ k}$$

$$V_{BB} = \frac{R_{B2}}{R_{B1} + R_{B2}} V_{CC} = \frac{5.9 \text{ k}}{34 \text{ k} + 5.9 \text{ k}} \times 15 = 2.22 \text{ V}$$

BE-KVL: $V_{BB} = R_B I_B + V_{BE} + R_E I_E$

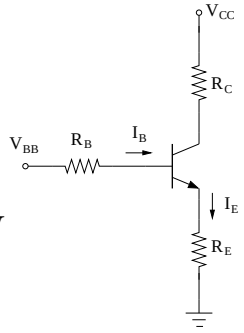
$$2.22 = 5.03 \times 10^3 I_E(\beta + 1) + 0.7 + 510 I_E$$

$$I_E = 2.84 \text{ mA} \qquad I_C = I_E \times (\beta)/(\beta + 1) \approx 2.84 \text{ mA}$$

$$I_B = I_E/(\beta + 1) = 14.1 \ \mu\text{A}$$

CE-KVL: $V_{CC} = R_C I_C + V_{CE} + R_E I_E$

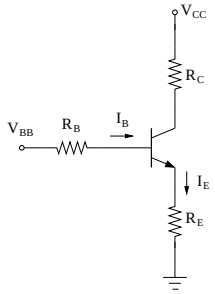
$$15 = (10^3 + 510) \times 2.84 \times 10^{-3} + V_{CE} \quad \rightarrow \quad V_{CE} = 10.7 \text{ V}$$




Since $V_{CE} > V_{D0} = 0.7$ V, assumption of BJT in active is justified.

**Example:** Design a BJT bias circuit (emitter degeneration with voltage divider) such that $I_C = 2.5$ mA and $V_{CE} = 7.5$ V. ($V_{CC} = 15$ V, Si BJT with $\beta$ ranging from 50 to 200 and $V_A = \infty$)

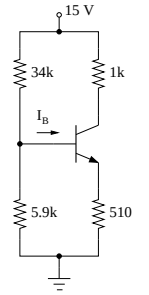
Prototype of the circuit is shown:




Step 1: Find $R_C$ and $R_E$:

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \quad \rightarrow \quad R_C + R_E = \frac{7.5}{2.5 \times 10^{-3}} = 3 \text{ k}\Omega$$

We are free to choose either $R_C$ or $R_E$ (we will see that the amplifier response sets the values of $R_C$ and $R_E$). However, we need $V_E = I_E R_E > 1$ V or $R_E > 1/I_E = 400 \ \Omega$. Let's choose $R_E = 1$ k$\Omega$ which gives $R_C = 3 - R_E = 2$ k$\Omega$ (both commercial values).




Step 2: Find $R_B$ and $V_{BB}$: Since $R_B$ is necessary, we set:

$$R_B = 0.1(1 + \beta_{min}) R_E = 0.1 * 51 * 1,000 = 5.1 \text{ k}\Omega$$

$$V_{BB} \approx V_{BE} + I_E R_E = 0.7 + 2.5 \times 10^{-3} \times 10^3 = 3.2 \text{ V}$$

Step 3: Find $R_{B1}$ and $R_{B2}$

$$R_B = R_{B1} \parallel R_{B2} = \frac{R_{B1}R_{B2}}{R_{B1}+R_{B2}} = 5.1 \text{ k}\Omega$$
$$\frac{V_{BB}}{V_{CC}} = \frac{R_{B2}}{R_{B1}+R_{B2}} = \frac{3.2}{15} = 0.21$$

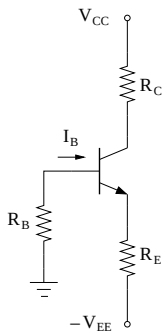
The above are two equations in 2 unknowns ($R_{B1}$ and $R_{B2}$). The easiest way to solve them is to divide the two equations to find $R_{B1}$ and use use the resultant $R_{B1}$ in the $V_{BB}$ equation:

$$R_{B1} = \frac{5.1 \text{ k}\Omega}{0.21} = 24 \text{ k}\Omega$$
$$\frac{R_{B2}}{R_{B1}+R_{B2}} = 0.21 \quad \rightarrow \quad 0.79R_{B2} = 0.21R_{B1} \quad \rightarrow \quad R_{B2} = 6.4 \text{ k}\Omega$$

Reasonable commercial values for $R_{B1}$ and $R_{B2}$ are and 24 kΩ and 6.2 kΩ, respectively.

**Bias with two power supply (grounded base)**

In some cases, we would like to have a "zero" bias voltage at the base of the BJT. This scheme is similar to the basic arrangement method as

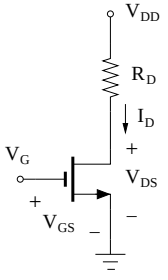



BE-KVL: $$R_B I_B + V_{BE} + R_E I_E - V_{EE} = 0$$
$$V_{EE} = R_B I_B + V_{BE} + R_E I_E$$

which is exactly the BE-KVL for the basic arrangement (with $V_{BB}$ replaced with $V_{EE}$.)

### 5.2.3 MOS Fixed Bias

The fixed-bias scheme for a MOS is shown. Note that because $I_G = 0$, there is no need for a resistor in the gate circuit (while a BJT needs $R_B$ for fixed bias). Since $V_{GS} = V_G$:



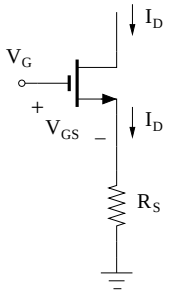

$$I_D = 0.5\mu_n C_{ox}(W/L)_n(V_G - V_t)^2$$
DS-KVL: $$V_{DS} = V_{DD} - I_D R_D = V_{DD} - 0.5\mu_n C_{ox} R_D (V_G - V_t)^2$$

The above two equations can be solved to find $I_D$ and $V_{DS}$.

This is NOT a good biasing scheme as both $V_t$ and $\mu_n C_{ox}(W/L)_n$ vary due to the manufacturing variation and temperature (similar to the BJT $\beta$). For example, as temperature is increased, both $V_t$ and $\mu_n$ decrease: decreasing $\mu_n$ reduces $I_D$ while decreasing $V_t$ raises $I_D$. The net effect (usually) is that $I_D$ decreases. Similar to the case of the BJT, MOS can easily move out of saturation. We need to bias the transistor such that $I_D$ is forced to take the desired value.

### 5.2.4 MOS Bias with Source Degeneration

Addition of a resistor $R_S$ provides the negative feedback necessary to stabilize the bias point (similar to BJT emitter degeneration).




GS-KVL: $\quad V_G = V_{GS} + R_S I_D$

If we choose $R_S$ such that $R_S I_D \gg V_{GS}$, then GS-KVL above gives, $I_D \approx V_G/R_S$ which is a constant and independent of MOS parameters.

It is usually difficult to satisfy $R_S I_D \gg V_{GS}$ condition. Fortunately, even $R_S I_D \geq 2V_{GS}$ is usually sufficient to stabilize the bias point (within 10%).

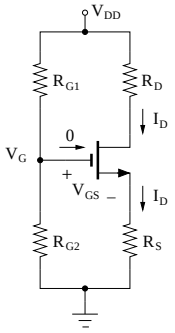
To see the negative feedback action of $R_S$, we note

$$I_D = 0.5\mu_n C_{ox}(W/L)_n(V_G - V_t)^2$$

Since $V_{GS} = V_G - R_S I_D$, any decrease in $I_D$ would increase $V_{GS}$ which would result in an increase $I_D$. Similarly, any increase in $I_D$ would decrease $V_{GS}$ and decreases $I_D$. As a result, $I_D$ will stay nearly constant.

**Bias with one power supply (Voltage divider)**

The basic arrangement for bias with source degeneration requires a power supply at the gate ($V_G$). The gate bias voltage can be provided by a voltage divider as is shown below, resulting in a circuit that requires only one power supply. Since $I_G = 0$ in MOS, there is no need to replace the voltage divider with its Thevenin equivalent as:

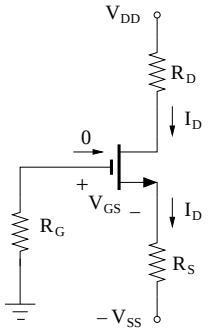



$$V_G = \frac{R_{G2}}{R_{G1} + R_{G2}} V_{DD}$$

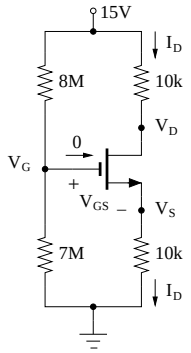
Note that in the case of BJT emitter degeneration bias with a voltage divider, we had to ensure that $R_B = R_{B1} \parallel R_{B2} \ll (1+\beta_{min})R_E$ for negative feedback to be effective. This generally limits the value of $R_{B1}$ and $R_{B2}$. No such limitation exists for a MOS and $R_{G1}$ and $R_{G2}$ can be taken to be large (MΩ).

**Bias with two power supply (grounded gate)**

Similar to the BJT case, two voltage sources can be used as is shown. Resistor $R_G$ is NOT necessary for bias but may be needed for coupling the signal to the circuit.




**Example:** Find the bias point of the MOS ($V_t = 1$ V, $\mu_n C_{ox}(W/L) = 1$ mA/V$^2$ and ignore channel-width modulation).




Assume MOS in saturation:

$$V_G = \frac{7\text{ M}}{7\text{ M} + 8\text{ M}} \times 15 = 7\text{ V}$$

$$I_D = 0.5\mu_n C_{ox}(W/L)V_{OV}^2$$

GS-KVL: $$V_G = 7 = V_{GS} + R_S I_D = V_{OV} + 1 + 10^4 I_D$$

Substituting for $I_D$ in GS-KVL, we get a quadratic equation for $V_{OV}$:

$$10^4 \times 0.5 \times 10^{-3} V_{OV}^2 + V_{OV} - 6 = 0$$

$$5V_{OV}^2 + V_{OV} - 6 = 0$$

Only the positive root, $V_{OV} = 1$ V is physical. It is usually beneficial to compute the node voltages at the transistor terminals (instead of $V_{GS}$, etc):

$$V_{GS} = V_{OV} + 1 = 2\text{ V}$$

$$V_S = V_G - V_{GS} = 7 - 2 = 5\text{ V}$$

Ohm Law : $$I_D = V_S/R_S = 0.5\text{ mA}$$

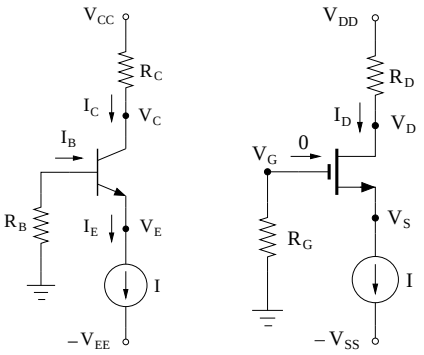
DS-KVL: $$15 = R_D I_D + V_D \quad \rightarrow \quad V_D = 15 - R_D I_D = 10\text{ V}$$

$$V_{DS} = V_D - V_S = 10 - 5 = 5\text{ V}$$

Since $V_{DS} > V_{OV}$, our assumption of MOS in saturation is justified.

### 5.2.5 Biasing with Current Mirrors

As discussed before, stable bias requires that the circuit to be designed to "set" the value of $I_C$ in a BJT (or $I_D$ in a MOS). This objective can be achieved if we use a "current source" to bias the transistor as are shown.

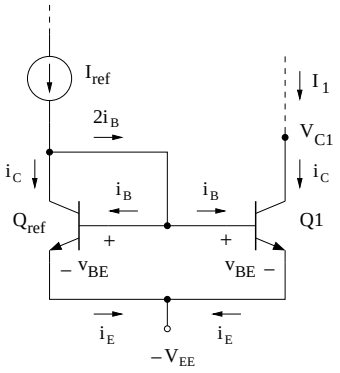



By using a current source, no bias resistor is needed and we only need to include resistors necessary for signal amplification. As such, integrated circuit chips use this technique for biasing as resistors take a lot of space on a chip compared to transistors.

For this biasing to work, we need to develop a circuit which acts as a current source. Examples are current mirror and current steering circuits.

**BJT current mirror circuits**:

This circuit is made of two identical BJTs. Transistor Qref is ON because current $I_{ref}$ flows into Qref. Furthermore, the collector of Qref is connected to its base with $v_{CE,ref} = v_{BE,ref} = V_{D0}$. Thus, Qref has to be in the active state.

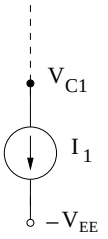



The base and the emitter of Qref are connected to the base and the emitter of Q1 so that $v_{BE,ref} = v_{BE1} = v_{BE}$. Assuming that Q2 is in active and since transistors are identical, this leads to $I_{C,ref} = I_{C1} \equiv I_C$ (if we ignore the Early effect). Similarly, $I_{B,ref} = I_{B1} \equiv I_B$ and $I_{E,ref} = I_{E1} \equiv I_E$:

$$I_B = \frac{I_C}{\beta}, \qquad I_1 = I_C = \beta I_B$$

KCL: $$I_{ref} = I_C + 2I_B = (\beta + 2)I_B$$

$$\frac{I_1}{I_{ref}} = \frac{\beta}{\beta + 2} = \frac{1}{1 + 2/\beta}$$



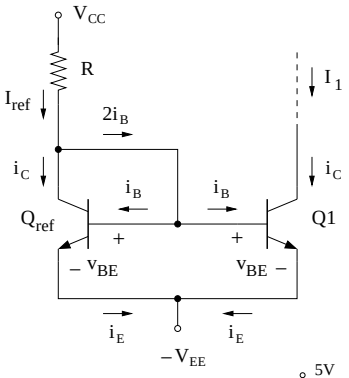

For $\beta \gg 1$, $I_1 \approx I_{ref}$ (with an accuracy of $2/\beta$). This circuit is called a "current mirror" as the two transistors work in tandem to ensure $I_1 \approx I_{ref}$.

This circuit is a two-terminal network (two wires coming out are at $V_{C1}$ and $-V_{EE}$, see above figure). Since the current $I_1$ is constant regardless of the voltage between its two terminals, this circuit acts as a current source.

Note that we had assumed that Q1 is in active. This requires that $V_{CE1} = V_{C1} + V_{EE} \geq V_{D0}$.

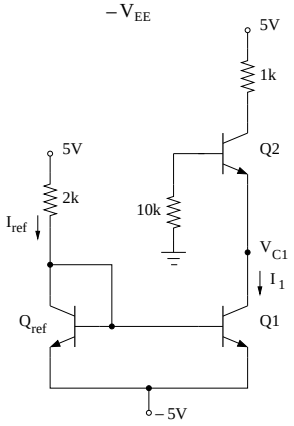
Value of $I_{ref}$ can be set in many ways. The simplest is by using a resistor $R$ as is shown. By KVL, we have:

$$V_{CC} = RI_{ref} + V_{BE,ref} - V_{EE}$$
$$I_{ref} = \frac{V_{CC} + V_{EE} - V_{D0}}{} = const$$



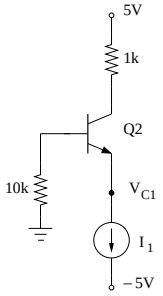

**Example:** Find the bias point of Q2 (Si BJTs with $\beta = 100$).

Qref and Q1 from a current mirror. Therefore, $I_1 \approx I_{ref}$ as long as Q1 is in active. Value of $I_{ref}$ is found from:




$$\text{CE(ref)-KVL:} \quad 5 = 2 \times 10^3 I_{ref} + V_{BE,ref} + (-5)$$
$$I_{ref} = 4.65 \text{ mA}$$
$$I_1 \approx I_{ref} = 4.65 \text{ mA}$$

We replace the Qref and Q1 current mirror with a current source to arrive at the circuit shown for Q2. We still need to prove that Q1 is in active for the current mirror to work (proved later). Since $I_{E2} = I_1 = 4.65$ mA, Q2 should be ON. Assuming Q2 in active:




$$I_{B2} = I_{E2}/(1+\beta) = 46\ \mu\text{A}, \quad I_{C2} \approx I_{E2} = 4.65 \text{ mA}$$
$$\text{BE2-KVL:} \quad 0 = 10 \times 10^3 I_{B2} + V_{BE2} + V_{E2} \quad \rightarrow \quad V_{E2} = V_{C1} = -1.16 \text{ V}$$
$$\text{CE2-KVL:} \quad 5 = 10^3 I_{C2} + V_{CE2} + V_{E2} = 4.65 + V_{CE2} - (-1.16)$$
$$V_{CE2} = 1.51 \text{ V}$$

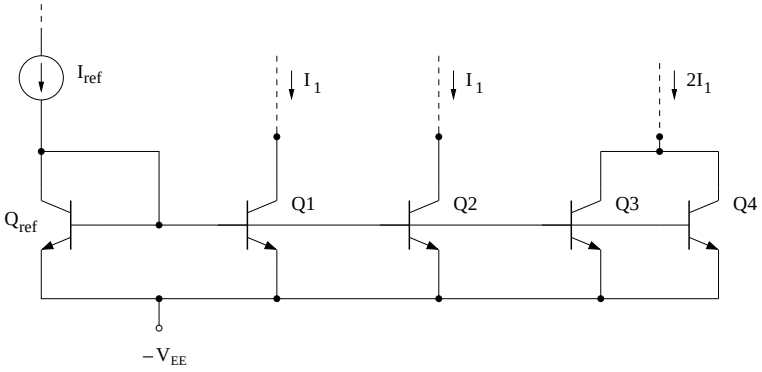
As $V_{CE2} = 1.515 > V_{D0} = 0.7$ V, assumption of Q2 in active is justified.

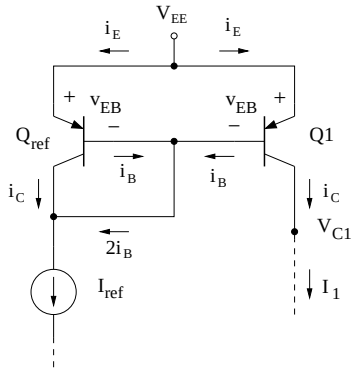
We also need to show that the current mirror acts properly, *i.e.,* Q1 is in active. We find $V_{CE1} = V_{C1} - (-5) = 3.49 > V_{D0}$.

In the simple current mirror circuit above, $I_1 \approx I_{ref}$ with a relative accuracy of $2/\beta$ and $I_{ref}$ is constant with an accuracy of small changes in $V_{BE1}$. Variations of the above current mirror, such as Wilson current mirror and Widlar current mirror, have $I_1 \approx I_{ref}$ with a higher accuracy (*e.g.,* $1/\beta^2$) and also can compensate for the small changes in $V_{BE}$ (See Problems). Wilson current mirror is especially popular because it replace $R$ with a transistor.

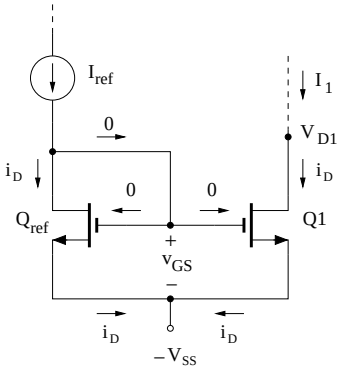
The right hand portion of the current mirror circuit can be duplicated such that one current mirror circuit can bias several BJT circuits as is shown. In fact, by coupling output of two or

more of the right hand BJTs, integer multiples of $I_{ref}$ can be made for biasing circuits which require a higher bias current as is shown below (left figure). Similarly, a current mirror can be constructed with the PNP transistors (right figure below).



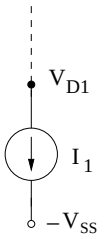




**MOS current steering circuits**:




Similar circuits can be constructed with MOS as is shown. Assume Qref and Q1 are constructed on the same chip and close to each other such that both have the same $\mu_n C_{ox}$ and $V_t$. Transistor Qref is ON because current $I_{ref}$ flows into Qref. Furthermore Qref MOS has to be in saturation as its drain is connected to its gate with $v_{DS,ref} = v_{GS,ref} > v_{GS,ref} - V_t$.

The gate and the source of Qref are connected to the gate and the source of Q1 so that $v_{GS,ref} = v_{GS1} = v_{GS}$. Since gate current is zero, $I_{D,ref} = I_{ref}$. Assuming Q1 is in saturation and ignoring channel-width modulation.

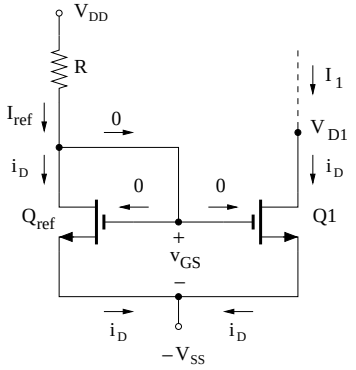



$$I_{ref} = I_{D,ref} = 0.5\mu_n C_{ox}(W/L)_{ref}(V_{GS,ref} - V_t)^2$$
$$I_1 = I_{D1} = 0.5\mu_n C_{ox}(W/L)_1(V_{GS1} - V_t)^2$$
$$\frac{I_1}{I_{ref}} = \frac{(W/L)_1}{(W/L)_{ref}}$$

Similar to the BJT current mirror, this circuit is a current source as the output current $I_1$ is constant and independent of voltage $V_{D1}$.

This circuit works as long as Q1 remains in saturation: $V_{DS1} > V_{OV1} = V_{GS1} - V_t$.

Similar to the BJT current mirror circuit, the value of $I_{ref}$ can be set in many ways. The simplest is by using a resistor $R$ as is shown. By KVL, we have:

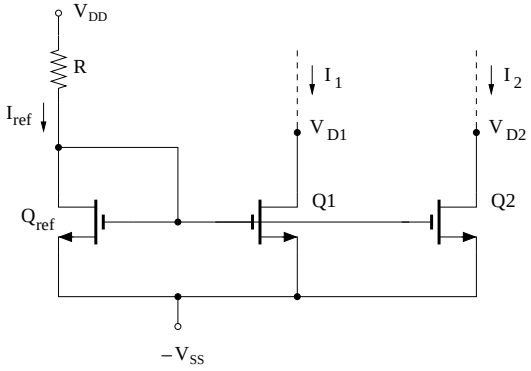


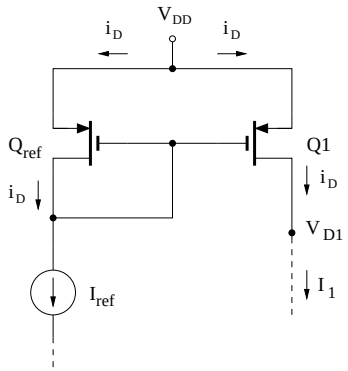

$$V_{DD} = RI_{ref} + V_{GS,ref} - V_{SS}$$

$$I_{ref} = I_{D,ref} = 0.5\mu_n C_{ox}(W/L)_{ref}(V_{GS,ref} - V_t)^2$$

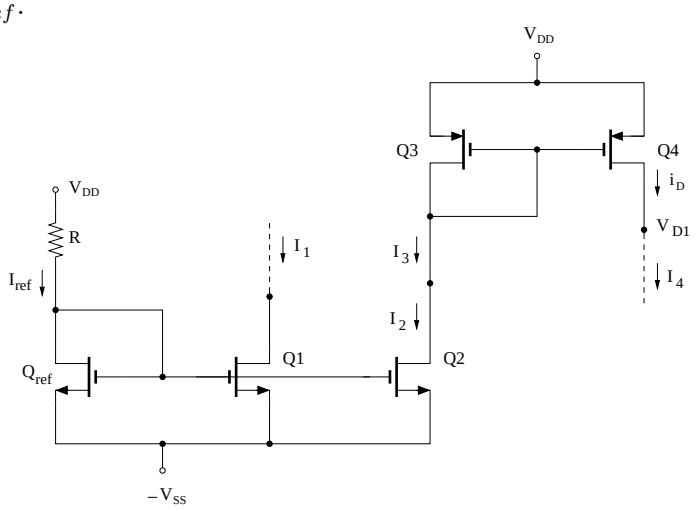
The above equations can be solved to find $V_{GS,ref}$ and $I_{ref}$ (or alternatively, for a desired $I_{ref}$ one can find $V_{GS,ref}$ and $R$).

Similar to a BJT current mirror, the right hand part of the current mirror circuit can be duplicated such that one current mirror circuit can bias several MOS circuits as is shown below (left). MOS allows much greater flexibility as by adjusting $(W/L)$ of each transistor, arbitrary bias currents can be generated (thus MOS circuits are usually called current steering circuits). Similarly, a current mirror can be constructed with the PMOS transistors (figure below, right).




**Exercise:** Find $I_1$ and $I_4$ in terms of $I_{ref}$.



### 5.3 Signal Circuit

We now focus on the response of the circuit and circuit elements to the signal. It is essential to recall that "signal" voltages and currents do NOT necessarily follow the $iv$ characteristics of each element. Therefore, signal circuit may look different than the original circuit. To see this, consider element A with the $iv$ equation $i_A = f(v_A)$. Current and voltage in the element are combinations of bias and signal parts, *e.g.,* $i_A = I_A + i_a$ and $v_A = V_A + v_a$:

$$
\begin{aligned}
&i_A = f(v_A) \\
&I_A = f(V_A) \\
&i_a = i_A - I_A = f(v_A) - f(V_A)
\end{aligned}
$$

Note that in general, $i_a \neq f(v_a)$ and, thus, the signal $iv$ equation can be quite different than the original $iv$ equation of the element A.

In order to arrive at the signal circuit, we need to find signal $iv$ equation of all circuit elements:

Resistors:

$$
\begin{aligned}
&i_R = f(v_R) = \frac{v_R}{R} \qquad I_R = f(V_R) = \frac{V_R}{R} \\
&i_r = i_R - I_R = \frac{v_R - V_R}{R} = \frac{v_r}{R}
\end{aligned}
$$

Therefore, the signal $iv$ equation for a resistor is $v_r = Ri_r$ and a resistor remains as a resistor in the signal circuit.

Capacitor:

$$
\begin{aligned}
&i_C = f(v_C) = C\,\frac{dv_C}{dt} \qquad I_C = f(V_C) = C\,\frac{dV_C}{dt} \\
&i_c = i_C - I_C = C\,\frac{d(v_C - V_C)}{dt} = C\,\frac{dv_c}{dt}
\end{aligned}
$$

Therefore, the signal $iv$ equation for a capacitor is $v_c = Cdv_c/dt$ and a capacitor remains as a capacitor in the signal circuit.

Note that in the bias circuit, $V_C$ is constant. Thus, $I_C = CdV_C/dt = 0$ and capacitor acts as an open circuit in bias calculations.

Independent Voltage Source (IVS):

$$v_{IVS} = f(i_{IVS}) = const = V_S \qquad V_{IVS} = f(I_{IVS}) = const = V_S$$
$$v_{ivs} = v_{IVS} - V_{IVS} = 0$$

Therefore, the signal *iv* equation for an independent source is $v_{ivs} = 0$ (while signal current $i_{ivs}$ is NOT zero). Thus an independent voltage source becomes a short circuit in the signal circuit.

Similarly, one can show that an independent current source becomes an open circuit in the signal circuit.

Diodes (in ON state):

$$i_D = I_s e^{v_D/nV_T} \qquad I_D = I_s e^{V_D/nV_T}$$
$$i_d = i_D - I_D = I_S \left(e^{v_D/nV_T} - e^{V_D/nV_T}\right) = I_S e^{V_D/nV_T} \left(e^{(v_D - V_D)/nV_T} - 1\right)$$
$$i_d = I_D \left(e^{v_d/nV_T} - 1\right)$$

We see that the diode signal *iv* equation: A) is different than the original *iv* equation, B) is non-linear, and C) depends on the bias value, $I_D$.

We assume that signal voltages/currents are small compared to bias values, *i.e.,* the input signal represents a small change in the input ($v_d \ll V_D$) and the output signal represents a corresponding small change in the output ($i_d \ll I_D$). This is called the small signal behavior. We will show that for small signals, non-linear circuit elements (diodes and transistors) behave as linear ones. This is the reason we can build linear circuits with diodes and transistors. Note that for this to work, the non-linear element should be always in ONE particular state (*e.g.,* diode should always be ON).

This small-signal behavior can be understood by noting that any non-linear function can be approximated in the "neighborhood" of a point by its tangent line at that particular point (see figure below). Mathematically, this approximation is based on the Taylor series expansion. Consider *iv* function for element A: $i_A = f(v_A)$. Suppose we know the value of the function $f$ and all of its derivative at some known point $V_A$. Then, the value of the function at $v_A$ can be found from the Taylor Series expansion as:

$$i_A = f(v_A)$$
$$i_A = f(V_A) + (v_A - V_A) \times \left.\frac{df}{dv}\right|_{v=V_A} + \frac{(v_A - V_A)^2}{2!} \times \left.\frac{d^2 f}{dv^2}\right|_{v=V_A} + ...$$
$$i_A = I_A + v_a \times \left.\frac{df}{dv}\right|_{v=V_A} + \frac{v_a^2}{2!} \times \left.\frac{d^2 f}{dv^2}\right|_{v=V_A} + ...$$

If $v_a$ is small (*i.e.,* $v_A$ is close to our original point of $V_A$), the high order terms of this expansion become very small:

$$i_A \approx I_A + v_a \times \left.\frac{df}{dv}\right|_{v=V_A}$$
$$i_a = i_A - I_A = v_a \times \left.\frac{df}{dv}\right|_{v=V_A}$$

As can be seen, the value of the function at a point close to $V_A$ is approximated by the tangent line to $f$ at $V_A$.

Note that the condition for small signal model (dropping high order terms) is:

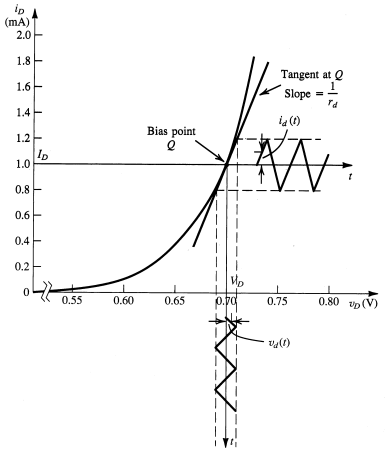
$$\left|\left.\frac{d^2f}{dv^2}\right|_{v=V_A} \times \frac{v_a^2}{2}\right| \ll \left|\left.\frac{df}{dv}\right|_{v=V_A} \times v_a\right| \quad \rightarrow \quad |v_a| \ll 2\left|\left.\frac{df/dv}{d^2f/dv^2}\right|_{v=V_A}\right.$$

Let's apply this approximation to a diode.

### 5.3.1 Diode Small Signal Model

For a diode in forward bias, we have:

$$i_D = f(v_D) = I_s e^{v_D/nV_T} \qquad I_D = f(V_D) = I_s e^{V_D/nV_T}$$
$$i_d \approx v_d \times \left.\frac{df}{dv}\right|_{v=V_D} = v_d \times \left.\left(\frac{1}{nV_T} I_s e^{v_D/nV_T}\right)\right|_{v_D=V_D}$$
$$i_d \approx v_d \times \frac{I_D}{nV_T}$$

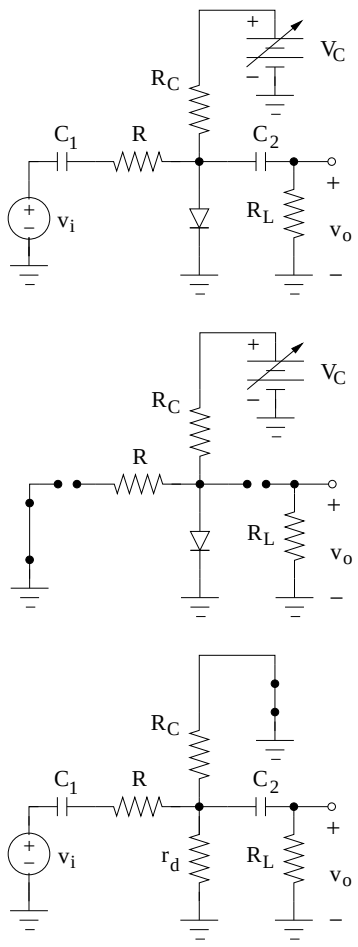



We see that the diode response ($i_d$) to a small signal $v_d$ is linear. Moreover the small-signal $iv$ equation of a diode is the same as that of a resistor, $i_d = v_d/r_d$ with:

$$r_d \equiv \frac{I_D}{nV_T}$$

Note that $r_d$ is the inverse of the slope of a line tangent to $i_D v_D$ characteristics curve of the diode at the bias point, *i.e.,* we are approximating the diode $iv$ characteristic curve with a line tangent to its bias point as is shown in the above figure.

**Example: Voltage-controlled Attenuator**




In this circuit, $v_i$ is a sine wave ($|v_i| << V_{D0}$), $V_C$ is a DC source which biases the diode (and its value can be changed). Capacitors are large (*i.e.,* their impedance is small at the frequency of the signal).

*Bias:* We zero the signal ($v_i$ become a short circuit). Because the voltage source, $V_C$, is a DC source, capacitors become open circuits (see circuit). Then,

$$I_D = \frac{V_C - V_{D0}}{R_C}$$

Because $C_2$ is also open circuit, no voltage appears at $v_o$.

*Signal Circuit:* We short DC bias voltage, $V_C$ ($V_C$ is replaced with ground, see figure). We replace the diode with its small-signal model, $r_d$. We note that $R_C$, $r_d$, and $R_L$ are in parallel (capacitor are both short circuit). Defining $R_p = R_C \parallel r_d \parallel R_L$, we get:

$$\frac{v_o}{v_i} = \frac{R_p}{R_p + R}$$

For $r_D \ll R_C$ and $r_D \ll R_L$, $R_p \approx r_d$ and

$$\frac{v_o}{v_i} = \frac{r_d}{r_d + R}$$
$$r_d = \frac{nV_T}{I_D} = \frac{nV_T R_C}{V_C - V_{D0}}$$

As can be seen, the output voltage $v_o$ depends on $r_d$. Value of $r_d$ is controlled by $V_C$. If $V_C$ increases, $r_d$ is reduced, decreasing $v_o$ for a given $v_i$. Alternatively, reducing $V_C$, increases $r_d$ and $v_o$.

An application of this circuit is in a speakerphone. A frequent problem is that some speakers speak quietly (or are far from the microphone) and some speak loudly (or are close). If $v_i$ is the output of the microphone and $v_o$ is attached to a high-gain amplifier and phone system, a control voltage $V_C$ can compensate for changes in $v_i$ ($V_C$, for example, can be the output of a peak detector circuit with $v_i$ as the input, large $v_i$ makes $V_C$ larger and decreases $v_o/v_i$ in the voltage-controlled attenuator).

### 5.3.2 MOS Small Signal Model

We can develop similar small-signal models for transistors. Let's first take the simpler case of a MOS. We assume that MOS is always in saturation. The NMOS $iv$ characteristics equations are:

$$i_D = f(v_{GS}, v_{DS}) = 0.5\mu_n C_{ox}(W/L)_n(v_{GS} - V_{tn})^2(1 + \lambda v_{DS}) \qquad i_G = 0$$

At the bias, $I_D = f(V_{GS}, V_{DS})$.

We can derive the small signal response of a MOS using a procedure similar to the diode small signal model, *i.e.,* use a Tyler series expansion. The only difference for a MOS is that $i_D$ is a function of TWO variables ($v_{GS}$ and $v_{DS}$). In this case, we should use Taylor series expansion in two variables (around the point $V_{GS}$ and $V_{DS}$). Keeping only the first order terms:

$$i_D = f(v_{GS}, v_{DS})$$

$$i_D \approx f(V_{GS}, V_{DS}) + (v_{GS} - V_{GS}) \times \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{V_{GS},V_{DS}} + (v_{DS} - V_{DS}) \times \left.\frac{\partial i_D}{\partial v_{DS}}\right|_{V_{GS},V_{DS}}$$

$$i_d \approx v_{gs} \times \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{V_{GS},V_{DS}} + v_{ds} \times \left.\frac{\partial i_D}{\partial v_{DS}}\right|_{V_{GS},V_{DS}}$$

Defining

$$g_m \equiv \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{V_{GS},V_{DS}} = 2 \times 0.5\mu_n C_{ox}(W/L)_n(v_{GS} - V_{tn})\,(1 + \lambda v_{DS})|_{V_{GS},V_{DS}}$$

$$g_m = \frac{2}{V_{GS} - V_{tn}} \times \left[0.5\mu_n C_{ox}(W/L)_n(V_{GS} - V_{tn})^2(1 + \lambda V_{DS})\right] = \frac{2I_D}{V_{OV}}$$

and

$$\frac{1}{r_o} \equiv \left.\frac{\partial i_D}{\partial v_{DS}}\right|_{V_{GS},V_{DS}} = \lambda \times [0.5\mu_n C_{ox}(W/L)_n]\,(v_{GS} - V_{tn})^2\Big|_{V_{GS},V_{DS}}$$

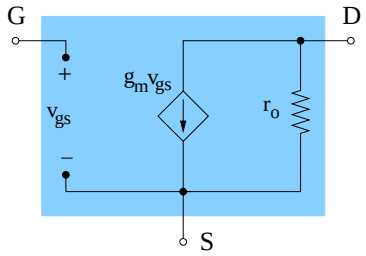
$$\frac{1}{r_o} = \frac{\lambda I_D}{1 + \lambda V_{DS}} \qquad \rightarrow \qquad r_o = \frac{1 + \lambda V_{DS}}{\lambda I_D} \approx \frac{1}{\lambda I_D}$$

Substituting $g_m$ and $r_o$ in the MOS small signal equations we get:

$$i_g = 0 \qquad \text{and} \qquad i_d = g_m v_{gs} + \frac{v_{ds}}{r_o}$$

It is useful to relate the above equations to circuit elements so that we can solve MOS circuits with circuit-analysis tools. The first equation $i_g = 0$ indicates that there is an "open circuit" between gate and source terminals. As $i_d = i_s$, the second equation applies between drain and source terminals. Furthermore, this equation is like a KCL: current $i_d$ is divided into two parts. The first term, $g_m v_{gs}$, is a voltage-controlled current source (as its value does not depend on $v_{ds}$). The second term, $v_{ds}/r_o$, is the Ohm's law for a resistor $r_o$. Thus, the small-signal model for a NMOS is:

$$g_m = \frac{2I_D}{V_{OV}}$$
$$r_o = \frac{1 + \lambda V_{DS}}{\lambda I_D} \approx \frac{1}{\lambda I_D}$$




Similarly, we can derive a small-signal model for a PMOS. The small-signal circuit model for a PMOS looks exactly like that of an NMOS (we do NOT need to replace $v_{gs}$ with $v_{sg}$). PMOS $g_m$ and $r_o$ are the same as those of a NMOS (replace $V_{DS}$ in $r_o$ equation with $V_{SD}$).

We will use this MOS small-signal model to analysis MOS amplifiers in the next section.

### 5.3.3 BJT Small Signal Model

The a small-signal model for BJT can be similarly constructed. We assume that BJT is always in active. The BJT $iv$ equations give values of $i_B$ and $i_C$ in terms of $v_{BE}$ and $v_{CE}$. For NPN transistors:

$$i_B = f_1(v_{BE}) = \frac{I_S}{\beta} e^{v_{BE}/V_T}$$
$$i_C = f_2(v_{BE}, v_{CE}) = I_S e^{v_{BE}/V_T} \left(1 + \frac{v_{CE}}{V_A}\right)$$

Using Taylor series expansion in one variable ($v_{BE}$) for $i_B$ and Taylor series expansion in two variables ($v_{BE}$ and $v_{CE}$) for $i_C$, we get:

$$i_b = v_{be} \times \left.\frac{di_B}{dv_{BE}}\right|_{V_{BE},V_C E}$$
$$i_c = v_{be} \times \left.\frac{\partial i_C}{\partial v_{BE}}\right|_{V_{BE},V_C E} + v_{ce} \times \left.\frac{\partial i_C}{\partial v_{CE}}\right|_{V_{BE},V_C E} +$$

Defining:

$$\frac{1}{r_\pi} \equiv \left.\frac{di_B}{dv_{BE}}\right|_{V_{BE},V_CE} = \frac{1}{V_T} \times \frac{I_S}{\beta}\, e^{V_{BE}/V_T} = \frac{I_B}{V_T} \qquad \rightarrow \qquad r_\pi = \frac{V_T}{I_B}$$

$$g_m \equiv \left.\frac{\partial i_C}{\partial v_{BE}}\right|_{V_{BE},V_CE} = \frac{1}{V_T} \times I_S\, e^{V_{BE}/V_T}\left(1 + \frac{V_{CE}}{V_A}\right) = \frac{I_C}{V_T}$$

$$\frac{1}{r_o} \equiv \left.\frac{\partial i_C}{\partial v_{CE}}\right|_{V_{BE},V_CE} = \frac{1}{V_A} \times I_S\, e^{V_{BE}/V_T} = \frac{I_C}{V_A(1 + V_{CE}/V_A)} = \frac{I_C}{V_A + V_{CE}}$$

we can write small signal model of a BJT as (setting $v_{be} = v_\pi$):

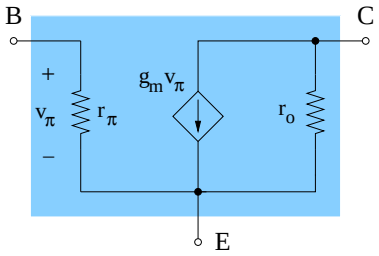
$$i_b = \frac{v_{be}}{r_\pi} \qquad \text{and} \qquad i_c = g_m v_{be} + v_{ce}/r_o$$

Similar to MOS, we relate the above equation to circuit elements to derive a small-signal circuit model for the BJT. The first equation is the statement of Ohm's law between base and emitter terminals (resistor $r_\pi$ between B and E). The right equation is a KCL with a voltage-controlled current source and a resistor (similar to NMOS model).

$$g_m = \frac{I_C}{V_T}$$

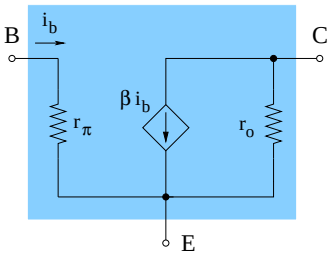
$$r_o = \frac{V_A + V_{CE}}{I_C} \approx \frac{V_A}{I_C}$$

$$r_\pi = \frac{V_T}{I_B} = \frac{V_T}{I_C} \times \frac{I_C}{I_B} = \frac{\beta}{g_m}$$




Similarly, we can derive a small-signal model for a PNP which looks exactly like a NPN.

Since $g_m v_\pi = \beta(v_\pi/r_\pi) = \beta i_\pi$, an alternative model for BJT can be developed using a current-controlled current source as is shown.



## 5.4 Exercise Problems

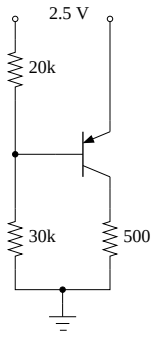
**Problem 1.** Find the bias point of the transistor (Si BJT with $\beta = 100$ and $V_A \to \infty$).

**Problem 2.** Find parameters and state of transistor of problem 1 if $\beta = 200$.

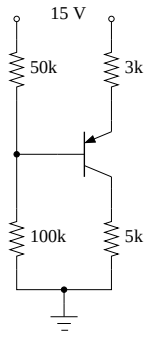
**Problems 3-6.** Find the bias point of the transistor (Si BJTs with $\beta = 200$ and $V_A \to \infty$).

**Problems 7-8.** Find the bias point of the transistor (Si BJTs with $\beta = 100$ and $V_A \to \infty$).

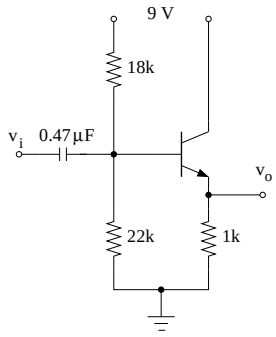
**Problem 9.** In the circuit below with a SI BJT ($V_A \to \infty$), we have measured $V_E = 1.2$ V. Find BJT $\beta$ and $V_{CE}$.



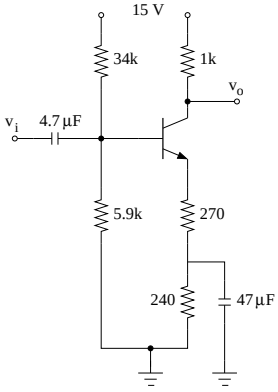

Problem 1



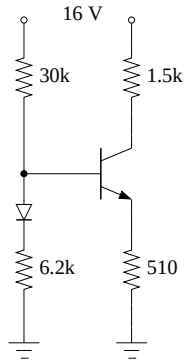

Problem 3



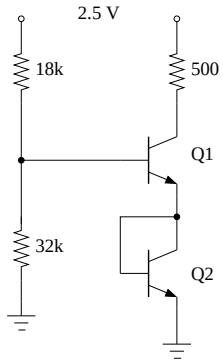

Problem 4



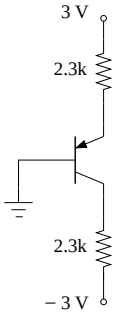

Problem 5



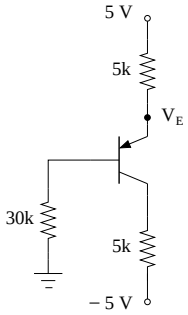

Problem 6




Problem 7




Problem 8




Problem 9

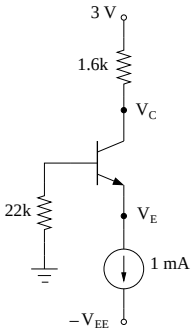
**Problem 10.** Find $V_E$ and $V_C$ (SI BJT with $\beta \to \infty$ and $V_A \to \infty$).

**Problem 11.** Find The bias point of this BJT (ignore Early effect).

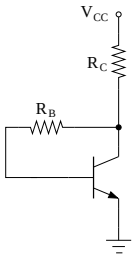
**Problem 12.** Find $R$ such that $V_{DS} = 0.8$ V ($\mu_n C_{ox}(W/L) = 1.6$ mA/V$^2$, $V_{tn} = 0.5$ V, and $\lambda = 0$).

**Problem 13.** Find the bias point of the transistor ($V_{tn} = 1$ V, $\mu_n C_{ox}(W/L) = 0.5$ mA/V$^2$, $\lambda = 0$, and large capacitors).

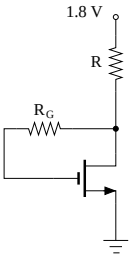
**Problem 14.** Find the bias point of the transistor below ($\mu_p C_{ox}(W/L) = 1$ mA/V$^2$, $V_{tp} = -1$ V, and $\lambda = 0$.



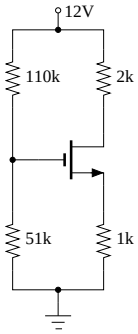
Problem 10



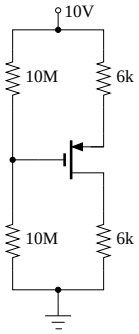
Problem 11



Problem 12



Problem 13



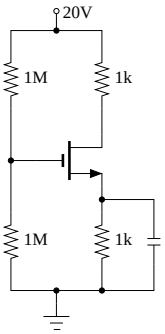
Problem 14

**Problem 15.** Find the bias point of the transistor ($V_{tn} = 3$ V, $\mu_n C_{ox}(W/L) = 0.4$ mA/V$^2$, $\lambda = 0$ and large capacitors).

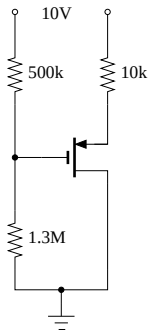
**Problem 16.** Find the bias point of the transistor ($V_{tp} = -4$ V, $\mu_p C_{ox}(W/L) = 0.4$ mA/V$^2$, $\lambda = 0$ and large capacitors).

**Problem 17.** Find $V_D$ and $V_S$ ($\mu_n C_{ox}(W/L) = 1$ mA/V$^2$, $V_{tn} = 2$ V, and $\lambda = 0$).

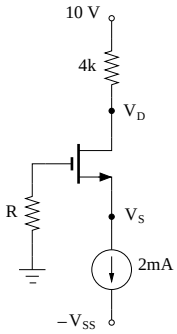
**Problem 18.** Find the bias point of the transistor $V_{tn} = 0.5$ V, ($\mu_n C_{ox}(W/L) = 1.6$ mA/V$^2$, and $\lambda = 0$).



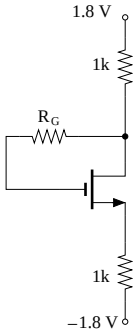
Problem 15



Problem 16

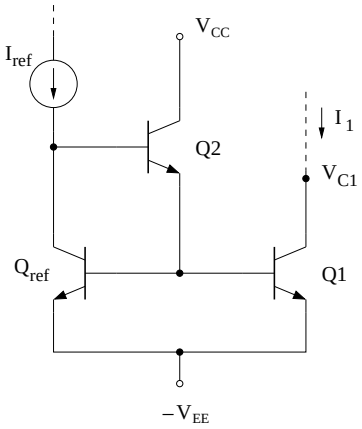


Problem 17

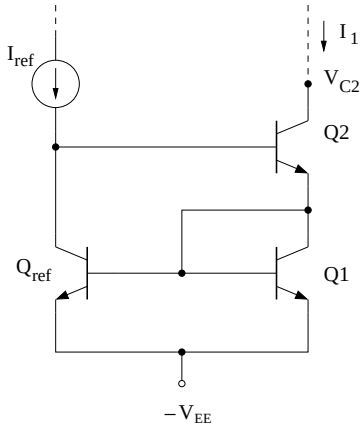


Problem 18

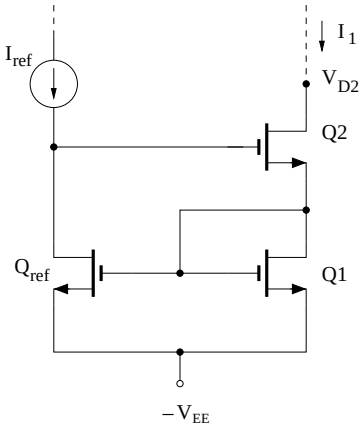
**Problem 19 to 21.** Compute $I_1$ assuming identical transistors.




Problem 19




Problem 20

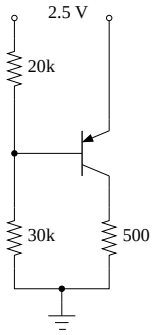



Problem 21

## 5.5 Solution to Selected Exercise Problems

**Problem 1.** Find the bias point of the transistor (Si BJT with $\beta = 100$ and $V_A \to \infty$).

This is a fixed bias scheme (because there is no $R_E$) with a voltage divider providing $V_{BB}$ (it is unstable to temperature changes, see problem 2).




Assuming BJT (PNP) is in active. Replace the voltage divider with its Thevenin equivalent:

$$R_B = 30 \text{ k} \parallel 20 \text{ k} = 12 \text{ k}, \qquad V_{BB} = \frac{30}{30+20} \times 2.5 = 1.5 \text{ V}$$

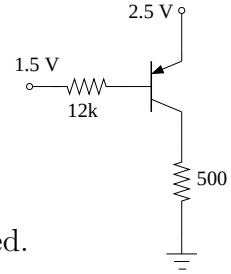
EB-KVL: $2.5 = V_{EB} + 12 \times 10^3 I_B + 1.5$

$$I_B = (2.5 - 1.5 - 0.7)/(12 \times 10^3) = 25 \ \mu\text{A}$$

$$I_C = \beta I_B = 2.5 \text{ mA}$$

EC-KVL: $2.5 = V_{EC} + 500 I_C$

$$V_{EC} = 2.5 - 500 \times 2.5 \times 10^{-3} = 1.25 \text{ V}$$

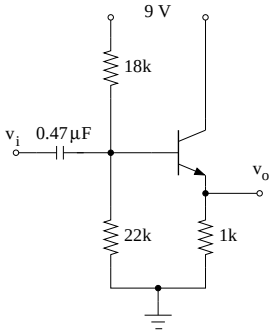



Since $V_{EC} \geq 0.7$ V and $I_C > 0$, the assumption of BJT in active is justified.

Bias Summary: $V_{EC} = 1.25$ V, $I_C = 2.5$ mA, and $I_B = 25$ $\mu$A.

**Problem 4.** Find the bias point (Si BJT with $\beta = 200$ and $V_A \to \infty$).

Assuming BJT (NPN) is in active. Replace the voltage divider with its Thevenin equivalent:




$$R_B = 18 \text{ k} \parallel 22 \text{ k} = 9.9 \text{ k}, \qquad V_{BB} = \frac{22}{18+22} \times 9 = 4.95 \text{ V}$$

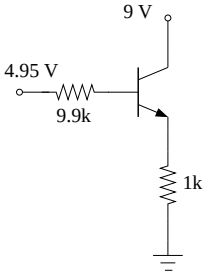
BE-KVL: $V_{BB} = R_B I_B + V_{BE} + 10^3 I_E \qquad I_B = \dfrac{I_E}{1+\beta} = \dfrac{I_E}{201}$

$$4.95 - 0.7 = I_E \left( \frac{9.9 \times 10^3}{201} + 10^3 \right)$$

$$I_E = 4 \text{ mA} \approx I_C, \qquad I_B = \frac{I_C}{\beta} = 20 \ \mu\text{A}$$

CE-KVL: $V_{CC} = V_{CE} + 10^3 I_E$

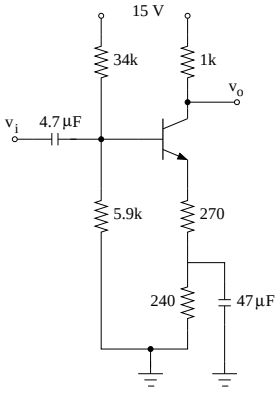
$$V_{CE} = 9 - 10^3 \times 4 \times 10^{-3} = 5 \text{ V}$$




Since $V_{CE} \geq 0.7$ V and $I_C > 0$, assumption of BJT in active is justified.

Bias Summary: $V_{CE} = 5$ V, $I_C = 4$ mA, and $I_B = 20$ $\mu$A.

**Problem 5.** Find the bias point (Si BJT with $\beta = 200$ and $V_A \to \infty$).




Assume BJT (NPN) is in active. Replace the voltage divider with its Thevenin equivalent. Since capacitors are open, the emitter resistance for bias is $270 + 240 = 510\ \Omega$.

$$R_B = 5.9\text{ k} \parallel 34\text{ k} = 5.0\text{ k}, \qquad V_{BB} = \frac{5.9}{5.9+34}\,15 = 2.22\text{ V}$$

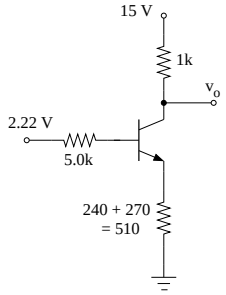
BE-KVL: $\quad V_{BB} = R_B I_B + V_{BE} + 510 I_E \qquad I_B = \dfrac{I_E}{1+\beta} = \dfrac{I_E}{201}$

$$2.22 - 0.7 = I_E\left(\frac{5.0\times 10^3}{201} + 510\right)$$

$$I_E = 3\text{ mA} \approx I_C, \qquad I_B = \frac{I_C}{\beta} = 15\ \mu\text{A}$$

CE-KVL: $\quad V_{CC} = 1000 I_C + V_{CE} + 510 I_E$

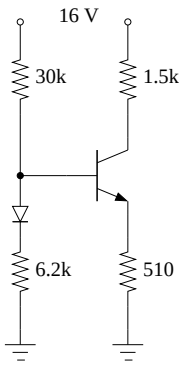
$$V_{CE} = 15 - 1,510 \times 3 \times 10^{-3} = 10.5\text{ V}$$

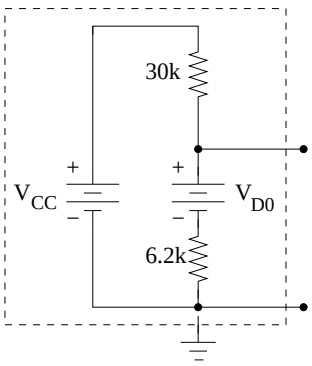


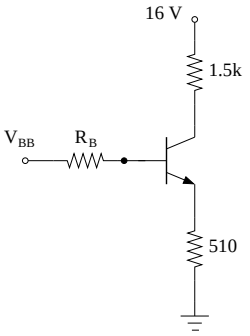

Since $V_{CE} \geq 0.7$ V and $I_C > 0$, assumption of BJT in active is justified.

Bias Summary: $V_{CE} = 10.5$ V, $I_C = 3$ mA, and $I_B = 15\ \mu$A.

**Problem 6.** Find the bias point (Si BJT with $\beta = 200$ and $V_A \to \infty$).




Assuming that the BJT is in active, the base voltage has to be large enough to forward bias the BE junction. Thus, base voltage would be large enough to forward bias the diode. With diode ON, we can find the Thevenin equivalent of the voltage divider part by:)

$$V_{BB} = V_{oc} = \frac{6.2}{30+6.2}\,(V_{CC} - V_{D0}) + V_{D0} = 2.74 + 0.83 V_{D0}\ \text{(V)}$$

$$R_B = R_T = 30\text{ k} \parallel 6.2\text{ k} = 5.14\text{ k}$$

BE-KVL: $V_{BB} = R_B I_B + V_{BE} + 510 I_E$

$$2.74 + 0.83 V_{D0} = 5.14 \times 10^3 \frac{I_E}{201} + V_{D0} + 510 I_E$$

$$I_E = \frac{2.74 - 0.17 V_{D0}}{536} = 4.9 \text{ mA} \approx I_C, \qquad I_B = \frac{I_C}{\beta} = 24 \ \mu\text{A}$$

CE-KVL: $V_{CC} = 1,500 I_C + V_{CE} + 510 I_E$

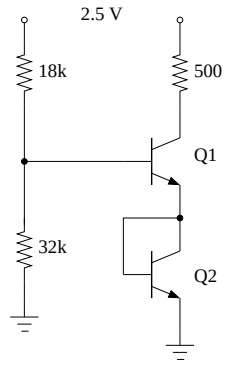
$$V_{CE} = 16 - 2,010 \times 4.9 \times 10^{-3} = 6.15 \text{ V}$$

Since $V_{CE} \geq 0.7$ V and $I_C > 0$, assumption of BJT in active is justified. Note that the dependence of $I_E$ to $V_{D0}$ is reduced by a factor of 6 i.e., $I_E$ now scales as $2.74 - 0.17 V_{D0}$ instead of $2.74 - V_{D0}$ (the case with no diode). As such, changes in $V_{D0}$ due to temperature has a much smaller impact on this circuit (and $R_E I_E \geq 1$ V condition can be relaxed.)

Bias Summary: $V_{CE} = 6.15$ V, $I_C = 4.9$ mA, and $I_B = 24$ $\mu$A.

**Problem 7.** Find the bias point (Si BJTs with $\beta = 100$ and $V_A \to \infty$).

Assume Q1 in active. Replace $R_1/R_2$ voltage divider with its Thevenin equivalent:




$$R_B = 18 \text{ k} \parallel 32 \text{ k} = 11.5 \text{ k}, \qquad V_{BB} = \frac{32}{32 + 18} \times 2.5 = 1.6 \text{ V}$$

BE-KVL: $V_{BB} = R_B I_{B1} + V_{BE1} + V_{BE2}$

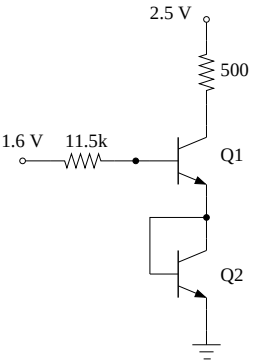
$$I_{B1} = \frac{1.6 - 1.4}{11.5 \times 10^3} = 17.4 \ \mu\text{A}$$

$$I_{C1} = \beta I_{B1} = 1.74 \text{ mA},$$

$$I_{E1} = (\beta + 1) I_{B1} = 1.76 \text{ mA}$$

CE-KVL: $2.5 = 500 I_{C1} + V_{CE1} + V_{BE2}$

$$V_{CE1} = 2.5 - 500 \times 1.74 \times 10^{-3} - 0.7 = 0.93 \text{ V}$$



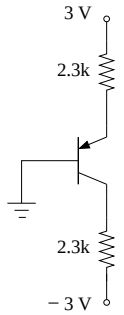

Since $V_{CE1} \geq 0.7$ V and $I_{B1} > 0$, assumption of Q1 active is justified.

For Q2, we note that $V_{CE2} = V_{BE2} = 0.7$ V and $I_{E2} = I_{E1} = 1.76$ mA. So, Q2 should be in active and $I_{B2} = I_{E2}/(1 + \beta) = 17.4$ $\mu$A and $I_{C2} = 1.74$ mA.

Bias Summary: $V_{CE1} = 0.93$ V, $I_{C1} = 1.74$ mA, and $I_{B1} = 17.4$ $\mu$A.

**Problem 8.** Find the bias point of the transistor (Si BJT with $\beta = 100$ and $V_A \to \infty$).

Assume BJT (PNP) in active.




EB-KVL: $3 = 2.3 \times 10^3 I_E + V_{EB}$

$I_E = (3 - 0.7)/(2.3 \times 10^3) = 1$ mA

$I_B = I_E/(\beta + 1) = 10$ $\mu$A

$I_C = \beta I_B = 0.99$ mA

EC-KVL: $3 = 2.3 \times 10^3 I_E + V_{EC} + 2.3 \times 10^3 I_C - 3$

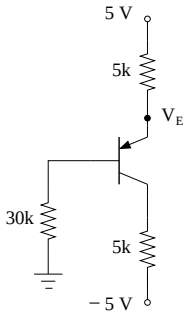
$V_{EC} = 2.4$ V

Since $V_{EC} \geq 0.7$ V and $I_C > 0$, assumption of BJT in active is justified.

Bias Summary: $V_{EC} = 2.4$ V, $I_C = 1$ mA, and $I_B = 10$ $\mu$A.

**problem 9.** In the circuit below with a SI BJT ($V_A \to \infty$), we have measured $V_E = 1.2$ V. Find BJT $\beta$ and $V_{CE}$.

Assume BJT (PNP) in active:




Ohm Law: $5 \times 10^3 I_E = 5 - V_E = 3.8 \quad \to \quad I_E = 0.76$ mA

EB-KVL: $V_E = V_{EB} + 30 \times 10^3 I_B$

$I_B = (1.2 - 0.7)/(30 \times 10^3) = 16.7$ $\mu$A

$I_C = I_E - I_B = 0.74$ mA

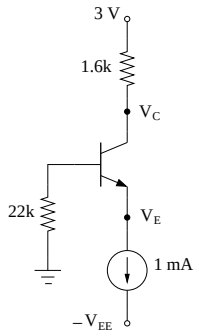
$$\beta = \frac{I_C}{I_B} = \frac{0.74 \times 10^{-3}}{16.7 \times 10^{-6}} \approx 47$$

EC-KVL: $V_E = V_{EC} + 5 \times 10^3 I_C - 5$

$1.2 = V_{EC} + 5 \times 10^3 \times 0.74 \times 10^{-3} - 5 \quad \to \quad V_{EC} = 2.4$ V

Since $V_{EC} \geq 0.7$ V and $I_C > 0$, assumption of BJT in active is justified.

**Problem 10.** Find $V_E$ and $V_C$ (SI BJT with $\beta \to \infty$ and $V_A \to \infty$).




Assume Q1 in active. Since $\beta \to \infty$, then $I_B \to 0$ (this does not mean that BJT is in cut-off, rather $I_B$ is so small that it can be ignored in calculations).:

$$I_E = 1 \text{ mA} \qquad I_C = I_E - I_B = 1 \text{ mA}$$

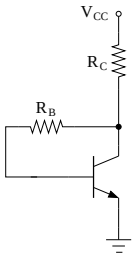
$$\text{BE-KVL} \quad 0 = 22 \times 10^3 I_B + V_{BE} + V_E \quad \to \quad V_E = -0.7 \text{ V}$$

$$\text{KVL} \quad 3 = 1.6 \times 10^3 I_C + V_C \quad \to \quad V_C = 1.4 \text{ V}$$

and $V_{CE} = V_C - V_E = 1.4 - (-0.7) = 2.1$ V. Since $V_{CE} > 0.7$ V and $I_E > 0$, assumption of BJT in active is justified.

Bias Summary: $I_C = 1$ mA and $V_{CE} = 2.1$ V.

**Problem 11.** Find The bias point of this BJT (ignore Early effect).




This is another stable biasing scheme called self Bias. This scheme uses $R_c$ as the feedback resistor. The interesting property of this biasing scheme is that the transistor is always in active state. We write a KVL through BE and CE terminals:

$$V_{CE} = R_B I_B + V_{BE} = R_B I_B + V_{D0} > V_{D0}$$

Since $V_{CE} > V_{D0}$, BJT is always in the active state with $i_C/i_B = \beta$. Noting (by KCL) that $I_1 = I_C + I_B$:

$$\text{BE-KVL:} \quad V_{CC} = R_C I_1 + R_B I_B + V_{BE} = R_C I_C + (R_B + R_C)\frac{I_C}{\beta} + V_{D0}$$

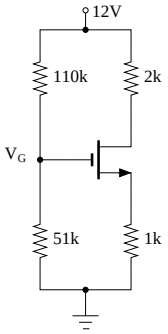
$$I_C = \frac{V_{CC} - V_{D0}}{R_C + (R_C + R_B)/\beta}$$

If, $(R_B + R_C)/\beta \ll R_C$ or $R_B \ll (\beta - 1)R_C$, we will have:

$$I_C \approx \frac{V_{CC} - V_{D0}}{R_C}$$

and the bias point is stable as $I_C$ is independent of $\beta$.

**Problem 13.** Find the bias point of the transistor ($V_{tn} = 1$ V, $\mu_n C_{ox}(W/L) = 0.5$ mA/V$^2$, $\lambda = 0$, and large capacitors).




Since $I_G = 0$,

$$V_G = \frac{51 \text{ k}}{51 \text{ k} + 110 \text{ k}} \times 12 = 3.80 \text{ V}$$

Assume NMOS is in the active state,

$$I_D = 0.5\mu_n C_{ox}(W/L)V_{OV}^2 = 0.5 \times 0.5 \times 10^{-3} V_{OV}^2$$

GS-KVL: $V_G = V_{GS} + 10^3 I_D = V_{OV} + V_t + 10^3 I_D$

$$10^3 I_D + V_{OV} - 2.8 = 0$$

$$10^3 \times 0.25 \times 10^{-3} V_{OV}^2 + V_{OV} - 2.8 = 0$$

$$0.25 V_{OV}^2 + V_{OV} - 2.8 = 0$$

Negative root is not physical. Thus, $V_{OV} = 1.9$ V. $V_{GS} = V_{OV} + V_t = 2.9$ V. Then,

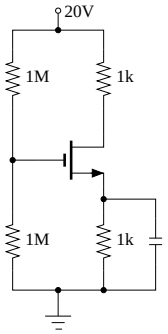
GS-KVL: $3.8 = V_{GS} + 1,000 I_D \quad \rightarrow \quad I_D = 0.9$ mA

DS-KVL: $12 = 2,000 I_D + V_{DS} + 1,000 I_D = V_{DS} + 2.7 \quad \rightarrow \quad V_{DS} = 9.3$ V

As $V_{DS} = 9.3 > V_{OV} = 1.9$ V, our assumption of NMOS in active is correct.

Bias Summary: $V_{GS} = 2.9$ V, $V_{DS} = 9.3$ V, and $I_D = 0.9$ mA.

**Problem 15.** Find the bias point of the transistor ($V_{tn} = 3$ V, $\mu_n C_{ox}(W/L) = 0.4$ mA/V$^2$, $\lambda = 0$ and large capacitors).




Capacitor is open circuit in the bias circuit. Since $I_G = 0$:

$$V_G = \frac{10^6}{10^6 + 10^6} \times 20 = 10 \text{ V}$$

Assume NMOS is in active,

$$I_D = 0.5\mu_n C_{ox}(W/L)V_{OV}^2 = 0.5 \times 0.4 \times 10^{-3} V_{OV}^2$$

GS-KVL: $10 = V_{GS} + 10^3 I_D = V_{OV} + V_t + 10^3 I_D$

$$10^3 \times 0.2 \times 10^{-3} V_{OV}^2 + V_{OV} - 7 = 0$$

$$0.2 V_{OV}^2 + V_{OV} - 7 = 0$$

Negative root is not physical. Thus, $V_{OV} = 3.92$ V. $V_{GS} = V_{OV} + V_t = 6.92$ V. Then,

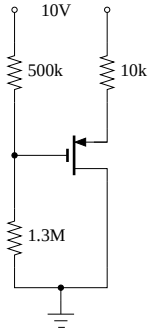
$$\text{GS-KVL:} \quad 10 = 6.92 + 10^3 I_D \quad \rightarrow \quad I_D = 3.08 \text{ mA}$$

$$\text{DS-KVL:} \quad 20 = 10^3 I_D + V_{DS} + 10^3 I_D \quad \rightarrow \quad V_{DS} = 20 - 2 \times 10^3 \times 3.08 \times 10^{-3} = 13.8 \text{ V}$$

Since $V_{DS} = 13.8 > V_{OV} = 3.92$ V, our assumption of NMOS in active state is justified.

Bias summary: $V_{GS} = 6.92$ V, $V_{DS} = 13.8$ V, and $I_D = 3.08$ mA

**Problem 16.** Find the bias point of the transistor ($\mu_p C_{ox}(W/L) = 0.4$ mA/V$^2$, $V_{tp} = -4$ V, and $\lambda = 0$ and large capacitors).




Since $I_G = 0$

$$V_G = \frac{0.5 \text{ M}}{1.3 \text{ M} + 0.5 \text{ M}} \times 18 = 5 \text{ V}$$

Assume PMOS is in the active state,

$$I_D = 0.5 \mu_p C_{ox}(W/L) V_{OV}^2 = 0.5 \times 0.4 \times 10^{-3} V_{OV}^2$$

$$\text{SG-KVL:} \quad 18 = 10^4 I_D + V_{SG} + 5 = 10^4 I_D + V_{OV} + |V_{tp}| + 5$$

$$10^4 \times 0.2 \times 10^{-3} V_{OV}^2 + V_{OV} - (18 - 5 - 4) = 0$$

$$2V_{OV}^2 + V_{OV} - 9 = 0$$

Negative root is not physical. Thus, $V_{OV} = 1.89$ V. $V_{SG} = V_{OV} + |V_{tp}| = 5.89$ V. Then,

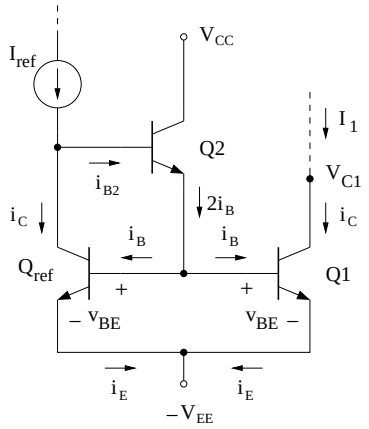
$$\text{SG-KVL:} \quad 18 = 10^4 I_D + V_{SG} + 5 \quad \rightarrow \quad I_D = 0.711 \text{ mA}$$

$$\text{SD-KVL:} \quad 18 = 10^4 I_D + V_{SD} \quad \rightarrow \quad V_{SD} = 18 - 10^4 \times 0.711 \times 10^{-3} = 10.9 \text{ V}$$

Since $V_{SD} = 10.9 > V_{OV} = 1.89$ V, our assumption of PMOS in active is justified.

Bias summary: $V_{SG} = 5.99$ V, $V_{SD} = 10.9$ V, and $I_D = 0.71$ mA

**Problem 19.** Compute $I_1$ assuming identical transistors.




Because the base and the emitter of Qref is atttached to the base and the emitter of Q1, $v_{BE,ref} = v_{BE1} = v_{BE}$. As BJT's are identical, they should have similar $i_B$ ($i_{B1} = i_{B,ref} = i_B$) and, therefore, similar $i_E$ and $i_C$.

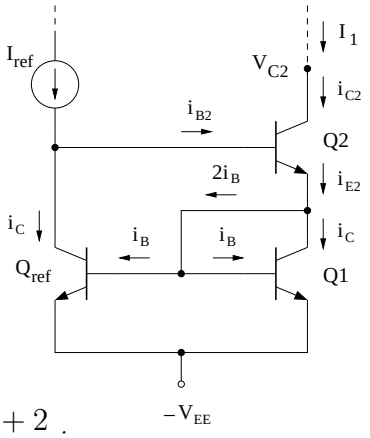
KCL: $\quad i_{E2} = 2i_B \qquad i_{B2} = \dfrac{2i_B}{1+\beta} = \dfrac{2i_c}{\beta(1+\beta)}$

KCL: $\quad I_{ref} = i_C + i_{B2} = i_C \left(1 + \dfrac{2}{\beta(1+\beta)}\right)$

$$\frac{I_{ref}}{i_C} \approx 1 + \frac{2}{\beta^2} \quad \rightarrow \quad \frac{I_1}{I_{ref}} \approx \frac{1}{1+1/\beta^2}$$

where we used $I_1 = i_c$. As can be seen, this is a better current mirror than our simple version as $I_o \approx I_{ref}$ with an accuracy of $2/\beta^2$. Similar to our simple current-mirror circuit, $I_{ref}$ can be set by using a resistor $R$ (*e.g.*, replace $I_{ref}$ with $R$).

**Problem 20.** Compute $I_1$ assuming identical transistors.




Similar to Problem 19, Qref and Q1 have the same $v_{BE}$ and the same $i_B$ and $i_C$ (we are assuming that Q1 is in active).

$$i_B = \frac{i_E}{\beta+1}$$

KCL: $\quad i_{E2} = 2i_B + i_c = \dfrac{2i_E}{\beta+1} + \dfrac{\beta i_E}{\beta+1} = \dfrac{\beta+2}{\beta+1}\, i_E$

$$i_{B2} = \frac{i_{E2}}{\beta+1} = \frac{\beta+2}{(\beta+1)^2}\, i_E$$

KCL: $\quad I_{ref} = i_C + i_{B2} = \dfrac{\beta i_E}{\beta+1} + \dfrac{\beta+2}{(\beta+1)^2}\, i_E = \dfrac{\beta(\beta+1)+\beta+2}{(\beta+1)^2}\, i_E$

$$I_1 = i_{C2} = \frac{\beta}{\beta+1}\, i_{E2} = \frac{\beta(\beta+2)}{(\beta+1)^2}\, i_E$$

$$\frac{I_1}{I_{ref}} = \frac{\beta(\beta+2)}{\beta(\beta+1)+\beta+2} = \frac{\beta(\beta+2)}{\beta(\beta+2)+2} = \frac{1}{1+\dfrac{2}{\beta(\beta+2)}} \approx \frac{1}{1+2/\beta^2}$$

This circuit is called the Wilson current mirror after its inventor. It has a reduced $\beta$ dependence compared to our simple current mirror and has a greater output impedance compared to the current mirror of problem 19.