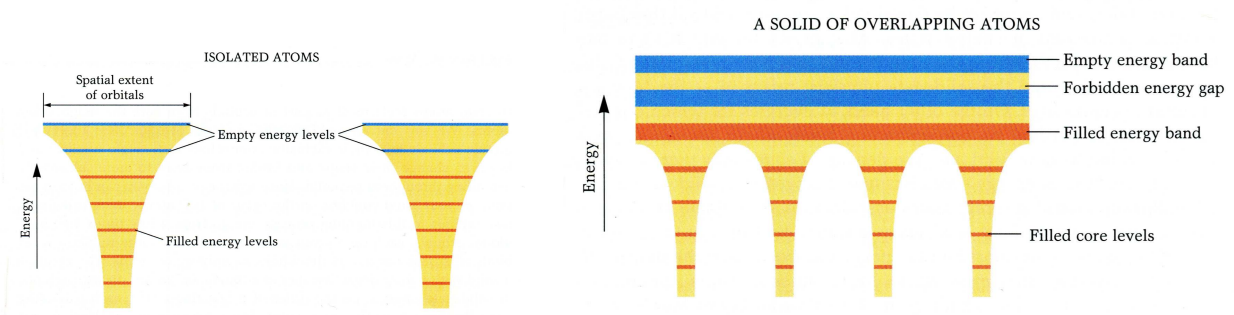
II. Diodes

We start our study of nonlinear circuit elements. These elements (diodes and transistors) are made of semiconductors. A brief description of how semiconductor devices work is first given to understand their iv characteristics. You will see a rigorous analysis of semiconductors in the breadth courses.

2.1 Energy Bands in Solids

In every atom, the nucleus (positively charged) is surrounded by a cloud of electrons. It was first envisioned that the atomic structure would be similar to that of the solar system: the nucleus in the center (similar to the sun), electrons revolving on orbits around the nucleus (planets), and the electric attraction force between the nucleus and electrons being similar to the gravitational force between the sun and planets. However, according to Maxwell's equations, electrons that revolve around a nucleus should emit electromagnetic radiation. As such, electrons should lose their energy gradually and their orbit should decay (in a fraction of a second!). This means that there is a mechanism that would not allow the electrons to lose energy gradually and is one of reasons that the quantum theory was developed.

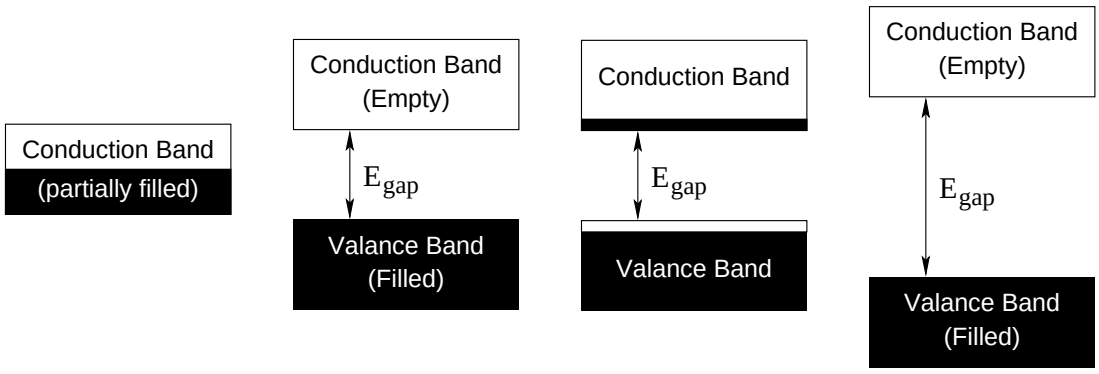
According to the quantum theory electrons revolving around an atom can only have discrete levels of energy as is shown below. Electrons are not allowed to gradually lose or gain energy. They can only "jump" from one energy level to another (by absorbing or emitting a quanta of energy, a photon). Furthermore, there are only a finite number of electrons that are allowed in each state (Pauli's Principle). Therefore, both the energy levels for electrons and the number of electrons at each energy level are specified. Because any system would tend to be in a minimum energy state, electrons in an atom start by "filling" the lowest energy level. Once all allowable slots is filled, electrons start filling the next energy level and so on. Therefore, the electronic structure include "filled" energy levels (all slots are taken by electrons), "empty" energy levels (positions are available but no electron is present), and "partially filled" levels (there are some electrons but there is also room for more electrons). Electrons at each energy level are confined to a region in space called the orbital. Higher energy levels have larger orbital sizes (as is shown in the figure).



When atoms are arranged in a solid, the inter-spacing between atoms can become comparable to the size of electron orbitals of each atom . In this case, the outer orbitals merge into energy bands. Instead of discrete energy levels, electrons in these bands can have continuous values of energy within a "band" of energy. As before, there are range of energies that no electron can occupy. These range of energies are called "Forbidden Gaps." (see the figure above). In addition, electrons in these energy band are not necessarily attached to one atom. They can be shared and/or be free to move around the solid.

The lowest energy band in which electrons can move freely in the material (and not tied to any particular atom) is called the conduction band. The energy band directly below the conduction band is called the valance band in semiconductors and insulators. The energy difference between the top of the valance band and the bottom of the conduction band is called the band-gap of the material.

The electric properties of metals, semiconductors, and insulators can be understood with this picture. As these properties are tied to energy bands and forbidden gaps, we only focus on these bands (see figure below).



Metal | Semiconductor at 0 kelvin | Semiconductor at room temperature | Insulator

In metals, the conduction band is partially filled. As electrons in the partially filled conduction band can easily move around the material, metals can conduct electricity (and heat) very well.

In a semiconductor at 0 kelvin (absolute zero), the valance band is completely filled while the conduction band is completely empty. As such, a semiconductor does not conduct electricity at 0 kelvin. However, the band-gap of a semiconductor is relatively small. At room temperature, the thermal energy in the material is sufficient to move a number of electrons from the valance band into the conduction band. These conduction band electrons can carry electricity as they are free to move around the material.

In addition, promotion of some electrons to the conduction band leaves spaces (or "holes") in the valance band. While electrons in the valance band are tied to atoms, they can "jump" from one hole in the valance band into the next hole and participate in the conduction of electricity. As we are interested only on a small potion of electrons in the conduction band, *i.e.,* those are stepping from one hole to another, it is easier to keep track of the small number of holes in the valance band. In this picture, when electrons move to the left of the material to fill a hole, it would look like the hole is moving to the right. So, in describing semiconductors we usually keep track of negatively charged electrons (those that are in the conduction band) and positively charged holes (electrons in the valance band). Electrons and holes are called the charge carriers in a semiconductor.

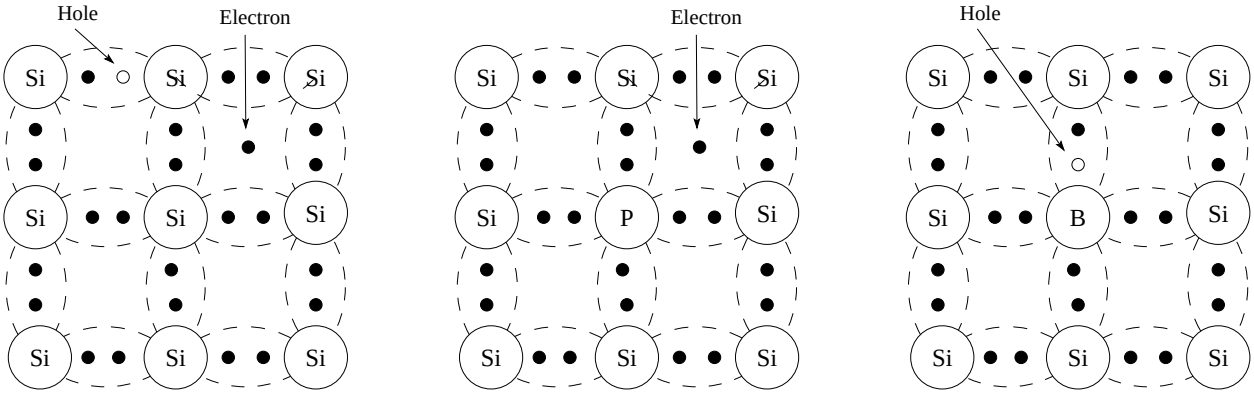
Since at room temperature the number of electrons that are promoted into the conduction band of a semiconductor ($\sim 10^{16}$ /m^3 to 10^{19} /m^3) is much smaller than number of electrons in the partially-filled conduction band of a metal ($\sim 10^{28}$ /m^3 to 10^{29} /m^3), semiconductors conduct electricity but have a much lower conductivity than metals (thus, the name semiconductor). Overall, the properties of semiconductors are very sensitive to temperature as the number of electron/hole pairs increases exponentially with temperature. This is an important effect and should be taken into account in the design of electronic circuits.

Lastly, insulators energy band structure is similar to semiconductors (filled valance band, empty conduction band at 0 kelvin). However, the band-gap of an insulator is several time larger than that of a semiconductor. As such, the number of electrons that can be promoted to the conduction is very small ($\sim 10^7$ /m^3 at room temperature). So, these material are very poor conductors.

2.2 Semiconductors

Semiconductor material are mainly made of elements from group IVB of the periodic table like C (diamond), Si, Ge, SiC. These material have 4 electrons in their outer most electronic shell. Each atom can form a "covalent" bond with four of its neighbors sharing one electron with that atom. In this manner, each atom "sees" eight electrons in its outer most electronic shell (4 of its own, and four from four neighbors), completely filling that shell. It is also possible to form this type of covalent bond by combining elements from group IIIB (sharing three electrons) with element from group VB (sharing five electrons). Examples of these semiconductors are GaAs or AlGaAs. They are usually called "3-5" semiconductors. We focus mostly on Si semiconductors in this class. Figure below shows this covalent bond structure for Si. Note that Si form a tetrahedron structure with an atom in the center of the tetrahedron sharing electrons with atoms on the each vertex. Figure below is a two-dimensional representation of such a structure. The left figure is for a pure Si semiconductor. A thermally-generated electron-hole pair is also shown.

If we add a small amount of an element from group VB, such as P, to the semiconductor, we create a n-type semiconductor and the impurity dopant is called a n-type dopant or donor atoms. A donor atoms also forms covalent bonds with four of its neighbors. However, as a n-type dopant has 5 valance electron, the extra electron can be in the valance band and will be promoted to the conduction band. As can be seen, there is no hole associated with this electron. In addition to electrons from the n-type dopant, there are electron-hair pair in the solid from the base semiconductor (Si in the above figure) which are generated due to temperature effects. In a n-type semiconductor, the number of free electrons from the dopant is much larger than the number of electrons or holes from electron-hole pairs. As such, electrons are called "majority" carriers and holes are called the "minority" carriers. Furthermore, a n-type semiconductor is considerably more conductive than the base semiconductor (in this respect, a n-type semiconductor is more like a "resistive" metal than a semiconductor).



Pure Semiconductor | n-type semiconductor | p-type semiconductor

Similarly, we can create a p-type semiconductor by adding an element from group IIIB, such as B, to the semiconductor. In this case, the p-type dopants or the acceptor atoms, lead to a large number of holes. For p-type semiconductors, holes are majority carriers and electrons are minority carriers.

An electric current flows if charge carriers as a whole have an average velocity. Normally, charge carriers move around the material through a random-walk process with a zero average speed and thus no current.

If an electric field is applied to the material (*i.e.,* a voltage), electrons move toward the positive voltage and holes toward the negative one resulting a net motion and a "drift" current:

$$I_{drift} = Aqn\mu_n E + Aqp\mu_p E$$

where A is the cross-sectional area of the semiconductor, q is the electronic charge, μ is the mobility of the charge carriers and E is the electric field. Density of electrons and holes are denoted by n and p, respectively.

If the concentration of charge carriers is NOT uniform throughout the semiconductor, charge carriers would move from regions of higher concentration to lower concentration in order to achieve a uniform distribution throughout the semiconductor. This process is called "diffusion," is characterized by the diffusion coefficient, D, and results in a "diffusion" current:

$$I_{diff} = AqD_n\frac{dn}{dx} - AqD_p\frac{dp}{dx}$$

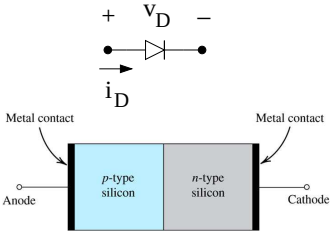
The ratio of D and μ is independent of the dopant or the base semiconductor material and is given by Einstein's Equation

$$\frac{D}{\mu} = \frac{kT}{q} \simeq \frac{T}{11,600} \approx V_T$$

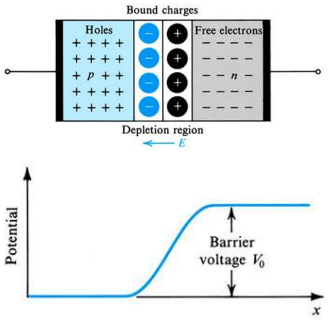
where k is the Boltzmann's constant and T is temperature in Kelvin. Parameter V_T is called the "volt-equivalent of temperature" or "thermal voltage" and appears in most semiconductor formulas. At room temperature, $V_T \approx 26$ mV.

2.3 The Junction Diode

The simplest semiconductor device is a pn-junction diode. Circuit symbol for the device is also shown with the "inward" arrow depicting the p-type material side. The convention for the direction of the diode current and voltage are also shown.



Let's ignore minority carriers for the moment. In the n side, there is a large concentration of free electrons. These electrons would like to diffuse to the p side where there are few electrons. Similarly there is a large concentration of holes in the p side and they would like to diffuse to the n side. When these electrons and holes meet in the vicinity of the junction, they combine and are neutralized. This region is depleted of mobile carriers and it is called the "depletion" region (also referred to as the "transition" or "space-charge" region). The width of depletion region is small, typically $\sim 0.5\mu$m. This diffusion of charge carriers sets up a I_{diff} from the p side to the n side of the junction.



Since the n side has lost electrons, it becomes positively charged. Similarly the p side becomes negatively charged. As a result, an electric potential and an electric field appear across the depletion region. This voltage barrier impedes the flow of electrons from the n side and flow of holes from the p side, forcing I_{diff} to go to zero. The height of this voltage barrier is called the "junction built-in voltage."

Let's consider the minority carrier now. Electrons in the p side see an attractive potential when they get close to the depletion region and are swept into the n side and combine with holes. Similarly holes on the n side are swept into the p side. This sets up a drift current I_s. As the minority carriers at this stage are due to thermal excitation, I_s is quite small ranging from 10^{-9} to 10^{-15} A. The drift current lowers the charge density on the p and n side. This lowers the potential barrier very slightly such that a diffusion current, $I_{diff} = -I_s$ will flow to ensure a zero net current: $i_D = I_{diff} - I_s = 0$.

Note that I_{diff} is a very sensitive function of barrier voltage as the number of electrons with a given energy E scales as $e^{-E/\cdots}$. Thus, a small reduction in the voltage barrier height can cause a large I_{diff} while a small increase in the voltage barrier height can cause $I_{diff} = 0$. On the other hand, the drift current I_s is independent of barrier height, but is a sensitive function of temperature: I_s doubles for every increase of ~ 7°C in temperature.

Let us attach a voltage source to this junction diode such that the positive terminal of the voltage source is attached to the n side. This configuration is called reverse bias. In this case, some of the free electrons from the n side will travel to the voltage sources making the n side more positively charged. Similarly, some of the holes from the p side would go the voltage source, making the p side more negatively charged. As a result, the depletion region becomes wider and the height of the potential barrier increases. This leads to a reduction in I_{diff} which rapidly tends to zero, leading to $i_D = -I_s$ (a very small value).

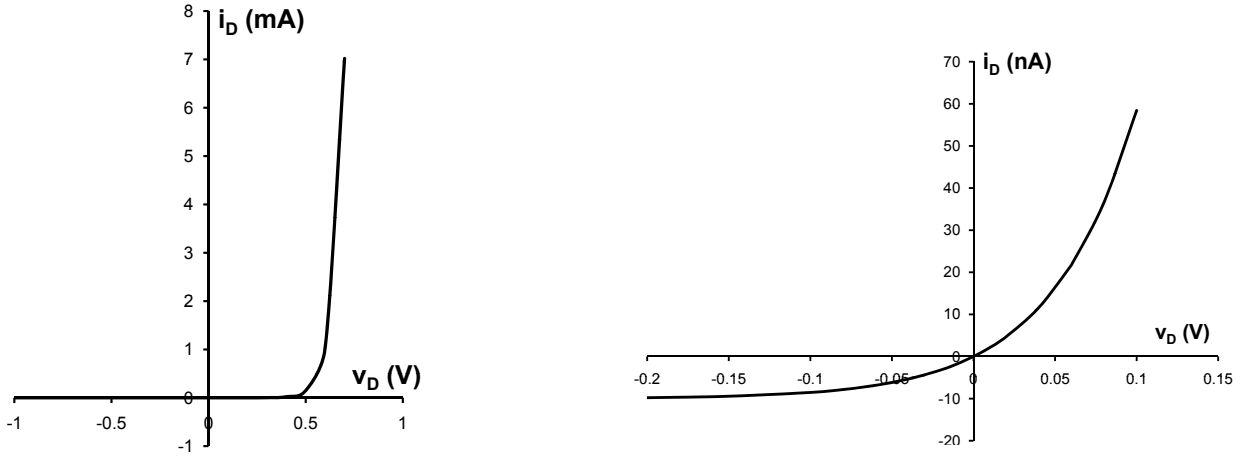
Now, let us attach the voltage source to the diode such that the positive terminal is attached to the p-type material. This configuration is called forward bias. Electrons are injected into the p side making that region less positively charged while electrons are taken from the n side making it less negatively charged. As a result, the depletion region become thinner and the height of the potential barrier decreases. In this case, I_{diff} increases rapidly, leading to $i_D \approx I_{diff}$.

iv Characteristics

One can compute I_{drift} and I_s by considering the diffusion and drift of charge carriers in the pn junction as a function of applied voltage, v_D. This is left for electronic device courses. The resultant *iv* characteristics equation of a junction diode is given by:

$$i_D = I_s \left(e^{v_D/nV_T} - 1 \right)$$

where the constant n is called the "emission coefficient" (For Si, $1 \leq n \leq 2$ in ICs). Figure below (left) shows the plot of i_D versus v_D for a typical Si diode. Note that because I_s is very small, v_D should become large enough such that large value of $\exp(v_D/V_T)$ compensate for the small value of I_s. As can be seen, the diode current sharply rises when v_D is in the range of 0.6 to 0.7 V.

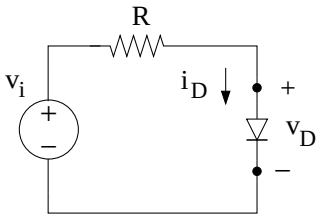


Diode Limitations: The power $P = i_D v_D$ is dissipated in the diode in the form of heat. The diode packaging provides for the conduction of this heat to the outside (*e.g.,* air). As the power dissipation increases, at some point the generated heat is more than capability of the diode package to conduct it away and diode temperature rises dramatically and diode burns out. In the forward bias region, as v_D changes slowly, this point is usually characterized by $i_{D,max}$, maximum forward current, and is specified by the manufacturer.

Since $i_D = -I_s$ and is very small in reverse bias, at first glance it appears that heat generation is not a problem as $i_D \simeq 0$ (and, thus, $P \simeq 0$). However, if we increase the reverse bias voltage, at some voltage, a large negative current can flow through the diode. This voltage is called the Zener voltage. This large reverse current is produced through two processes. First, in the reverse bias, minority carriers enter the depletion region. These minority carriers are accelerated by the voltage across the depletion region. If the reverse bias voltage is high enough, these minority carrier can accelerate to a sufficiently high energy, impact an atom, and disrupt a covalent band, thereby generating new electron-hole pairs. The new electron can accelerate, impact other atoms and generate new electron-hair pairs. In this manner, the number of minority carriers increases exponentially (an avalanches process), leading to a large reverse current. This is called the avalanche breakdown. Second, when the strength of the electric field across the junction becomes too large, electrons can be pulled out of the covalent bonds directly, generating a large number of electron-hole pairs and a large reverse current. This is known as the Zener effect or Zener breakdown.

Regular diodes are usually destroyed when operated in the Zener or reverse breakdown regions. These diode should be operated such that $v_D > -V_Z$ and/or special circuits provided to keep the reverse current to a low level. A special type of diodes, Zener diodes, are manufactured specifically to operate in the Zener region. We will discuss these diodes later.

2.4 Solving Diode Circuits



With diode iv characteristic in hand, we now attempt to solve diode circuits. Let's consider the simple circuit shown. Because the three elements are in series, current i_D flows through all elements. Writing KVL around the loop we have:

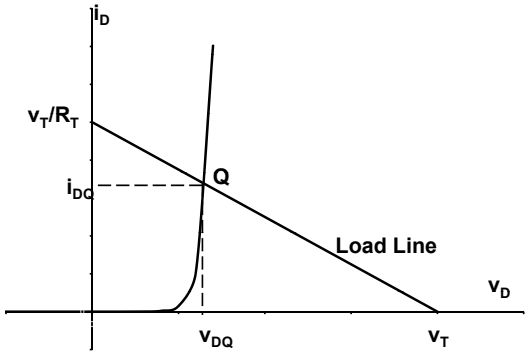
$$v_i = i_D R + v_D$$

This is an equation with two unknowns (i_D and v_D) as v_i and R_i are known. The second needed equation (to get two equations in the two unknown) is the diode iv equation:

$$i_D = I_s \left(e^{v_D / n V_T} - 1 \right)$$

The above two equations are non-linear and cannot be solved analytically. PSpice solves them numerically. There are are two other ways to solve these equations: 1) graphically (load-line analysis below) or 2) by making approximations to the diode iv equation.

2.4.1 Load Line

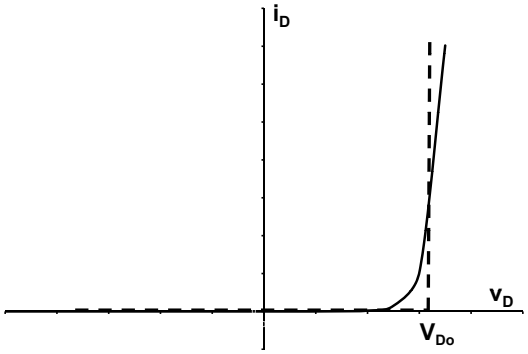


The iv characteristic of the diode is plotted in the figure. The i_D and v_D values of any point on the curve satisfies the diode equation above. Also plotted is the line representing $v_i = i_D R + v_D$. This line is called the "load line." The i_D and v_D values of any point on the load line satisfies $v_i = i_D R + v_D$.

Since the solution to the above two equations in two unknowns is a pair of i_D and v_D that satisfies both equations, such a point should be both on the iv plot of the diode and on the load line, *i.e.,* at the intersection of the two. This point is called the Q-point for the Quiescent point (or the operating point) of the diode.

The load line technique is not accurate in finding numerical values of i_D and v_D. However, it is a powerful tool to get qualitative measures of the circuit behavior *e.g.,* ensuring that the diode operating point is safety away from the maximum forward current.

2.4.2 Piecewise Linear Model



The problem in arriving at an analytical solution to the diode circuit is that the diode iv equation is nonlinear. An approach would be to try to "approximate" the diode iv equation by a linear equation (*i.e.,* the diode iv characteristics curve with a line).

As can be seen from the figure, it is NOT possible to approximate the iv curve with ONE line. However, it is possible to do so with TWO (or more) lines. This type of approximation is called a piecewise linear model, *i.e.,* pieces of the curve are replaced by lines. One such model for diodes, called the "constant voltage model," is shown in the figure with

Diode ON: $v_D = V_{D0}$ and $i_D \geq 0$

Diode OFF: $i_D = 0$ and $v_D < V_{D0}$

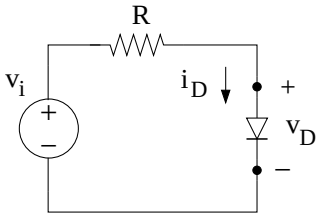
Parameter V_{D0} is called the "cut-in" voltage and depends on the base semiconductor. For Si, $V_{D0} \approx 0.6 - 0.7$ V. For GaAs, $V_{D0} \approx 1.7 - 1.9$ V. Note that each equation is valid for a range of parameters (*e.g.,* "Diode ON" equation is valid only if $i_D \geq 0$). Also, while the point with $v_D = V_{D0}$ and $i_D = 0$ is located on both Diode ON and Diode OFF lines, we have assumed that diode is ON at the point (although $i_D = 0$).

An issue that arises in solving circuits with diodes is that we do not know *a priori* the state of the diode (ON or OFF) and so we do not know which equation to use. The following "recipe" can be used to solve diode equations:

Recipe for solving diode circuits:

1. Write down all circuit equation with i_D and v_D as parameters and simplify as much as possible.
2. Assume diode is in one state (either ON or OFF). Use the diode equation for that state to solve the circuit equations and find i_D and v_D.
3. Check the inequality ("range of validity of the equation for the diode state") with the values of i_D and v_D that was found. If i_D or v_D values satisfy the inequality, the assumption was correct. Otherwise, the assumed diode state is incorrect. Go to step 2 above and assume that the diode is in the other state.

Let's use this method for the Si diode ($V_{D0} = 0.7$ V) circuit shown with $v_i = 5\ V$ and $R = 1$ kΩ.



Step 1: KCL tells that current i_D flow in all elements and by KVL:

$$v_i = i_D R + v_D \quad \rightarrow \quad 5 = 10^3 i_D + v_D$$

Step 2: Assume diode is OFF, $i_D = 0$ and $v_D < V_{D0}$. Substituting for $i_D = 0$ in the circuit equation, we get:

$$5 = 10^3 \times 0 + v_D \quad \rightarrow \quad v_D = 5 \text{ V}$$

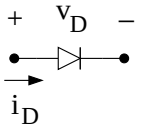
Step 3: Since $v_D = 5 > 0.7 = V_{D0}$, diode v_D does NOT satisfy range of validity and the assumed diode state is incorrect.

Step 2: Assume diode is ON, $v_D = V_{D0}$ and $i_D \geq 0$. Substituting for $v_D = V_{D0} = 0.7$ V in the circuit equation, we get:

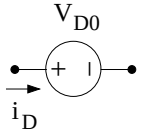
$$5 = 10^3 \times i_D + 0.7 \quad \rightarrow \quad i_D = 4.3 \text{ mA}$$

Step 3: Although we know that since diode was not OFF, it should be ON, it is a good practice to check the inequality in case we might have made a math mistake. For this case, $i_D > 0$ and satisfies the range of validity. So diode is ON and $v_D = 0.7$ V and $i_D = 4.3$ mA.

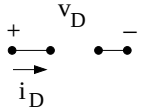
Diode circuit Model: The above method can become cumbersome if we have a complicated circuit and/or several diodes. A better approach would be to use circuit models (instead of equation) for the diode so that we can utilize circuit solution techniques such as node-voltage method.



Diode ON: $i_D \geq 0$



Diode OFF: $v_D < V_{D0}$,

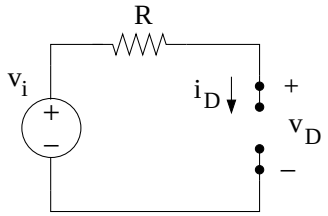


If you use the above circuit models, we need to modify our recipe for solving diode circuits accordingly:

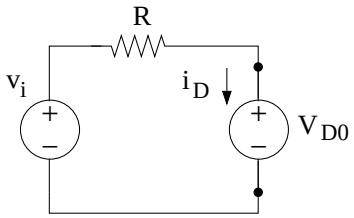
Recipe for solving diode circuits with diode circuit models:

1. Draw a circuit for each state of the diode (If more than one diode, you should draw circuits to all possible combinations of states of diodes).
2. Solve each diode circuit and find i_D and v_D.
3. Check the range of validity inequality with the values of i_D and v_D that were found. If i_D and v_D values satisfy the range of validity, the assumption was correct. Otherwise, the assumed diode state is incorrect. Go to step 2 above and start with another circuit.

As an example, let's solve the diode circuit of the previous page ($v_i = 5\ V$ and $R = 1$ kΩ) with this method:



Diode OFF: from the circuit by KVL, $v_D = v_i = 5$ V. Since $v_D > V_{D0} = 0.7$ V, our assumption is not correct.



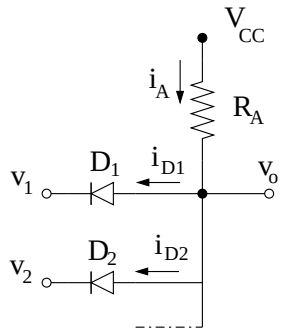
Diode ON: from the circuit by Ohm's Law, $i_D = (v_i - V_{D0})/R = 4.3$ mA. Since $i_D > 0$, our assumption is correct.

Therefore, the diode is ON with $v_D = 0.7$ V and $i_D = 4.3$ mA.

2.5 Diode Logic Gates

You have seen binary mathematics and logic gates in ECE25. We will explore some electronic logic gates in this course. Binary mathematics is built upon two states: 0, and 1. We need to relate the binary states to currents or voltages as these are parameters that we can manipulate in electronic circuits. It is advantageous (from power consumption point of view) to relate these the binary states to voltages. As such, we "choose" two voltages to represent the binary states: V_L for state 0 or Low state and V_H for state 1 or High state (for example, 0 V to represent state 0 and 5 V to represent state 1). These voltages are quite arbitrary and can be chosen to have any value. We have to be careful as it is extremely difficult, if not impossible, to design an electronic circuit to give exactly a voltage like 5 V (what if the input voltage was 4.99 V?). So, we need to define a range of voltages (instead of one value) to represent high and low states. We will discuss logic gates more thoroughly in the transistor section. Here, we consider a simpler diode logic gate.

Diode AND Gate: To study the behavior of the gate we will consider the state of the circuit with $V_{CC} = 5$ V and $R_A = 1$ kΩ for different values of v_1 and v_2 (either 0 or 5 V corresponding to low and high states). We also assume that in the output any voltage < 1 V would be considered a low state and any voltage > 4 V is considered a high state. We note that by KCL, $i_A = i_{D1} + i_{D2}$ (assuming that there is no current drawn from the circuit).



Case 1, $v_1 = v_2 = 0$:

Since the 5-V supply (V_{cc}) will tend to forward bias both D_1 and D_2, let's assume that both diodes are forward biased. Thus, $v_{D1} = v_{D2} = V_{D0} = 0.7$ V and $i_{D1} \geq 0$, $i_{D2} \geq 0$. Then,

$$v_o = v_1 + v_{D1} = v_2 + v_{D2} = 0.7 \text{ V}$$
$$i_A = \frac{V_{CC} - v_o}{R_A} = \frac{5 - 0.7}{1,000} = 4.3 \text{ mA}$$

Current i_A will be divided between two diodes by KCL, each carrying one half of i_A (because of symmetry). Thus, $i_{D1} = i_{D2} = 2.1$ mA. Since diode currents are positive, our assumption of both diode being forward biased is justified and, therefore, $v_o = 0.7$ V.

So, when v_1 and v_2 are low, D_1 and D_2 are ON and v_o is low.

Case 2, $v_1 = 0, v_2 = 5$ V:

Again, we note that the 5-V supply (V_{cc}) will tend to forward bias D_1. Assume D_1 is ON: $v_{D1} = V_{D0} = 0.7$ V and $i_{D1} \geq 0$. Then:

$$v_o = v_1 + v_{D1} = 0.7 \text{ V}$$
$$v_o = v_2 + v_{D2} \quad \rightarrow \quad v_{D2} = -4.3 \text{ V} < V_{D0}$$

and D_2 will be OFF ($i_{D2} = 0$). Then:

$$i_A = \frac{V_{CC} - v_o}{R_A} = \frac{5 - 0.7}{1,000} = 4.3 \text{ mA}$$
$$i_{D1} = i_A - i_{D2} = 4.3 - 0 = 4.3 \text{ mA}$$

Since $i_{D1} > 0$, our assumption of D_1 forward biased is justified and, therefore, $v_o = 0.7$ V.

So, when v_1 is low and v_2 is high, D_1 is ON and D_2 is OFF and v_o is low.

Case 3, $v_1 = 5$ V, $v_2 = 0$ V:

Because of the symmetry in the circuit, this is exactly the same as case 2 with roles of D_1 and D_2 reversed.

So, when v_1 is high and v_2 is low, D_1 is OFF and D_2 is ON and v_o is low.

Case 4, $v_1 = v_2 = 5$ V:

Examining the circuit, it appears that the 5-V supply (V_{cc}) will NOT be able to forward bias D_1 and D_2. Assume D_1 and D_2 are OFF: $i_{D1} = i_{D2} = 0$, $v_{D1} < V_{D0}$ and $v_{D2} < V_{D0}$. Then:

$$i_A = i_{D1} + i_{D2} = 0$$

$$v_o = V_{CC} - i_{D1}R_A = 5 - 0 = 5 \text{ V}$$

$$v_{D1} = v_o - v_1 = 5 - 5 = 0 < V_{D0} \qquad \text{and} \qquad v_{D2} = v_o - v_2 = 5 - 5 = 0 < V_{D0}$$

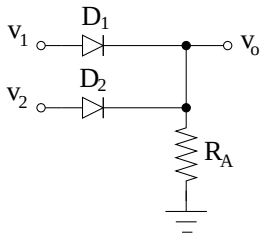
Thus, our assumption of both diodes being OFF are justified.

So, when v_1 and v_2 are high, D_1 and D_2 are OFF and v_o is high.

Overall, the output of this circuit is high only if both inputs are high (Case 4) and the output is low in all other cases (Cases 1 to 3). Thus, this is an AND gate. This analysis can be easily extended to cases with three or more diode inputs.

This circuit is not a good gate as for input we used low states of 0 V and the output low state was 0.7 V. We need to make sure that the input low state voltage is similar to the output low state voltage so that we can put these gates back to back. (You can easily show that if we had assumed low states of 0.7 V for input, the output low state would have been 1.4 V.) This gate is not usually used by itself but as part of diode-transistor logic gates that we will discuss in the BJT section.

Exercise: Show that this is an OR gate.



2.6 Parametric solution of diode circuits

In the diode circuits above, we need to know the value of all of the elements in order to find the state of the diode and currents and voltages in the circuit. This is cumbersome as for example, the input voltage v_i to the circuit changes in time, we need to solve the diode circuit for ALL values of v_i.

It is very useful if we can derive the circuit solution parametrically, *i.e.,* with values of various circuit elements, in particular, the input voltage as parameters. This approach would allows us to solve the circuit ONCE. The problem is that diode can be either of its two states which, in principle, depend on the values of circuit parameters (v_i and R in the example above).

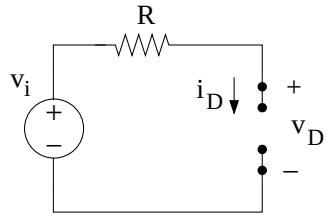
The approach to do this is to assume that the diode is one specific state and find the range of circuit parameters (*e.g.,* range of v_i) that would result in the diode being in that state. In this manner, we will have multiple solutions for v_o, each valid for range of v_i.

Recipe for solving diode circuits parametrically:

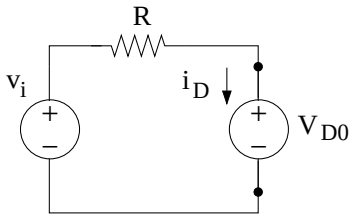
1. Draw circuits covering all possible diode states (2^n states, where n is the number of diodes)
2. Solve each circuit and find currents and voltages.
3. For each circuit, use the range of validity inequality of the diode states to find the range of circuit parameters which leads to that state.

For example, consider the diode circuit discussed before with v_i as a parameter. Following our recipe we get:

Diode OFF: from the circuit by KVL, $v_D = v_i$.
For diode OFF, we need $v_D < V_{D0}$ or $v_i < V_{D0}$. Therefore, when $v_i < V_{D0}$, diode will be OFF and $v_D = v_i$.



Diode ON: from the circuit by Ohm's Law, $i_D = (v_i - V_{D0})/R$.
For diode ON, we need $i_D \geq 0 \rightarrow (v_i - V_{D0})/R \geq 0$ or as R is positive, $v_i - V_{D0} \geq 0$.



Therefore, the parametric solution of the circuit can be summarized as:

$$\text{When} \quad v_i \geq V_{D0} \quad \rightarrow \quad \text{Diode is ON} \quad \rightarrow \quad v_D = V_{D0} \quad \text{and} \quad i_D = \frac{v_i - V_{D0}}{R}$$

$$\text{When} \quad v_i < V_{D0} \quad \rightarrow \quad \text{Diode is OFF} \quad \rightarrow \quad v_D = v_i \quad \text{and} \quad i_D = 0$$

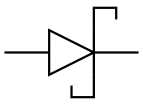
Note that if we had solved the circuit parametrically first, we could get the answer for the case $v_i = 5$ V and $R = 1$ kΩ immediately: $v_i = 5$ V $> V_{D0} = 0.7$ V, therefore, diode is ON, $v_D = V_{D0} = 0.7$ V and $i_D = (5 - 0.7)/10^3 = 4.3$ mA.

We will use the above method to explore some diode circuits later.

2.7 Other Types of Diodes

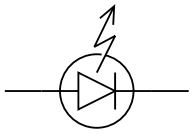
Three other types of diodes are in wide use. They include:

Schottky Barrier Diode: Schottky barrier diodes are formed by putting a metallic surface in contact with n-type semiconductors. This type of diode has a much larger I_s and, therefore, will go into forward-bias at $V_{D0} \approx 0.3$ V. Because majority carriers do not have to diffuse toward the contact point, Schottky diodes have a much faster switching speed and are used in digital circuits like transistor-transistor logic (TTL). The circuit symbol for a Schottky diode is similar to a junction diode but with the cathode vertical line modified to resembled an S.



Schottky Diode

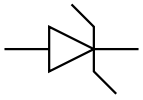
Light-Emitting Diode (LED): This type of diode emits light when it is forward biased. In order to have a visible light output, the band gap of the semiconductor should be larger than that of Si. Thus, these diodes are typically made of types III-V semiconductors (*e.g., GaAs*). As such, they have a much larger V_{D0} between 1.7 to 1.9 V.



LED

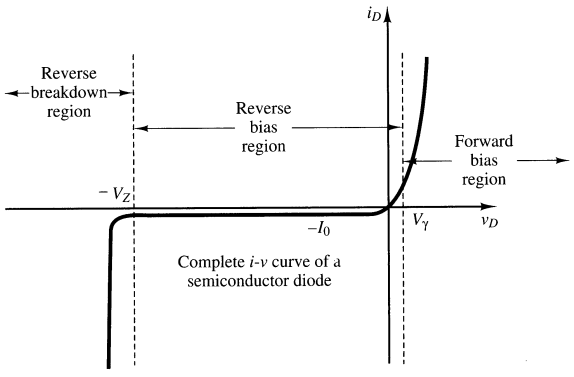
Both Schottky diodes and LEDs are similar to regular junction diodes (with the exception of V_{D0} value).

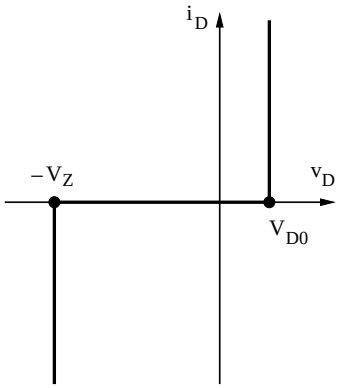
Zener Diodes: Zener diodes are specially manufactured to operate in the Zener region. In these diode, heavily doped regions are manufactured near the metal contacts to the semiconductor. The high density of charge carriers allows a substantial reverse breakdown current to be sustained. These diodes are useful in applications where a constant value of voltage is necessary, for example, in voltage regulators.



Zener Diode

The iv characteristics of a Zener diode and the corresponding constant-voltage model are shown below:



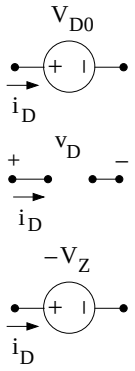


The constant-voltage model equations are:

ON: $v_D = V_{D0}$ and $i_D \geq 0$

OFF: $-V_z < v_D < V_{D0}$ and $i_D = 0$

Zener Region: $v_D = -V_Z$ and $i_D \leq 0$

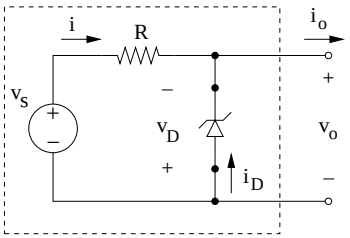


Diode circuit solution techniques discussed above can also be applied to Zener diodes. The only change is that a Zener diode has three states (instead of two for a regular diode).

2.7.1 A simple Power Supply

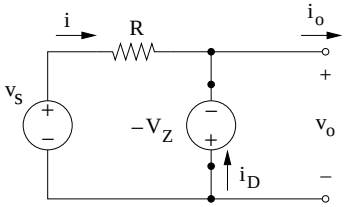
Electronic circuit are designed to be powered by a constant voltage. In most cases, the voltage of the power source may change (*e.g.* battery voltages changes as battery ages. As such, all electronic devices have a power supply circuit to ensure constant voltage to circuits.

This circuit is a simple power supply. Its output voltage v_o, is constant for a range of i_o's (even if v_s changes). Below we compute the iv characteristics of this circuit for $v_o \geq 0$.



Case 1: Diode is in the Zener region. The equivalent circuit is shown and we need to have $i_D \leq 0$. KVL in the right loop gives:

KVL: $v_o = V_Z = const$



So as long as the diode is in the Zener region, the output voltage will be constant regardless of the value of i_o.

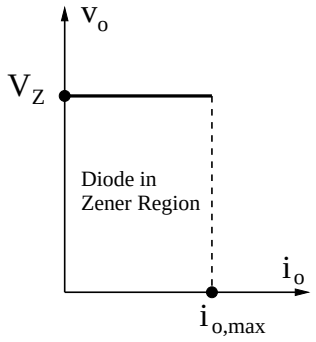
To find the range of parameters for which the diode remains in the Zener region ($i_D \leq 0$), we note:

KCL: $i_D = i_o - i$

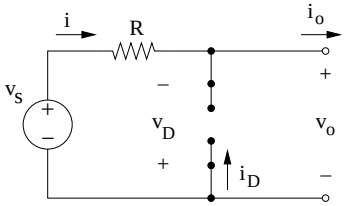
KVL : $v_s = Ri + V_Z$

$$i_D = i_0 - \frac{v_s - V_Z}{R} \leq 0 \qquad \rightarrow \qquad i_o \leq \frac{v_s - V_Z}{R}$$

The iv response of the circuit for this range of currents is shown. The circuit resembles an independent voltage source with a strength of V_Z as long as $i_o < (v_s - V_Z)/R = i_{o,max}$). In practice, because V_Z changes slightly when the diode current changes, the output voltage of circuit ($v_o = V_Z$) changes slightly. Much better power supply circuits can be build by addition of a transistor or OpAmps to the circuit



Case 2: Diode is in the reverse bias region. Let consider what happens if we exceed the $i_{o,max}$. The equivalent circuit is shown and we need to have $-V_Z < v_D < V_{D0}$. Because $i_D = 0$, KCL gives $i = i_o$. Then, KVL in the outer loop gives:



$$\text{KVL:} \qquad v_s = Ri_o + v_o \qquad \rightarrow \qquad v_o = v_s - Ri_o$$

i.e., the output voltage drops as more current is drawn from the circuit.

To find the range of parameters for which the diode remains in the reverse bias region ($-V_Z < v_D < V_{D0}$), we note: $v_o = -v_D$. Recall also that we are interested only in $v_o \geq 0$ (problem definition):

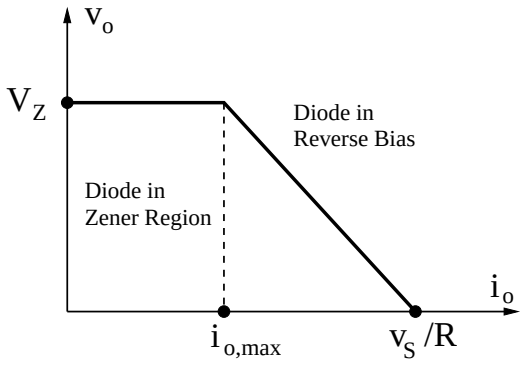
$$-V_Z < -v_o < V_{D0}$$

$$-V_Z > v_o > -V_{D0} \qquad \text{and} \qquad v_o \geq 0 \qquad \rightarrow \qquad 0 \leq v_o < V_Z$$

$$0 \leq v_s - Ri_o < -V_Z \qquad \rightarrow \qquad \frac{v_s - V_Z}{R} < i_o \leq \frac{v_s}{R}$$

We do not need to consider the forward bias case as $v_o \geq 0$ means $v_D \leq 0$.

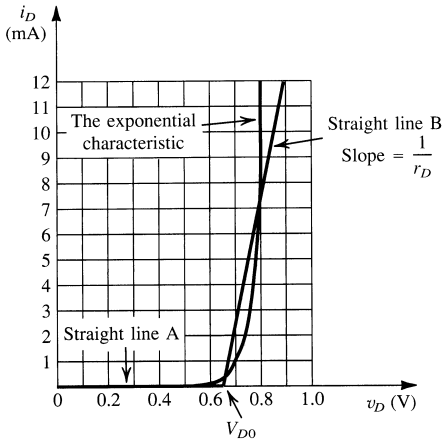
The complete iv characteristics of the circuit is shown in the figure.



2.8 Other Diode Models

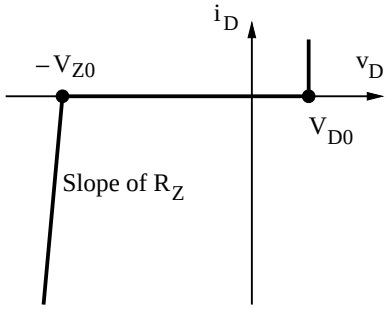
In this section, we introduced the piecewise linear model for the diode. Many choices for these model "lines" are possible. The constant voltage model utilized in this section approximated the ON state of the diode with a vertical line (*i.e.*, $v_D = V_{D0}$).

Figure shows another model in which the ON state is approximated with a "sloped" line. In this case, two parameters, V_{D0} and R_D, are necessary with $v_D = V_{D0} + i_D R_D$. The corresponding circuit model for the ON state is a voltage source V_{D0} in series with a resistor R_D. This model is not often used as A) a large set of V_{D0} and R_D can be chosen and the best choice actually depends on the operating point of the diode (which is not known a priori), and B) the increase in the amount of work for analyzing the circuit does not usually justify the improvement in the accuracy.

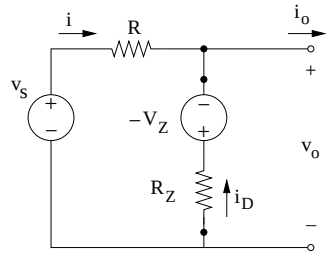


This type of model is useful only if resistances in the circuit are of the same order as R_D (typically 10's Ω).

Similarly for a Zener diode, the Zener region can be modeled with a combination of a voltage source ($-V_{Z0}$) and a resistor (R_Z). We analyze the simple the Zener-diode power supply circuit of page 2-16 to show how such a model is utilized. We consider the Zener state only.



Diode is in the Zener region: The equivalent circuit is shown and we need to have $i_D \leq 0$. We assume that i_o is known and compute v_o (to get the response of the circuit) and i_D (to check for the diode state). KCL and KVL in the left loop give:



$$\text{KCL:} \quad i_D + i = i_o$$

$$\text{KVL:} \quad v_s = Ri + V_{Z0} - R_Z i_D$$

We first find i_D by eliminating i between above equations:

$$i_D = -\frac{v_s - V_{Z0} - Ri_o}{R + R_Z}$$

$$i_D \leq 0 \qquad \rightarrow \qquad i_o \leq \frac{v_s - V_{Z0}}{R} = i_{o,max}$$

which is exactly the same as before (except V_Z is replaced with V_{Z0}).

The response of the circuit (v_o in terms of i_o) can be found by a KVL in the right loop:

$$v_o = V_{Z0} - R_Z i_D = V_{Z0} + R_Z \times \frac{v_s - V_{Z0} - R i_o}{R + R_Z} = \frac{R V_{Z0} + R_Z v_s}{R + R_Z} - \frac{R R_Z}{R + R_Z} i_o$$

$$v_o = \hat{V}_Z - (R \parallel R_Z)\, i_o$$

with $\hat{V}_Z = (R V_{Z0} + R_Z v_s)/(R + R_Z)$. This expression for v_o indicates that the output voltage is slowly decreasing with increasing i_o. The circuit resembles a combination of an independent voltage source $\hat{V}_Z$ and a resistor $R \parallel R_Z$.

The expression above can be simplified greatly by assuming $R_Z \ll R$ to get:

$$v_o \approx V_{Z0} - R_Z i_o$$

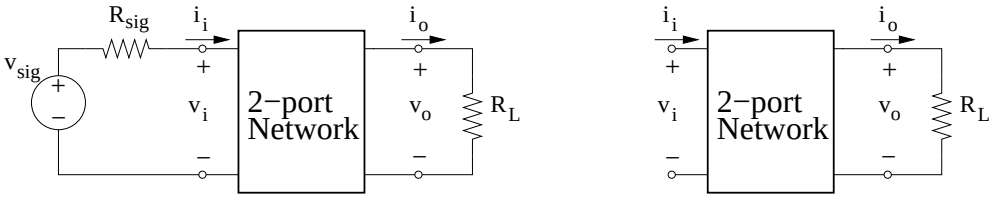
As can be seen, the more complicated model for the Zener diode and longer analysis has illuminated some slight changes in the circuit behavior.

2.9 Wave-form Shaping Circuits

In this section, we will examine several popular diode circuits. These circuit are generally called wave-form shaping circuits as a diode is utilized to "modify" the input voltage wave-form. Circuits like these are two-port networks. As discussed in Sec. 1, we only need to solve the circuit below (left) for two-port networks. We are interested to compute v_o as a function of v_i (the transfer function of the circuit). Knowing the transfer function, we can compute v_o for any value of v_i without analyzing the circuit again.

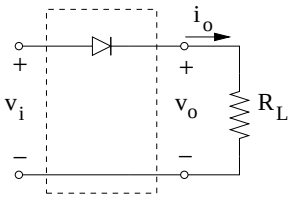
As the transfer function is computed as a function of v_i, we usually ignore v_{sig} and R_{sig} in our analysis (circuit below, right). We will see in the transistor amplifier section that we can find v_i in terms of v_{sig} and R_{sig} by utilizing the concept of the input resistance for a two-port network.

Lastly, in some circuits analysis is greatly simplified if $R_L \to \infty$ (or $i_o = 0$). This case is called the "open-loop" transfer function. As such, we may solve this case first in order to understand the circuit behavior before adding R_L to the circuit.



2.9.1 Rectifier Circuits

This is the simplest diode wave-form shaping circuit. Since $i_o = i_D$



$$\text{KVL} \qquad v_i = v_D + v_o$$

$$v_o = R_L i_D$$

Diode OFF: $i_D = 0$, $v_D < V_{D0}$

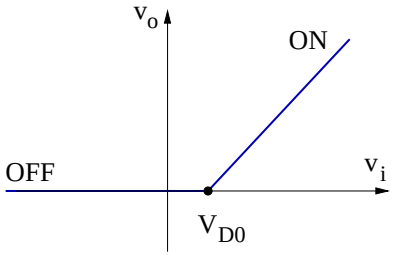
From above, $v_o = R_L i_D = 0$. Furthermore, Diode is in the OFF state when $v_D = v_i < V_{D0}$.

Diode ON: $v_D = V_{D0}$, $i_D \geq 0$,

$$v_i = v_D + v_o \qquad \rightarrow \qquad v_o = v_i - v_D = v_i - V_{D0}$$

$$i_D = \frac{v_i - V_{D0}}{R_L} \geq 0 \qquad \rightarrow \qquad v_i \geq V_{D0}$$

Thus, when $v_i \geq V_{D0}$, diode will be ON and $v_o = v_i - V_{D0}$.

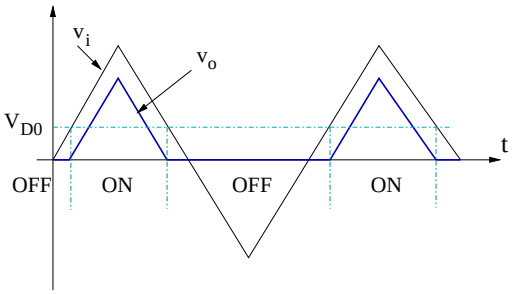


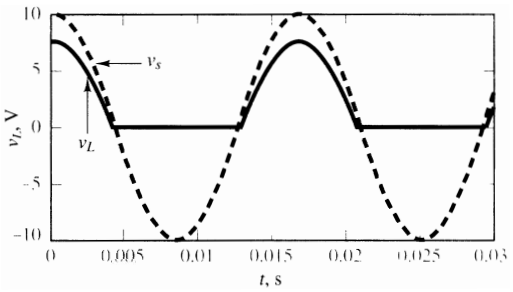
Transfer function of the circuit is:

$$v_i < V_{D0} \quad \rightarrow \quad \text{Diode is OFF:} \quad \text{and} \quad v_o = 0$$

$$v_i \geq V_{D0} \quad \rightarrow \quad \text{Diode is ON:} \quad \text{and} \quad v_o = v_i - V_{D0}$$

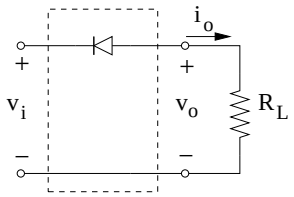
The figure below (left) shows how v_o can be found for a time dependent v_i (triangular wave in this case). We first find "time intervals" in which diode is OFF ($v_i < V_{D0}$) and time intervals in which diode is ON ($v_i \geq V_{D0}$): separated by vertical dashed lines in the figure. We can then construct the output wave-form by plotting $v_o = 0$ when diode is OFF and $v_o = v_i - V_{D0}$ when diode is ON as is shown below.



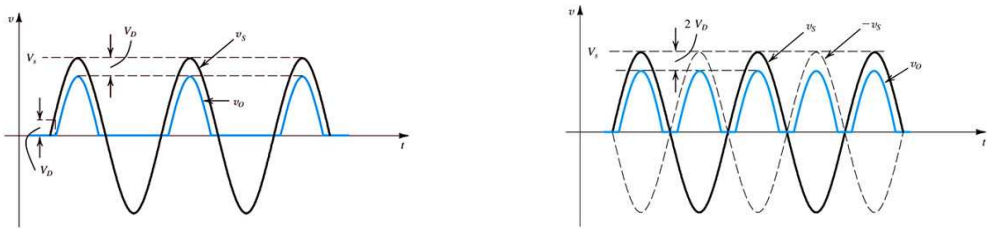


Exercise: Figure above right is the scope trace for a sinusoidal input waveform (dashed line) and the rectified output (solid line). Explain why the output trace does NOT EXACTLY follow $v_o = v_i - V_{D0}$ at every point.

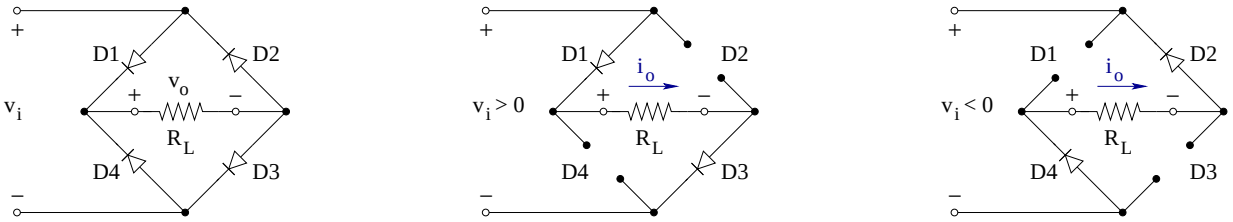
Exercise: What happens if the diode terminals are reversed (Answer: circuit work as a rectifier but the output voltage will be negative)



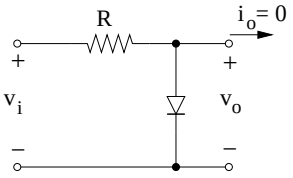
The above circuit is a simple method to convert AC input voltages to a "DC" output voltage and is used in AC to DC converter part of power supplies. Such circuits are called "rectifier" circuits. Because the output of the circuit above is only one half of the input waveform (figure below left), this circuit is called a "half-wave" rectifier circuit.



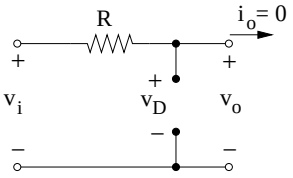
A better circuit is a "full-wave" rectifier in which both portions of the AC input waveform is turned into a DC output so that we do not "throw" away half of the input (figure above right). An example of such a full-wave rectifier is the bridge rectifier shown below (left) with four diodes. We can see that in the portion of the input period in which $v_i > 2V_{D0}$, diodes D1 and D3 are ON and a positive voltage appear across R_L (center circuit). Diodes D2 and D4 are OFF. In the portion of the waveform in which $v_i < -2V_{D0}$, Diode D2 and D4 are ON and diodes D1 and D3 are OFF and again a positive voltage appears on R_L (left circuit). Thus, for both positive and negative v_i, v_o would be positive.



2.9.2 Clipper Circuit

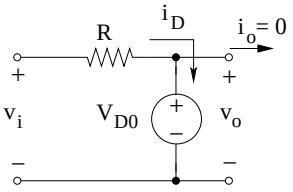


We will consider the open-loop transfer function first. Using the diode circuit model, we will arrive at the circuits below. Note that $v_o = v_D$.



Diode OFF: $i_D = 0$, $v_D < V_{D0}$:

For $i_D = i_o = 0$, no current flows in R and $v_o = v_i$. Furthermore, Diode is OFF when $v_D = v_o = v_i < V_{D0}$.

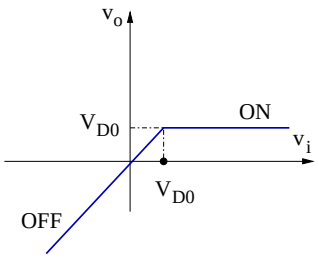


Diode ON: $v_D = V_{D0}$, $i_D \geq 0$:

In this case $v_o = v_D = V_{D0}$. Diode is ON when

$$i_D = \frac{v_i - V_{D0}}{R} \geq 0 \quad \rightarrow \quad v_i \geq V_{D0}$$

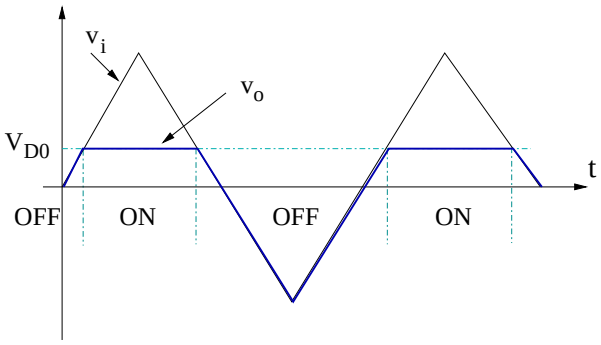
Transfer function of this circuit is shown with



$v_i < V_{D0} \quad \rightarrow \quad$ Diode is OFF: and $v_o = v_i$

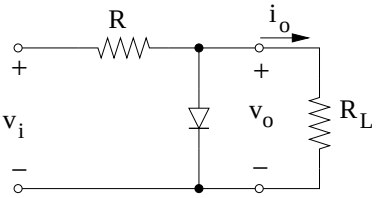
$v_i \geq V_{D0} \quad \rightarrow \quad$ Diode is ON: and $v_o = V_{D0}$

The figure shows v_o for a time dependent v_i (triangular wave in this case). Similar to the rectifier case, we first identify the time slices when the diode is ON and those when the diode is OFF and then plot v_o accordingly. As can be seen, $v_o = v_i$ when $v_i < V_{D0}$. But when $v_i \geq V_{D0}$, the output voltage has remained fixed at V_{D0}, as if values larger than V_{D0} were "clipped" from the wave-form . As such, this is called a clipper or a limiter circuit.



It is of interest to compare the clipper circuit with the half-wave rectifier. As can be seen circuits are the same with the exception of v_o being taken across the resistor for the half-wave rectifier (*i.e.*, $v_o = v_R$) while v_o is taken across the diode for the clipper circuit (*i.e.*, $v_o = v_D$). Since $v_i = v_D + v_R$, this circuit (combination of a diode and a resistor) divides the input signal into two parts, the "rectified" part which appears across the resistor and the clipped part which appears across the diode.

Exercise: A) Show that the transfer function does not change if a load R_L is attached to the circuit as long as $R_L \gg R$. B) What happens if R_L is not large?

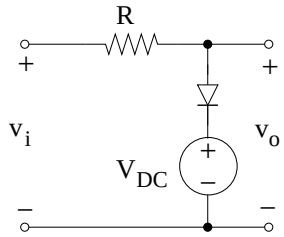


It is of interest to build circuits which can "clip" the input signal at values different than V_{D0}. These circuits can be realized by inspecting the clipper circuit above. We see that the signal is clipped when the diode is ON. At these time intervals, the diode appears as an independent voltage source in the circuit with $v_o = v_D = V_{D0}$. As such, Addition of a voltage source in series with the diode will change the clipping as is shown below. Note $v_o = v_D + V_{DC}$.

Diode ON: $v_D = V_{D0}$, $i_D \geq 0$,

$v_o = v_D + V_{DC} = V_{D0} + V_{DC}$. Diode is ON when

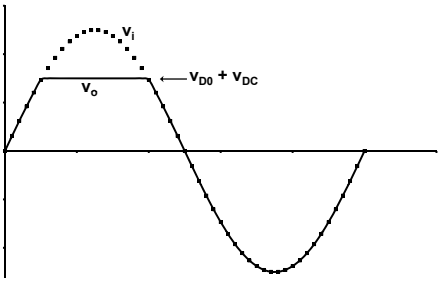
$$i_D = \frac{v_i - v_o}{R} \geq 0 \quad \rightarrow \quad v_i \geq v_o = V_{D0} + V_{DC}$$

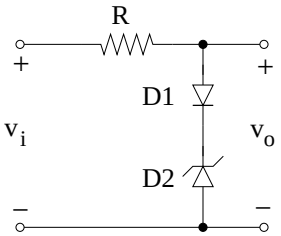


Diode OFF: $i_D = 0$, $v_D < V_{D0}$:

For $i_D = i_o = 0$, no current flows in R and $v_o = v_i$. Furthermore, Diode is OFF when $v_D = v_o - V_{DC} = v_i - V_{DC} < V_{D0}$ or $v_i < V_{D0} + V_{DC}$

Therefore, this circuit clips input voltages that are larger than $v_{DC} + V_{D0}$ as is shown below (left). Note that we can choose v_{DC} to be negative and make the clipping voltage to be negative. (However, always the "top" part of the wave form is clipped.)

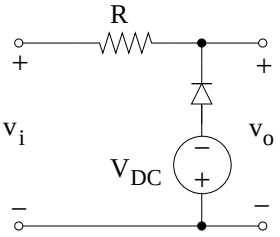




As power supplies are bulky and expensive, a Zener diode can be used instead of v_{DC} as is shown above (right). The draw back of a clipper circuit with Zener diodes is that V_Z is always positive. Therefore, we can only clip voltages above the positive value of $V_{D0} + V_Z$. The circuit containing the voltage source v_{DC} would allow clipping voltages above a "negative" value by choosing a negative v_{DC}.

Exercise: Show that the clipper circuit above with the Zener diode clips voltages larger than $V_Z + V_{D0}$.

We can clip voltages that are smaller than a certain value by switching the diode terminals as is shown in the circuit below. (Note that v_{DC} terminals are also switched). Here $v_o = -v_D - V_{DC}$



Diode ON: $v_D = V_{D0}$, $i_D \geq 0$,

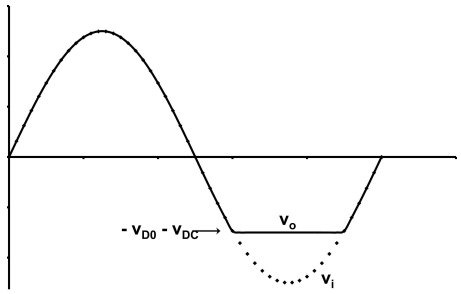
$v_o = -v_D - V_{DC} = -(V_{D0} + V_{DC})$. Diode is ON when

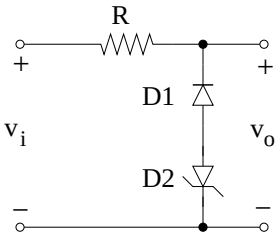
$$i_D = \frac{v_o - v_i}{R} \geq 0 \quad \rightarrow \quad v_i \leq v_o = -(V_{D0} + V_{DC})$$

Diode OFF: $i_D = 0$, $v_D < V_{D0}$:

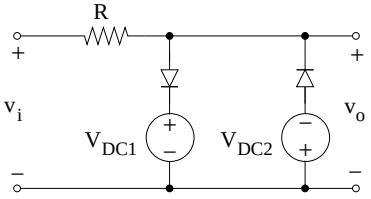
For $i_D = i_o = 0$, no current flows in R and $v_o = v_i$. Furthermore, Diode is OFF when $v_D = -v_o - V_{DC} = -v_i - V_{DC} < V_{D0}$ or $v_i > -(V_{D0} + V_{DC})$.

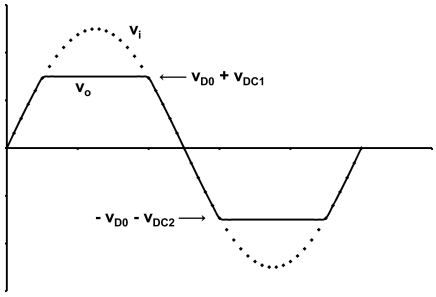
As can be seen, when $v_i > -(V_{D0} + V_{DC})$, $v_o = v_i$ and signals goes through. While when $v_i \leq -(V_{D0} + V_{DC})$, $v_o = -(V_{D0} + V_{DC})$. Therefore, this circuit clips input voltages that are smaller than $-(V_{DC} + V_{D0})$ as is shown below (left). Note that we can choose v_{DC} to be negative and make the clipping voltage to be positive. However, always the "bottom" part of the wave form is clipped. One can replace v_{DC} with a Zener voltage is shown below (right circuit).

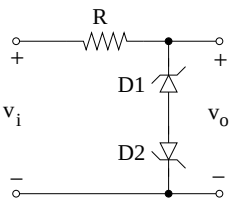




The above two circuits above can be combined to clip both voltages larger than $v_{DC1} + V_{D0}$ and voltages smaller than $-v_{DC2} - V_{D0}$.

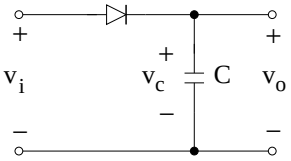






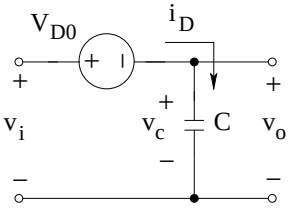
Exercise: Find the limiting voltages of the circuit above with Zener diodes.

2.9.3 Peak Detector



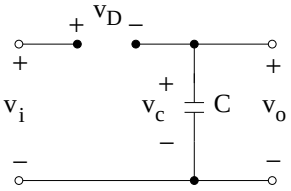
Another simple but useful diode circuit includes a diode and a capacitor. We will consider the open-loop transfer function first. Because the voltage across the capacitor, v_c, cannot change suddenly, state of the diode in this circuit depends not only on the instantaneous value of v_i but also on the "history" of the circuit (*e.g.* dv_i/dt, v_c at certain times).

Using diode circuit models, we will arrive at circuits below. Note that $v_o = v_c$.



Diode ON: $v_D = V_{D0}$, $i_D \geq 0$:

In this case $v_o = v_c = v_i - V_{D0}$.
Since $i_D = i_C = Cdv_c/dt = Cd(v_i - V_{D0})/dt = dv_i/dt$, condition of $i_D \geq 0$ requires v_i to be increasing.



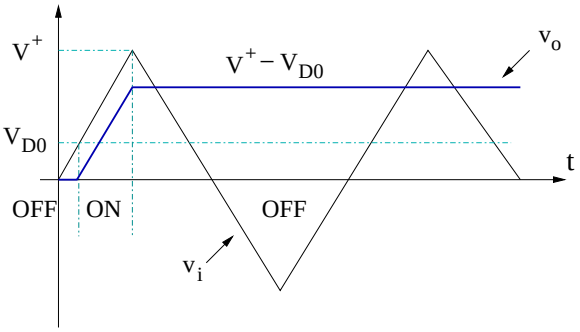
Diode OFF: $i_D = 0$, $v_D < V_{D0}$:

In this case $v_o = v_c = v_{c0}$ where v_{c0} is the capacitor voltage when the diode turned OFF. Diode remains OFF as long as $v_D = v_i - v_c \leq V_{D0}$ or $v_i < v_c + V_{D0}$.

$$\frac{dv_i}{dt} \geq 0 \quad \& \quad v_i = v_c + V_{D0} \qquad \text{Diode ON:} \qquad v_o = v_c = v_i - V_{D0}$$

$$v_i < v_c + V_{D0} \qquad \text{Diode OFF:} \qquad v_o = v_{c0}$$

As can be seen, the state of diode depends not only on v_i but also on dv_i/dt and v_c.

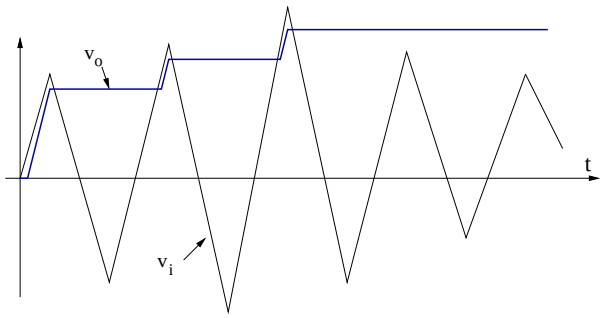


Assume the input signal is a triangular wave with a peak (positive) value of V^+. The source v_i is attached to the circuit at $t = 0$. At this time, $v_c = v_{c0} = 0$. While initially v_i is increasing, diode remains OFF because $v_c = v_{c0} = 0$ and $v_i < v_c + V_{D0} = V_{D0}$. When v_i reaches V_{D0}, the diode turns ON and the capacitor starts to charge with $v_o = v_c = v_i - V_{D0}$.

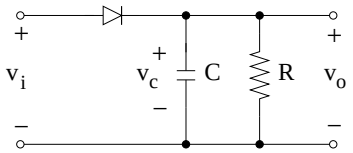
When v_i reaches its peak value, $v_c = v_i - V_{D0} = V^+ - V_{D0}$. After this point, the diode turns OFF because v_i is decreasing. Capacitor voltage remains at $v_c = V^+ - V_{D0}$. v_i eventually reaches its lowest value and start to increase again. Although v_i is increasing, the diode remains OFF because $v_i < v_c + V_{D0} = V^+$. Only when v_i reaches its peak value again, the diode turns ON. But it turns OFF immediately as v_i starts to decrease.

In summary, the capacitor charges up to a value of $V^+ - V_{D0}$ in the first cycle and its voltage remains constant from then on. Note that V^+ is the peak value of the input signal and the shape of the input signal is not important. This circuit is called a peak detector as the output voltage is the the peak of the input voltage (minus V_{D0}).

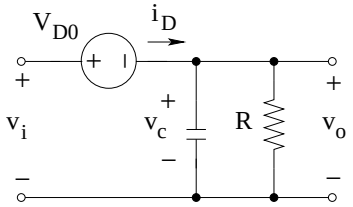
If an input signal with a varying amplitude is applied to an ideal peak detector, the capacitor charges up until it reaches the peak value for the complete waveform as is shown in the figure.



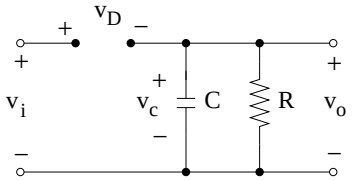
A practical peak-detector circuit includes a resistor in parallel with the capacitor. This resistor is either the load for the ideal peak detector or is placed in the circuit on purpose as is seen later.



Diode ON: $v_D = V_{D0}$, $i_D \geq 0$:
In this case $v_o = v_c = v_i - V_{D0}$.
Since $i_D = i_C = Cdv_c/dt = Cd(v_i - V_{D0})/dt = dv_i/dt$, condition of $i_D \geq 0$ requires v_i to be increasing.
As can be seen these conditions are similar to those for an ideal peak detector.



Diode OFF: $i_D = 0$, $v_D < V_{D0}$: In this case we have an RC circuit with the capacitor discharging in the resistor with a time constant $\tau = RC$ according to $v_o(t) = v_c(t) = v_{c0}\exp[-(t - t_0)/\tau]$. v_{c0} denotes the capacitor voltage when diode turned OFF (at t_0). Diode remains OFF as long as $v_D = v_i - v_c \leq V_{D0}$ or $v_i \leq v_c + V_{D0}$.

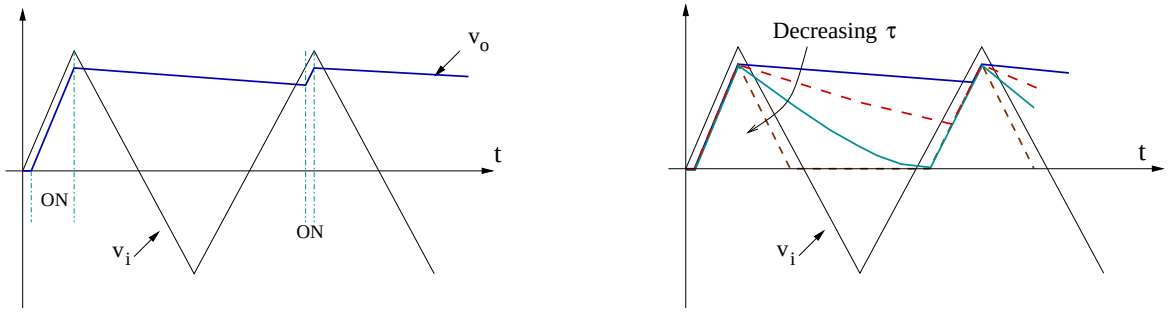


The diode OFF case is different from that of an ideal peak detector, as the voltage across the capacitor changes. The transfer function of the circuit is:

$$\frac{dv_i}{dt} \geq 0 \quad \& \quad v_i = v_c + V_{D0} \qquad \text{Diode ON:} \qquad v_o = v_c = v_i - V_{D0}$$

$$v_i < v_c + V_{D0} \qquad \text{Diode OFF:} \qquad v_o(t) = v_c(t) = v_{c0}\exp[-(t - t_0)/\tau]$$

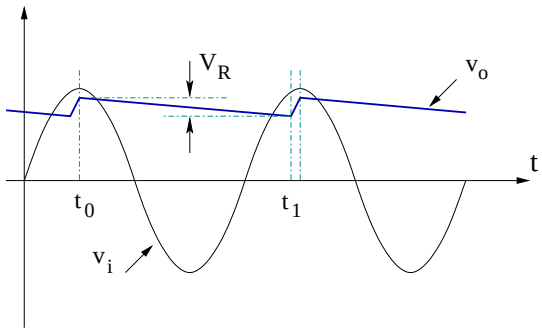
Behavior of this circuit during the first half cycle is identical to that of the ideal peak detector (see figure below, left). When v_i reaches its peak value, $v_c = V^+ - V_{D0}$. After this point, the diode turns OFF because v_i is decreasing. As opposed to the ideal peak detector, the capacitor voltage starts to decrease. v_i eventually reaches its lowest value and start to increase again. Diode remains OFF until v_i reaches $v_i = v_c + V_{D0}$. Because capacitor has discharged, v_c is lower than V^+ and the diode turns ON before v_i reaches its peak value. Diode remain ON until v_i reaches V^+ and and the capacitor is charged back to $v_c = V^+ - V_{D0}$. Then, v_i starts to decrease, diode turns OFF, and the cycle repeats itself.



The shape of output waveform depends on how much the capacitor discharges in each cycle (see figure above right). For $\tau = RC = \infty$, capacitor does NOT discharge and we recover the ideal peak detector response ($R = \infty$). Denoting the period of the input by T, if $\tau \gg T$, the capacitor would discharge very little in each cycle and v_o would be very close to that of an ideal peak detector.

When τ becomes comparable to T, the capacitor discharges considerably in each period and v_o departs from that of an ideal peak detector. It should be noted that the capacitor voltage cannot become negative. As such, v_o is always positive as is shown above (right figure). In the limit of $\tau \ll T$, capacitor discharges so rapidly that the circuit effectively becomes a rectifier circuit!

Peak detectors have many applications. One is in a AC to DC power supply. While a rectifier circuit converts AC input into DC, the output waveform is still "half" sinusoidal and not useful for powering electronic circuits. Addition of a capacitor (and effectively turning the rectifier into a peak detector) results in a relatively constant DC voltage as is shown.



Obviously capacitor value should be chosen such that $\tau = RC \gg T$. For this application, R is the load (*i.e.* equal to v_o divided by the current drawn by the electronic circuit).

The changes in the output voltage, V_R, is called the "ripple." To find V_R, we denote the time that capacitor starts to discharge as t_0 with $v_c(t_0) = V^+ - V_{D0}$. The capacitor discharges until diode turns ON at t_1. Since $\tau \gg T$, the length of the diode OFF interval (when capacitor is discharging) is very close to the period of the input wave, $t_1 \approx t_0 + T$.

$$v_c(t) = v_{c0}\, e^{-(t - t_0)/\tau}$$

$$V_R = v_c(t = t_0) - v_c(t = t_1) = v_{c0} - v_{c0}\, e^{-(t_1 - t_0)/\tau}$$

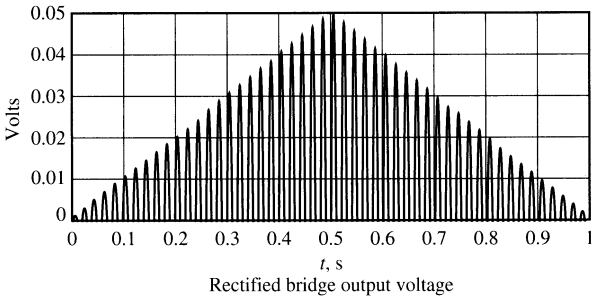
$$V_R = v_{c0}[1 - e^{-(t_1 - t_0)/\tau}] = (V^+ - V_{D0})v_{c0}[1 - e^{-T/\tau}]$$

$$1 - e^{-(t_1 - t_0)/\tau} \approx 1 - \left(1 - \frac{T}{\tau}\right) = \frac{T}{\tau}$$

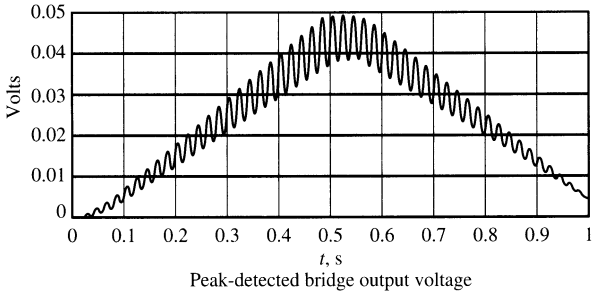
$$\frac{V_R}{V^+ - V_{D0}} = \frac{T}{\tau}$$

Thus, the "relative" magnitude of the ripple only depends on T/τ.

Another application of a peak detector is in Amplitude-Modulation (AM) receivers. The AM station transmits a carrier wave (corresponding to the radio station frequency). The amplitude of the carrier wave is modulated according the broadcast sound signal. An example of such a signal is shown below left for a triangular sound wave. We denote the period of carrier wave as $T_{carrier}$ and the period of the sound wave as T_{so}. In the receiver, this modulated voltage is applied to a peak-detector circuit. The circuit RC is chosen such that $T_{so} \gg \tau = RC \gg T_{carrier}$. The output of the peak detector is an approximation of the initial sound wave as is shown below (which is the envelope of the peak amplitudes of the input signal).



Rectified bridge output voltage

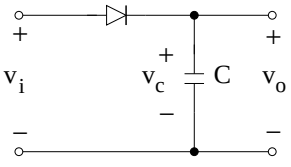


Peak-detected bridge output voltage

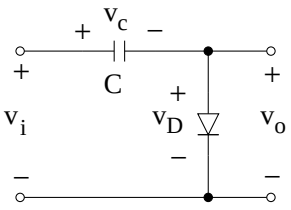
Exercise: What happens if diode terminals in a peak detector are reversed?
(Answer: $v_o = -(V^- - V_{D0})$ where $-V^-$ is the smallest value of the input voltage.)

2.9.4 Clamp Circuit

We saw that in the ideal peak detector (shown on the right), the diode is ON in the first cycle and the capacitor charges to a voltage of $v_c = V^+ - V_{D0}$. Capacitor voltage remains constant after-wards (and diode remains OFF). In this circuit $v_o = v_c$.



A clamp circuit (shown on the right) is identical to the ideal peak detector, except that the output voltage is taken across the diode, $v_o = v_D$.

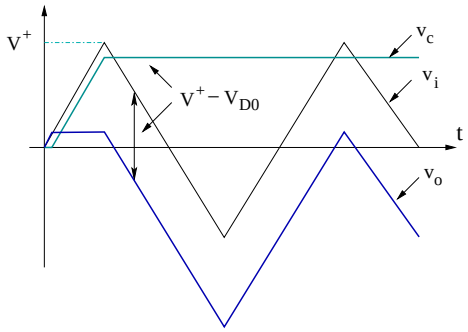


Since the two circuits are identical, we do not need to solve the clamp circuit. We use the analysis of the ideal peak detector and note that ignoring the first cycle, $v_c = V^+ - V_{D0}$. Thus,

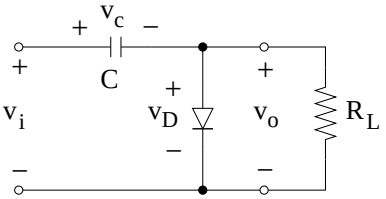
$$v_i = v_c + v_D$$

$$v_o = v_D = v_i - v_c \qquad \rightarrow \qquad v_o = v_i - (V^+ - V_{D0})$$

Thus, the output voltage is equal to the input voltage "shifted downward" by a DC value of $-(V^+ - V_{D0})$ as is shown in the figure. Although the shape of the input signal is not important, its amplitude (or its peak value, V^+) should be constant. Otherwise the output voltage would be "distorted" as it would have different value of shifts at different times.

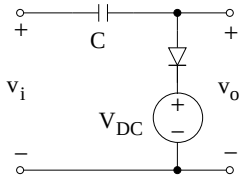


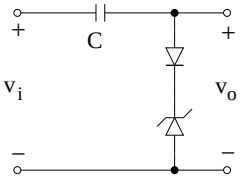
Let's consider the impact of a load, R_L. During the first cycle when the diode is ON, the capacitor charges to a voltage of $v_c = V^+ - V_{D0}$ (similar to open-loop case). However, when the diode turns OFF, the capacitor discharges in R_L and its voltage drops. Similar to a peak detector with a load, the diode turns ON in the following cycle and charge the capacitor back to $v_c = V^+ - V_{D0}$.



In a clamp circuit $v_o = v_i - v_c$ and we need v_c to remain fairly constant in order for v_o to be a "shifted" v_i (and not distorted). Therefore, capacitor should discharge very little in each cycle. This constraint requires that $\tau = R_L C \ll T$. With this constraint, v_o of a clamp circuit with a R_L would be similar to that of the open-loop case.

Since the capacitor is charged when the diode is ON, different values of downward shift (corresponding to different capacitor charged-up voltages) can be produced by adding a DC voltage source in series with the diode (circuit below, left):





$v_o = v_i - (V^+ - V_{D0} - v_{DC})$ $\qquad$ $v_o = v_i - (V^+ - V_{D0} - v_Z)$

Since capacitor charges up when the diode is ON (and charges until v_i reaches V^+):

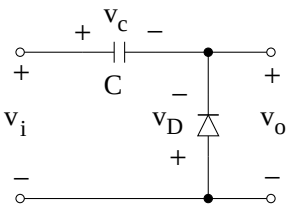
$$v_i = +v_c + V_{D0} + v_{DC} \qquad \rightarrow \qquad v_c = V^+ - V_{D0} - v_{DC}$$

From then on, capacitor voltage remains constant, diode remains OFF, and

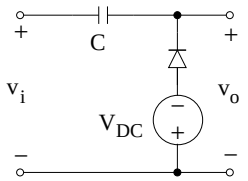
$$v_o = v_i - v_c = v_i - (V^+ - V_{D0} - v_{DC})$$

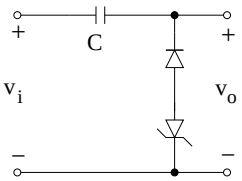
If needed, v_{DC} can be replaced with a Zener diodes (similar to clipper circuits) as is shown in the circuit above (right).

If we switch terminals of the diode, the capacitor charges to a voltage of $v_c = -(V^- - V_{D0})$. Therefore, $v_o = v_i - v_c = v_i + (V^- - V_{D0})$, and the circuit adds a positive voltage to the input ("upward" shift in scope traces).



Similarly, we can produce different values of upward shift by the addition of a DC voltage source in series with the diode or using Zener diodes.



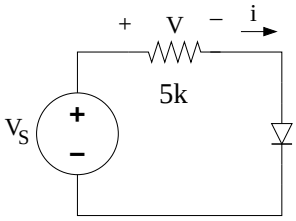


$v_o = v_i + (V^- - V_{D0} - v_{DC})$ $\qquad$ $v_o = v_i + (V^- - V_{D0} - v_Z)$

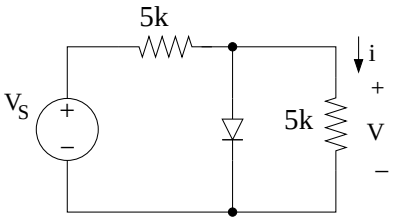
2.10 Exercise Problems

In circuit design, use commercial resistor values (1, 1.1, 1.2, 1.3, 1.5, 1.6, 1.8, 2, 2.2, 2.4, 2.7, 3., 3.3, 3.6, 3.9, 4.3, 4.7, 5.1, 5.6, 6.2, 6.8, 7.5, 8.2, 9.1) and commercial capacitor values (1, 1.5, 1.8, 2. or 2.2, 3.3, 4.7, and 6.8) values. You can also use Zener diodes with any Zener voltage.

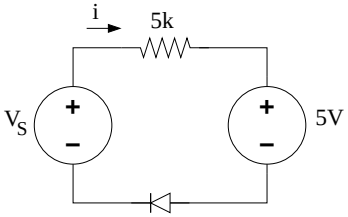
Problems 1 to 9. In circuits below with Si diodes ($V_{D0} = 0.7$ V) and $V_Z = 5$ V for Zener diodes, A) Find v and/or i for $v_s = 10$ V, B) Find v and/or i for v_s ranging from -20 to $+20$ V.



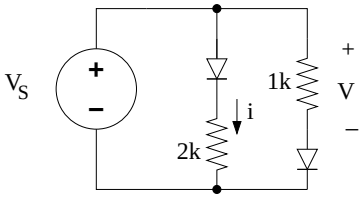
Problem 1



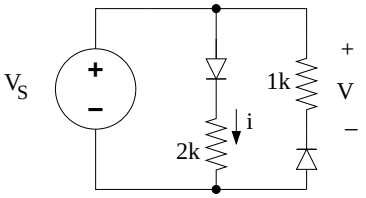
Problem 2



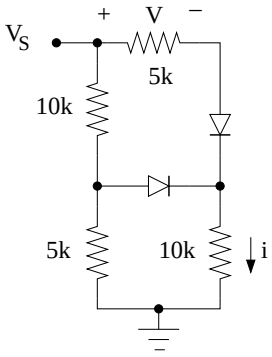
Problem 3



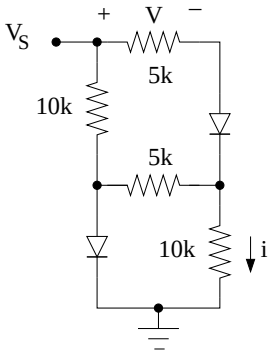
Problem 4



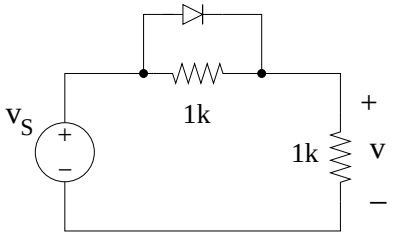
Problem 5



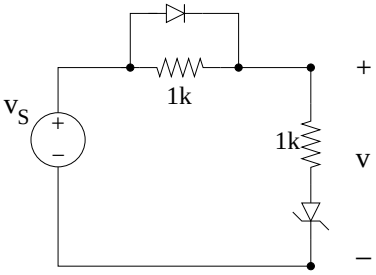
Problem 6



Problem 7

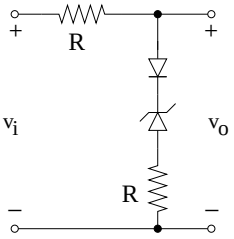


Problem 8

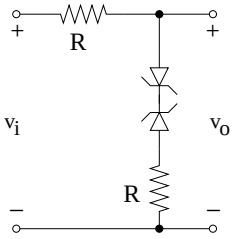


Problem 9

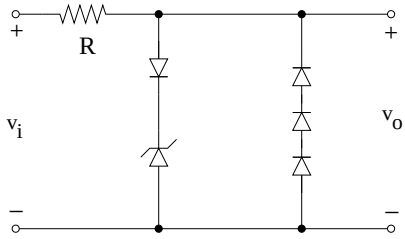
Problems 10 to 12. Find transfer functions of circuits below (Si diodes with V_{D0}=0.7 V and $V_Z = 5$ V for Zener diodes).



Problem 10



Problem 11



Problem 12

Problem 13. Design a clipper circuit that clips voltages above 5 V using a) DC power supplies only, b) Zener diodes only.

Problem 14. Design a clipper circuit that clips voltages above 5 V and below −3 V using a) DC power supplies only, b) Zener diodes only.

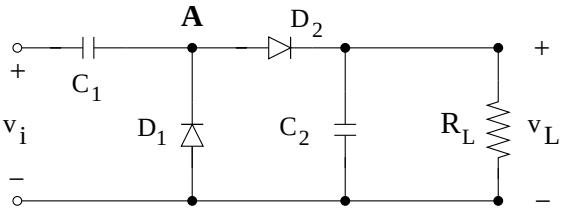
Problem 15. Design a clipper circuit that clips voltages above 5 V and below +3 V using a) DC power supplies only, b) Zener diodes only.

Problem 16. Consider a sinusoidal source with $v_i = 15\sin(\omega t)$ V. Design a clamp circuit that adds a DC offset of +5 to the input voltage using a) DC power supplies only, b) Zener diodes only.

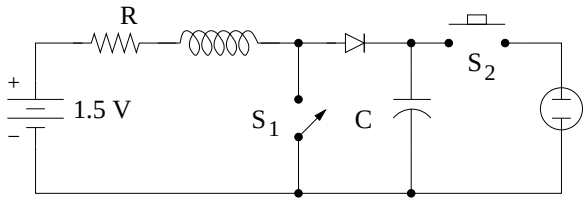
Problem 17. Consider a sinusoidal source with $v_i = 15\sin(\omega t)$ V. Design a clamp circuit that adds a DC offset of −5 to the input voltage using a) DC power supplies only, b) Zener diodes only.

Problem 18. Circuit below is a "voltage doubler." Show that if $v_i = V_p\sin(\omega t)$, $v_o = 2V_p$ (Assume that capacitor C is large such that it discharge very little per cycle and $V_p \gg V_{D0}$.)

Problem 19. Circuit below is a simplified version of an electronic flash for cameras. Switch S2 is controlled by the shutter and is closed to operate the flash bulb. Normally switch S2 is open. The circuit to the left of switch S2 charges the capacitor to about 100 V using a 1.5 V battery. Switch $S1$ is an electronic switch that is opened and closed at about 10 kHz. As a result, the capacitor is charged to about 100 V using a 1.5 V battery. Explain how the charge-up circuit works.



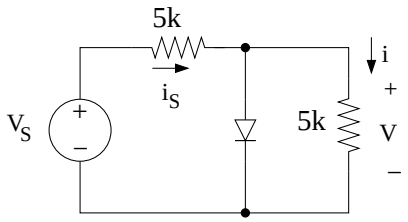
Problem 18



Problem 19

2.11 Solution to Selected Exercise Problems

Problem 2. In circuit below with Si diodes ($V_{D0} = 0.7$ V) and $V_Z = 5$ V for Zener diodes, A) Find v and/or i for $v_s = 10$ V, B) Find v and/or i for v_s ranging from -20 to $+20$ V.



Circuit equations:

KCL: $i_s = i_D + i$

KVL: $v_s = 5 \times 10^3 i_s + v_D$

KVL: $v = v_D = 5 \times 10^3 i$

Part A: $v_s = 10$ V.

Assume diode is ON: $v_D = V_{D0} = 0.7$ V, $i_D \geq 0$. Substituting in the above equations we get:

$$v_s = 5 \times 10^3 i_s + v_D \quad \rightarrow \quad 10 = 5 \times 10^3 i_s + 0.7 \quad \rightarrow \quad i_s = 1.86 \text{ mA}$$

$$v = v_D = 0.7 \text{ V}$$

$$v = v_D = 5 \times 10^3 i \quad \rightarrow \quad 0.7 = 5 \times 10^3 i \quad \rightarrow \quad i = 0.14 \text{ mA}$$

$$i_s = i_D + i \quad \rightarrow \quad 1.86 \times 10^{-3} = i_D + 0.14 \times 10^{-3} \quad \rightarrow \quad i_D = 1.72 \text{ mA}$$

Since $i_D = 1.72$ mA > 0, our assumption of diode being ON is correct and $i = 0.14$ mA and $v = 0.7$ V.

Part B: Parametric Solution:

For diode being ON: $v_D = V_{D0} = 0.7$ V, $i_D \geq 0$. Substituting in the circuit equations we get:

$$v_s = 5 \times 10^3 i_s + v_D \quad \rightarrow \quad v_s = 5 \times 10^3 i_s + 0.7 \quad \rightarrow \quad i_s = 2 \times 10^{-4}(v_s - 0.7) \text{ A}$$

$$v = v_D = 0.7 \text{ V}$$

$$v = v_D = 5 \times 10^3 i \quad \rightarrow \quad 0.7 = 5 \times 10^3 i \quad \rightarrow \quad i = 0.14 \text{ mA}$$

$$i_s = i_D + i \quad \rightarrow \quad i_D = i_s - 0.14 \times 10^{-3} = 2 \times 10^{-4}(v_s - 0.7) - 1.4 \times 10^{-4}$$

$$i_D \geq 0 \quad \rightarrow \quad 2 \times 10^{-4}(v_s - 0.7) - 1.4 \times 10^{-4} \geq 0 \quad \rightarrow \quad v_s \geq 1.4 \text{ V}$$

For diode being OFF: $i_D = 0$ and $v_D < V_{D0} = 0.7$ V. From circuit equations, we get:

$$i_s = i_D + i \quad \rightarrow \quad i_s = i$$

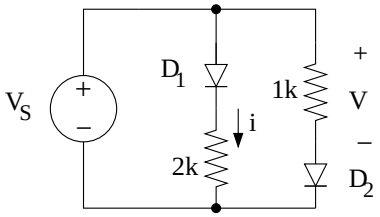
$$v_s = 5\times 10^3 i_s + v_D = 5\times 10^3 i_s + 5\times 10^3 i = 1\times 10^4 i \quad \rightarrow \quad i = 10^{-4} v_s$$

$$v = v_D = 5\times 10^3 i \quad \rightarrow \quad v = v_D = 0.5 v_s$$

$$v_D < V_{D0} = 0.7 \quad \rightarrow \quad 0.5 v_s < 0.7 \quad \rightarrow \quad v_s < 1.4 \text{ V}$$

Therefore, for $v_s < 1.4$ V, diode is OFF $v = 0.5 v_s$ and $i = 10^{-4} v_s$.
For $v_s \geq 1.4$ V, diode is ON, $v = 0.7$ V, and $i = 0.14$ mA.

Problem 4. In circuit below with Si diodes ($V_{D0} = 0.7$ V) and $V_Z = 5$ V for Zener diodes, A) Find v and/or i for $v_s = 10$ V, B) Find v and/or i for v_s ranging from -20 to $+20$ V.



Circuit equations:

KVL: $v_s = v_{D1} + 2\times 10^3 i_{D1}$

KVL: $v_s = 10^3 i_{D2} + v_{D2}$

$v = 10^3 i_{D2}$ and $i = i_{D1}$

Part A: $v_s = 10$ V.

Assume both diodes are ON: $v_{D1} = v_{D2} = V_{D0} = 0.7$ V, $i_{D1} \geq 0$, and $i_{D2} \geq 0$. Substituting in the above equations we get:

KVL: $v_s = v_{D1} + 2\times 10^3 i_{D1} \rightarrow 10 = 0.7 + 2\times 10^3 i_{D1} \rightarrow i_{D1} = 4.65\times 10^{-3} = 4.65$ mA

KVL: $v_s = 10^3 i_{D2} + v_{D2} \quad \rightarrow \quad 10 = 0.7 + 10^3 i_{D2} \quad \rightarrow \quad i_{D2} = 9.3\times 10^{-3} = 9.3$ mA

$v = 10^3 i_{D2} \quad \rightarrow \quad v = 9.3$ V

Since both i_{D1} and i_{D1} are positive, our assumption of both diodes being ON is correct and $v = 9.3$ V and $i = i_{D1} = 4.65$ mA.

Part B: Parametric Solution: Here, we have to consider four cases.

Case 1: D1 and D2 are both ON: $v_{D1} = v_{D2} = V_{D0} = 0.7$ V, $i_{D1} \geq 0$, and $i_{D2} \geq 0$.

KVL: $v_s = v_{D1} + 2\times 10^3 i_{D1} \rightarrow v_s = 0.7 + 2\times 10^3 i_{D1} \rightarrow i_{D1} = 5\times 10^{-4}(v_s - 0.7)$

KVL: $v_s = 10^3 i_{D2} + v_{D2} \quad \rightarrow \quad v_s = 0.7 + 10^3 i_{D2} \quad \rightarrow \quad i_{D2} = 10^{-3}(v_s - 0.7)$

$v = 10^3 i_{D2} \quad \rightarrow \quad v = v_s - 0.7$

$i_{D1} \geq 0 \quad \rightarrow \quad 5\times 10^{-4}(v_s - 0.7) \geq 0 \quad \rightarrow \quad v_s \geq 0.7$ V

$i_{D2} \geq 0 \quad \rightarrow \quad 10^{-3}(v_s - 0.7) \geq 0 \quad \rightarrow \quad v_s \geq 0.7$ V

So, for $v_s > 0.7$ V, both diodes will be ON with $v = v_s - 0.7$ V and $i = i_{D1} = 5 \times 10^{-4}(v_s - 0.7) = 0.5(v_s - 0.7)$ mA.

Case 2: D1 and D2 are both OFF: $i_{D1} = i_{D2} = 0$, $v_{D1} < V_{D0} = 0.7$ V, and $v_{D2} < V_{D0} = 0.7$ V.

KVL: $v_s = v_{D1} + 2 \times 10^3 i_{D1} \quad \rightarrow \quad v_{D1} = v_s$

KVL: $v_s = 10^3 i_{D2} + v_{D2} \quad \rightarrow \quad v_{D2} = v_s$

$v = 10^3 i_{D2} \quad \rightarrow \quad v = 0$

$v_{D1} < V_{D0} = 0.7 \quad \rightarrow \quad v_s < 0.7$ V

$v_{D2} < V_{D0} = 0.7 \quad \rightarrow \quad v_s < 0.7$ V

So, for $v_s < 0.7$ V, both diodes will be OFF with $v = 0$ and $i = i_{D1} = 0$

Note that since for $v_s > 0.7$ V, both diodes will be ON and for $v_s < 0.7$ V, both diodes will be OFF, one would expect that it would not be possible for one diode to be ON and one to be OFF. We will demonstrate this below.

Case 3: D1 is ON: $v_{D1} = V_{D0} = 0.7$ V, and $i_{D1} \geq 0$ while D2 is OFF: $i_{D2} = 0$ and $v_{D2} < V_{D0} = 0.7$ V.

KVL: $v_s = v_{D1} + 2 \times 10^3 i_{D1} \rightarrow v_s = 0.7 + 2 \times 10^3 i_{D1} \rightarrow i_{D1} = 5 \times 10^{-4}(v_s - 0.7)$

KVL: $v_s = 10^3 i_{D2} + v_{D2} \quad \rightarrow \quad v_{D2} = v_s$

$v = 10^3 i_{D2} \quad \rightarrow \quad v = v_s - 0.7$

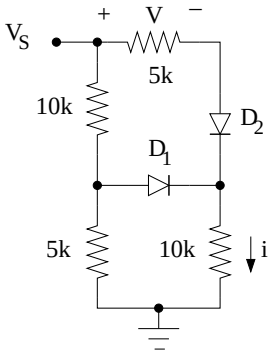
$i_{D1} \geq 0 \quad \rightarrow \quad 5 \times 10^{-4}(v_s - 0.7) \geq 0 \quad \rightarrow \quad v_s \geq 0.7$ V

$v_{D2} < V_{D0} = 0.7 \quad \rightarrow \quad v_s < 0.7$ V

We see that for D1 to be ON ($i_{D1} \geq 0$), we need $v_s \geq 0.7$ V and for D2 to be OFF ($v_{D2} < V_{D0}$) we need $v_s < 0.7$ V. These cases are mutually exclusive so we cannot have simultaneously D1 ON and D2 OFF.

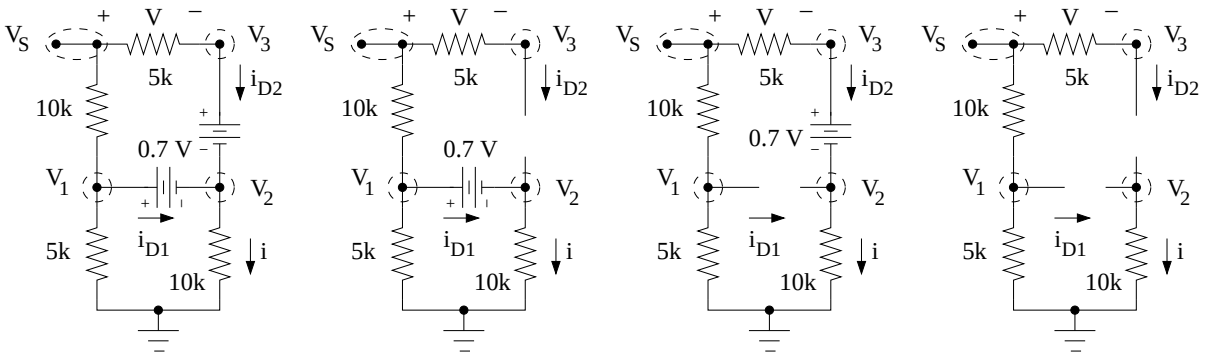
Similarly, we can find D1 is OFF and D2 ON case is not possible.

Problem 6. In circuit below with Si diodes ($V_{D0} = 0.7$ V) and $V_Z = 5$ V for Zener diodes, A) Find v and/or i for $v_s = 10$ V, B) Find v and/or i for v_s ranging from -20 to $+20$ V.



Part A: $v_s = 10$ V.

With the exception of simple circuits, it is usually more useful to redraw the circuit based on the state of the diodes as this can simplify the circuit considerably. Note that when a diode is ON, $v_D = V_{D0}$ for $i_D > 0$ and the diode resembles an ideal voltage source with the strength of V_{D0}. When the diode is OFF, $i_D = 0$ and the diode resembles an open circuit. This can be seen in circuits below:



D1 ON, D2 ON | D1 ON, D2 OFF | D1 OFF, D2 ON | D1 OFF, D2 OFF

Case 1: Assume D1 is ON and D2 is ON. The above circuit can be solved by node voltage method. This circuit has four nodes, v_1, v_2, v_3, and $v_s = 10$ V. All nodes are supernodes as they are attached to a voltage source. So we have only we KCL containing nodes v_1, v_2, and v_3:

$$\text{Supernode:} \quad v_1 - v_2 = 0.7$$

$$\text{Supernode:} \quad v_3 - v_2 = 0.7$$

$$\text{KCL at } v_1, v_2, v_3: \quad \frac{v_1 - v_s}{10 \times 10^3} + \frac{v_3 - v_s}{5 \times 10^3} + \frac{v_1 - 0}{5 \times 10^3} + \frac{v_2 - 0}{10 \times 10^3} = 0$$

$$v_1 - v_s + 2(v_3 - v_s) + 2v_1 + v_2 = 0$$

$$3v_1 + v_2 + 2v_3 = 3v_s = 30 \text{ V}$$

We substitute for v_1 and v_3 from the first two equations in the last equation to get:

$$3(v_2 + 0.7) + v_2 + 2(v_2 + 0.7) = 30 \quad \rightarrow \quad v_2 = 4.42 \text{ V} \quad \text{and} \quad v_1 = v_3 = 5.12 \text{ V}$$

To check the validity of our assumption of D1 and D2 ON, we need to compute i_{D1} and i_{D2}. i_{D2} is the same as the current in the 5 k resistor on the top of the circuit and i_{D2} can be found by KCL at node v_1:

$$i_{D1} = \frac{v_s - v_1}{10 \times 10^3} + \frac{0 - v_1}{5 \times 10^3} = \frac{10 - 5.12}{10 \times 10^3} + \frac{-5.12}{5 \times 10^3} = -0.54 \text{ mA} < 0$$
$$i_{D2} = \frac{v_s - v_3}{5 \times 10^3} = \frac{10 - 5.12}{5 \times 10^3} = 0.98 \text{ mA} > 0$$

Since $i_{D1} < 0$, our assumption is incorrect and we should consider other cases.

Case 2: Assume D1 is ON and D2 is OFF. The above circuit can be solved by node voltage method. This circuit has three nodes, v_1, v_2, and $v_s = 10$ V ($v_3 = v_s = 10$ V as $i_{D2} = 0$). All nodes are supernodes as they are attached to a voltage source. So:

$$\text{Supernode:} \quad v_1 - v_2 = 0.7$$
$$\text{KCL at } v_1, v_2: \quad \frac{v_1 - v_s}{10 \times 10^3} + \frac{v_1 - 0}{5 \times 10^3} + \frac{v_2 - 0}{10 \times 10^3} = 0$$
$$v_1 - v_s + 2v_1 + v_2 = 0 \quad \rightarrow \quad 3v_1 + v_2 = v_s = 10 \text{ V}$$

We substitute for v_1 from the first equation in the second equation to get:

$$3(v_2 + 0.7) + v_2 = 10 \quad \rightarrow \quad v_2 = 1.98 \text{ V} \quad \text{and} \quad v_1 = 2.68 \text{ V}$$

To check the validity of our assumption of D1 ON and D2 OFF, we need to compute i_{D1} (KCL at node v_1) and v_{D2}.

$$i_{D1} = \frac{v_s - v_1}{10 \times 10^3} + \frac{0 - v_1}{5 \times 10^3} = \frac{10 - 1.98}{10 \times 10^3} - \frac{1.98}{5 \times 10^3} = 4.06 \text{ mA} > 0$$
$$v_{D2} = v_3 - v_2 = 10 - 1.98 = 8.02 > 0.7 \text{ V}$$

Since $v_{D2} > 0.7$, our assumption is incorrect and we should consider other cases.

Case 3: Assume D1 is OFF and D2 is ON. The above circuit can be solved by node voltage method. This circuit has four nodes, v_1, v_2, v_3, and $v_s = 10$ V. All nodes except v_1 are supernodes as they are attached to a voltage source. So:

$$\text{Supernode:} \quad v_3 - v_2 = 0.7$$
$$\text{KCL at } v_2, v_3: \quad \frac{v_3 - v_s}{5 \times 10^3} + \frac{v_2 - 0}{10 \times 10^3} = 0 \quad \rightarrow \quad 2v_3 - 20 + v_2 = 0$$
$$\text{KCL at } v_1: \quad \frac{v_1 - v_s}{10 \times 10^3} + \frac{v_1 - 0}{5 \times 10^3} = 0 \quad \rightarrow \quad v_1 - 10 + 2v_1 = 0 \quad \rightarrow \quad v_1 = 3.33 \text{ V}$$

The first two equations can be solved to find v_2 and v_3:

$$2(v_2 + 0.7) + v_2 = 20 \quad \rightarrow \quad v_2 = 6.2 \text{ V} \quad \rightarrow \quad v_3 = 6.9 \text{ V}$$

To check the validity of our assumption of D1 OFF and D2 ON, we need to compute v_{D1} and i_{D2}.

$$v_{D1} = v_1 - v_2 = 3.33 - 6.2 = -2.87 < 0.7 \text{ V}$$
$$i_{D2} = \frac{v_s - v_3}{5 \times 10^3} = \frac{10 - 6.9}{5 \times 10^3} = 0.62 \text{ mA} > 0$$

Since $v_{D1} < 0.7$ and $i_{D2} > 0$, our assumption is correct. So D1 is OFF, D2 is ON and $i = i_{D2} = 0.62$mA and $v = v_s - v_3 = 10 - 6.9 = 3.1$ V.

This case could have been solved more simply by noting that when D1 is OFF, the two branches of the circuit become independent (we have two separate circuits) and v_1 and v_2 can be directly calculated:

$$v_1 = \frac{5 \times 10^3}{10 \times 10^3 + 5 \times 10^3} \times 10 = 3.33 \text{ V}$$
$$i = i_{D2} = \frac{v_s - 0.7}{10 \times 10^3 + 5 \times 10^3} = 0.62 \text{ mA}$$

and proceed to compute $v_{D1} < 0.7$ to show that our assumption was valid.

Case 4: Assume D1 is OFF and D2 is OFF.

While we proved that D1 is OFF and D2 is ON, let's proceed to solve this case. Again, we see that two branches of the circuit are independent. In addition, since $i = 0$, $v_2 = 0$ and $v_3 = v_s = 10$ V. From voltage divider, we have $v_1 = 3.33$ V (similar to case 3).

To check our assumption, we note $v_{D1} = v_1 - v_2 = 3.33 - 0 = 3.33 > 0.7$ V so D1 cannot be OFF and assumption was incorrect.

As can be seen, the simplest circuit is when diodes are OFF as the circuit usually divides into several simpler circuits. As such, if one cannot make an educated guess regarding the state of the diodes, it is usually best to start the analysis with diodes being OFF.

Part B: Parametric Solution: Here, we have to consider four cases. As discussed above, we will start with simplest cases (diodes OFF).

Case 1: D1 and D2 are both OFF: we see that two branches of the circuit are independent. In addition, since $i = 0$, $v_2 = 0$ and $v_3 = v_s$. From voltage divider, we have $v_1 = v_s/3$.

To find the range of validity of this solution,

$$v_{D1} = v_s/3 < V_{D0} \quad \rightarrow \quad v_s < 2.1 \text{ V}$$
$$v_{D2} = v_3 - v_2 < V_{D0} \quad \rightarrow \quad v_s < 0.7 \text{ V}$$

For both diodes to be OFF, we need $v_s < 0.7$ V (the most restrictive of both conditions).

So, for $v_s < 0.7$ V, both diodes will be OFF, $i = 0$ and $v = 0$

Case 2: D1 OFF and D2 ON: we see that two branches of the circuit are independent. From voltage divider, we have $v_1 = v_s/3$ V.

$$i = i_{D2} = \frac{v_s - 0.7}{10 \times 10^3 + 5 \times 10^3} = 6.67 \times 10^{-5}(v_s - 0.7)$$
$$v = 5 \times 10^3 i = 0.33(v_s - 0.7)$$

To find the range of validity of this solution,

$$i_{D2} = 6.67 \times 10^{-5}(v_s - 0.7) \geq 0 \quad \rightarrow \quad v_s \geq 0.7 \text{ V}$$
$$v_{D1} = v_1 - v_2 < V_{D0} \quad \rightarrow \quad \frac{v_s}{3} - 10 \times 10^3 i < 0.7$$
$$0.33 v_s - 0.67(v_s - 0.7) < 0.7 \quad \rightarrow \quad v_s > -0.7 \text{ V}$$

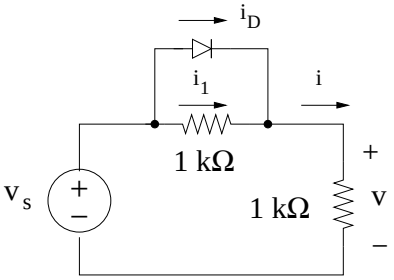
For D1 OFF and D2 ON, we need $v_s \geq 0.7$ V (the most restrictive of both conditions).

So, for $v_s \geq 0.7$ V, D1 OFF and D2 ON, $i = 6.67 \times 10^{-5}(v_s - 0.7)$ and $v = 0.33(v_s - 0.7)$.

Since for $v_s < 0.7$ V, both diodes will be OFF and for $v_s > 0.7$ V, D1 is OFF and D2 is ON, there is no range of values for v_s when other cases (D1 ON and D2 OFF or both ON) are possible.

Exercise: Solve circuit equations directly to show that D1 ON and D2 OFF Case or both diodes ON Cases are not physically possible.

Problem 8. In circuit below with Si diodes ($V_{D0} = 0.7$ V) and $V_Z = 5$ V for Zener diodes, A) Find v and/or i for $v_s = 10$ V, B) Find v and/or i for v_s ranging from -20 to $+20$ V.



Part A: $v_s = 10$ V.

Assume diode is OFF: $i_D = 0$ and $v_D < V_{D0} = 0.7$ V. Then $i_1 = i = v_s/(10^3+10^3) = 5$ mA and $v = 10^3 i = 5$ V.

To check the our assumption, we note $v_D = 10^3 i_1 = 5 > 0.7$ V, so the assumption is incorrect.

Assume diode is ON: $v_D = V_{D0} = 0.7$ V and $i_D \geq 0$ Then by KVL: $v = v_s - v_D = 9.3$ V and $i = v/10^3 = 9.3$ mA.

To check the our assumption, we note $i_1 = v_D/10^3 = 0.7$ mA and by KCL $i_D = i - i_1 = 8.6$ mA. Since $i_D > 0$, our assumption is correct.

Therefore, diode is ON and $i = 9.3$ mA and $v = 9.3$ V.

Part B: Parametric Solution:

Case 1: Assume diode is ON: $v_D = V_{D0} = 0.7$ V and $i_D \geq 0$.

KVL: $\quad v = v_s - v_D = v_s - 0.7$

To check the region of validity of our assumption we need to calculate i_D:

$$i_1 = \frac{v_D}{10^3} = 0.7 \times 10^{-3} \text{ A} = 0.7 \text{ mA} \quad \text{and} \quad i = \frac{v}{10^3} = 10^{-3} \times (v_i - 0.7)$$

$$i_D = i - i_1 \geq 0 \quad \rightarrow \quad 10^{-3} \times (v_s - 0.7) - 0.7 \times 10^{-3} \geq 0 \quad \rightarrow \quad v_s \geq 1.4 \text{ V}$$

So, if $v_s \geq 1.4$ V, the diode will be ON and $v = v_s - 0.7$ V.

Case 2: Assume diode is OFF: $i_D = 0$ and $v_D < V_{D0} = 0.7$ V.

KCL: $\quad i = i_1 + i_D = i_1$

KVL: $\quad v_s = 10^3 i_1 + 10^3 i = 2 \times 10^3 i \quad \rightarrow \quad i = i_1 = 0.5 \times 10^{-3} v_s$

$\qquad v = 10^3 i = 0.5 v_s$

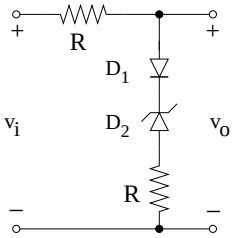
To check the region of validity of our assumption we need to calculate v_D:

$$v_D = v_s - v = v_s - 0.5 v_s = 0.5 v_s$$

$$v_D < V_{D0} \quad \rightarrow \quad 0.5 v_s < 0.7 \quad \rightarrow \quad v_s < 1.4 \text{ V}$$

So, if $v_s < 1.4$ V, the diode will be OFF and $v = 0.5 v_s$.

Problem 10. Find transfer function of the circuit below (Si diodes with V_{D0}=0.7 V and $V_Z = 5$ V for Zener diodes).



The regular diode can have two states (ON and OFF) and the Zener diode has three states (ON, OFF, and Zener). So, it appears that we need to consider $2 \times 3 = 6$ possible cases. However, an examination of the circuit shows that only two of these six combinations are possible by nothing $i_{D1} = -i_{D2}$.

If D1 is ON, $i_{D1} \geq 0$. This means that $i_{D2} < 0$ and D2 diode has to be in Zener state.

If D2 is OFF, $i_{D1} = 0$. This means that $i_{D2} = 0$ and D2 diode has to be OFF.

Case 1: D1 is ON ($v_{D1} = V_{D0} = 0.7$ V, $i_{D1} \geq 0$) and D2 is in Zener state ($v_{D2} = -V_Z = -5$ V and $i_{D2} \leq 0$). By KVL:

$$v_i = Ri_{D1} + v_{D1} - v_{D2} + Ri_{D1} \quad \rightarrow \quad i_{D1} = \frac{v_i - v_{D1} + v_{D2}}{2R}$$

$$v_o = v_i - Ri_{D1} = v_i - 0.5(v_i - v_{D1} + v_{D2}) = 0.5(v_i + v_{D1} - v_{D2}) = 0.5(v_i + 5.7)$$

The range of validity of this solution can be found by setting $i_{D1} \geq 0$ ($i_{D2} \leq 0$ will be automatically satisfied).

$$i_{D1} = \frac{v_i - v_{D1} + v_{D2}}{2R} \geq 0 \quad \rightarrow \quad v_i \geq v_{D1} - v_{D2} = 0.7 + 5.0 = 5.7 \text{ V}$$

Case 2: D1 and D2 are OFF ($i_{D1} = i_{D2} = 0$, $v_{D1} < V_{D0} = 0.7$ V, $-V_Z < v_{D2} < V_{D0} = 0.7$ V).

In this case, $v_o = v_i - Ri_{D1} = v_i$.

The range of validity of this solution can be found by noting:

$$v_{D1} - v_{D2} = v_o = v_i$$

$$v_{D1} < V_{D0} \quad \text{and} \quad -V_{D0} < -v_{D2} < V_Z$$

$$v_{D1} - v_{D2} < V_{D0} + V_Z \quad \rightarrow \quad v_i < V_{D0} + V_Z = 5.7 \text{ V}$$

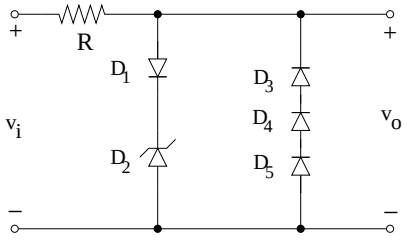
Transfer function:

$$v_i < 5.7 \text{ V} \quad \rightarrow \quad v_o = v_i$$

$$v_i \geq 5.7 \text{ V} \quad \rightarrow \quad v_o = 0.5(v_i + 5.7) \text{ V}$$

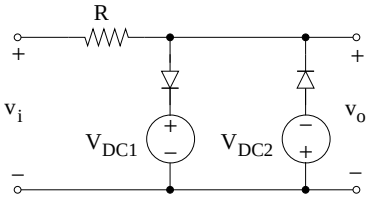
Problem 12. Find v_o for $v_s = V_s \sin(\omega t)$.

Diodes D3, D4, and D5 all have the same state (all are ON or all OFF). So, they act like ONE diode with a cut-in voltage of $3V_{D0} = 2.1$ V. Therefore, examination of the circuit shows that this is a clipper circuit. It clips the input voltage above $V_{D0} + V_Z = 5.7$ V and clips the voltage below $-3V_{D0} = -2.1$ V

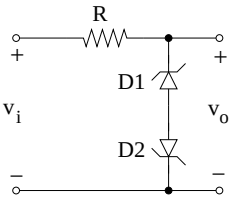


Problem 14. Design a clipper circuit that clips voltages above 5 V and below -3 V using a) DC power supplies only, b) Zener diodes only.

Part A: Set $v_{DC1} + V_{D0,1} = 5$ or $v_{DC1} = 4.3$ V
Set $-v_{DC2} - V_{D0,2} = -3$ or $v_{DC2} = 2.3$ V



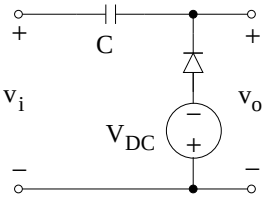
Part B: Set $V_{Z,1} + V_{D0,2} = 5$ or $V_{Z,1} = 4.3$ V
Set $-V_{Z,2} - V_{D0,1} = -3$ or $V_{Z,2} = 2.3$ V



Problem 16. Consider a sinusoidal source with $v_i = 15 \sin(\omega t)$ V. Design a clamp circuit that adds a DC offset of +5 to the input voltage using a) DC power supplies only, b) Zener diodes only.

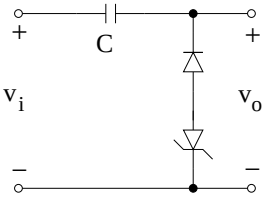
Part A: Prototype of circuit is shown with $v_o = v_i + (V^- - V_{D0} - v_{DC})$. Since $V^+ = V^- = 15$ V:

$$V^- - V_{D0} - v_{DC} = 5 \quad \rightarrow \quad v_{DC} = 15 - 0.7 - 5 = 9.3 \text{ V}$$



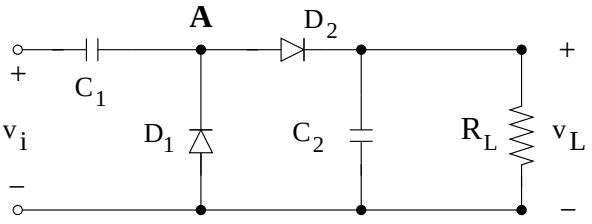
Part B: Prototype of circuit is shown with $v_o = v_i + (V^- - V_{D0} - V_Z)$.

$$V^- - V_{D0} - V_Z = 5 \quad \rightarrow \quad V_Z = 15 - 0.7 - 5 = 9.3 \text{ V}$$



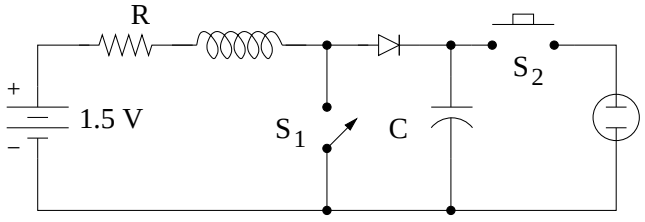
Capacitor values (or the load) should be chosen such that $R_L C = \tau \gg T$.

Problem 18. Circuit below is a "voltage doubler." Show that if $v_i = V_p \sin(\omega t)$, $v_o = 2V_p$ (Assume that capacitor C is large such that it discharge very little per cycle and $V_p \gg V_{D0}$.)



Capacitor C1 and diode D1 form a clamp circuit. As a result the voltage at point A is a sinusoidal voltage with a DC offset of V_p (ignoring V_{D0}). Diode D2 and capacitor C2 form a peak-detector circuit. They will generate a DC signal with a value which is equal to the peak of AC signal or $2V_p$

Problem 19. Circuit below is a simplified version of an electronic flash for cameras. Switch S2 is controlled by the shutter and is closed to operate the flash bulb. Normally switch S2 is open. The circuit to the left of switch S2 charges the capacitor to about 100 V using a 1.5 V battery. Switch $S1$ is an electronic switch that is opened and closed at about 10 kHz. As a result, the capacitor is charged to about 100 V using a 1.5 V battery. Explain how the charge-up circuit works.



When the electronic switch is closed, the battery increases the inductor current, *i.e.,* inductor charges up as its magnetic stored energy increases. When the electronic switch opens, the inductor current cannot change suddenly. The inductor current has to flow through the diode and the capacitor which charges up the capacitor and increases its voltage (Note $i_L = i_C = Cdv_c/dt > 0$ leads to an increase in v_c). So each time, the electronic switch closes and opens, the capacitor voltage is increased. When the capacitor reaches its desired voltage, the electronic switch stays at open position. Diode D1 prevents the capacitor to discharge back into the power supply and resistor R.

Note that The inductor can charge the capacitor voltage to a high value without violating KVL as during the capacitor charge up cycle, a negative voltage appears across the inductor $v_L = Ldi/dt$ which means that capacitor voltage would become much larger than the battery voltage.