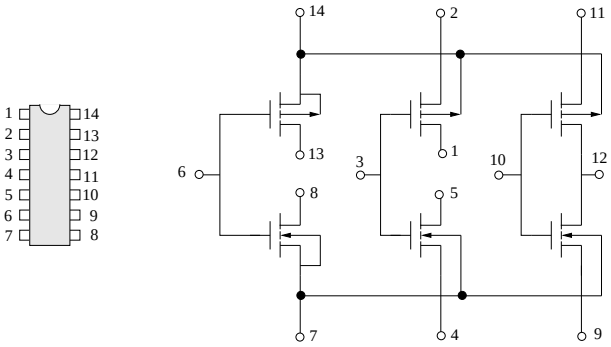
University of California, San Diego
Department of Electrical and Computer Engineering

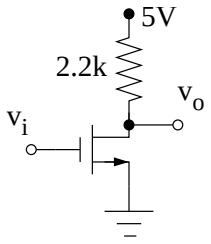
ECE65, Winter 2012

Lab 5, Logic Gates

Note: In this Lab we use CD4007 chip that consists of 3 pairs of complementary n-channel and p-channel MOSFETs. One pair is internally wired as a CMOS inverter. The pin arrangement for the chip is shown below. You need to power the chip by attaching a 5 V supply to pin 14 ($V_{DD} = 5$ V) and grounding pin 7. Note that by grounding pin 7, all MOSFET "bodies" are connected to the lowest voltage in the circuit, 0 V. Use $V_t = 1.4$ V for your calculations.



Experiment 2: NMOS Inverter



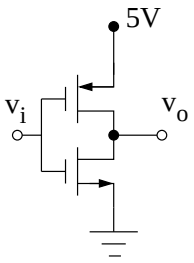
Circuit Analysis:
Compute values of v_o for $v_i = 0$, 2.5, and 5 V.
Use $k'_n(W/L)_n = 0.3$ mA/V^2 for this part.

Lab Exercise:
For this experiment use the NMOS inverter that is attached to pins 6, 7, and 8. Assemble the circuit on the protoboard. Set up the function generator to produce a triangular wave with a peak-to-peak amplitude of 5 V and a DC offset of 2.5 V similar to experiment 1. Attach scope channel A to the input and channel B to the output of the gate. Set the scope display to XY mode. You should see the transfer characteristics of the inverter circuit on the scope display.

a) Make a hard copy of the transfer function and on the hard copy, draw v_i and v_o axes and label and mark the voltage scales. Identify regions in which MOS is in cut-off, ohmic, and active regions.

b) Measure v_o for $v_i = 2.5$ and 5 V. In each case, solve the MOS circuit and find the value of the parameter $k'_n(W/L)_n$.

Experiment 3: CMOS Inverter



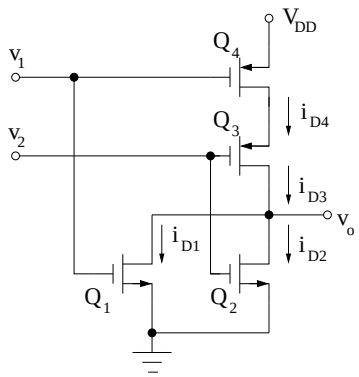
Circuit Analysis: Compute values of i_D for $v_i = 2.5$ V.
Use $k'_n(W/L)_n = k'_p(W/L)_p = 0.3$ mA/V^2.

Lab Exercise:
For this experiment use the CMOS inverter that is attached to pins 9 through 12. Assemble the circuit on the protoboard. As in experiment 1, set up the function generator to produce a triangular wave with a peak-to-peak amplitude of 5 V and a DC offset of 2.5 V. Apply this signal to the input of the gate. Attache scope channel A to the input and scope channel B to the output. Set the scope display to XY mode. You should see the transfer characteristics of the inverter circuit on the scope display.

a) Make a hard copy of the transfer function and on the hard copy, draw V_i and V_o axes and label and mark the voltage scales.

b) A major advantage of CMOS inverter is that it draw zero current when it is in high or low state. However, the drain current is not zero when CMOS is transitioning between states. To see this, attach a 100 Ω resistor between pin 9 and ground. The voltage across this resistor will be proportional to drain current. Apply the triangular wave above to the input of the gate. Attach scope channel A to the input and scope channel B to the 100 Ω resistor. Set the scope display to XY mode. You should see a plot of i_D vs v_i. Make a hard copy and on the hard copy, draw v_i and i_D axis and label and mark the voltage and current scales. Compare the maximum values of i_D with your calculations.

Experiment 4: CMOS NOR Gate



Circuit Analysis: Show that the circuit below acts as a NOR gate.

Lab Exercise:
For this experiment use the CMOS inverter that is attached to pins 9 through 12 and MOS transistors with the gate connected to pin 6. Draw the circuit diagram NOR gate in your lab report and identify chip pins on the circuit diagram and explain which pins should be connected together. Wire your chip to make a two-input NOR gate. Test your NOR gate with attaching a 1 kHz square wave (0-5 V) to pin 6 and a DC voltage of either zero or 5 V to pin 10. In each case, attached the waveform to the lab report. Describe the output waveform in each case and explain how it corresponds to the NOR of the two inputs, using a truth table format.