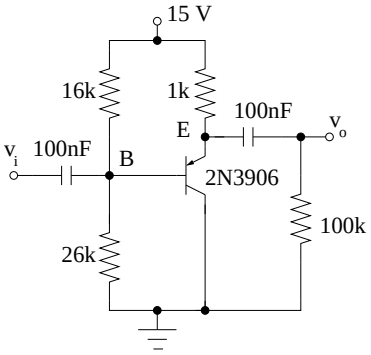
University of California, San Diego
Department of Electrical and Computer Engineering

ECE65, Winter 2012

Lab 7, BJT Amplifiers

Experiment 1: Emitter Follower

Circuit Analysis:
a) Compute the bias point
(assume $\beta = 200$, $V_A = 150$ V).



b) Compute the mid-frequency gain (with the load), input resistance, and lower cut-off frequency of this amplifier.

PSpice Simulation:
c) Simulate the circuit with PSpice (bias point details) and compare bias point values with part a.

d) Simulate the frequency response of the circuit in the frequency range of 10 Hz to 1 MHz. Print out the Bode plots (gain in dB and phase). Compare your simulation results with part b results.

e) Using your simulations of part d, plot the input resistance ($R_i = v_i/i_i$) of this amplifier as a function of frequency. Compare with part b results. Explain your observations.

Lab Exercise:
f) Build the circuit. Measure bias voltages and currents and compare with analysis results of part a and simulation results of part c.

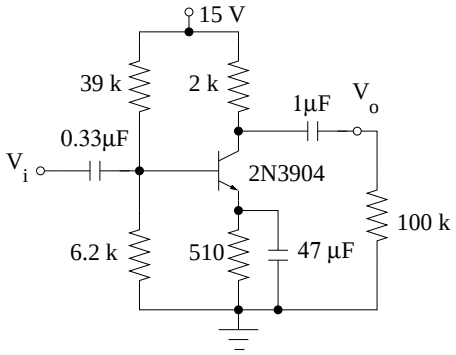
g) Set v_i to be a sinusoidal wave with a frequency of 2 kHz and an amplitude of 3 V (no DC offset). Print out the input and output signals (same plot). Is there a phase shift?. Measure the gain of the amplifier and compare it with calculation (part b) and simulation (part d) results.

h) With scope channel 1 still on the input, attach scope channel 2 to points B and then to point E. At each point, measure the signal amplitude and its DC offset. Compare measured voltage at B, E, and the output with the input signal. Explain your observations.

i) Measure the lower cut-off frequency of the amplifier (see page 2).

j) With v_i back at 2 kHz, increase the amplitude of v_i and watch v_o on the scope. At some v_i ampitude, the output is NOT a sin wave any more. Record the v_i amplitude that this happens and explain your observation (you need to do some calculations to justify your explanation).

Experiment 2: Common Emitter



Circuit Analysis:
a) Compute the bias point
(assume $\beta = 200$, $V_A = 150$ V).

b) Compute the mid-frequency gain (with the load), input resistance, and lower cut-off frequency of this amplifier.

PSpice Simulation:
c) Simulate the circuit with PSpice (bias point details) and compare bias point values with part a.

d) Simulate the frequency response of the circuit in the frequency range of 10 Hz to 1 MHz. Print out the Bode plots. Compare your simulation results with part b results.

Lab Exercise:
e) Build the circuit. Measure bias voltages and currents and compare with analysis results of part a and simulation results of part c.

f) Set the function generator to produce a sinusoidal wave with a frequency of 2 kHz and amplitude of 0.02 V. (Use 20 dB attenuation button on the function generator). Print out the input and output signals (same plot). Is there a phase shift?. Measure the gain of the amplifier and compare with calculation (part b) and simulation (part d) results.

g) Measure the lower cut-off frequency of the amplifier.

How to measure the cut-off frequency:

The cut-off frequency is defined to be the frequency at which the gain of the amplifier is reduced by $1/\sqrt{2} \approx 0.7$ from its maximum value (*i.e.,* the mid-frequency gain). Therefore, if we keep v_i amplitude constant, the amplitude of v_o at the cut-off frequency should be 0.7 of its maximum value.

Measurement: With function-generator amplitude fixed, find amplitude of v_o to the mid-frequency gain (scan the frequency until v_o amplitude reaches its maximum and does not change). Use this maximum v_o value to calculate v_o amplitude corresponding to the cut-off frequency. Reduce the frequency of the input (without changing v_i amplitude) until the amplitude of v_o reaches the calculated value corresponding to the cut-off frequency. Read the frequency from the scope.