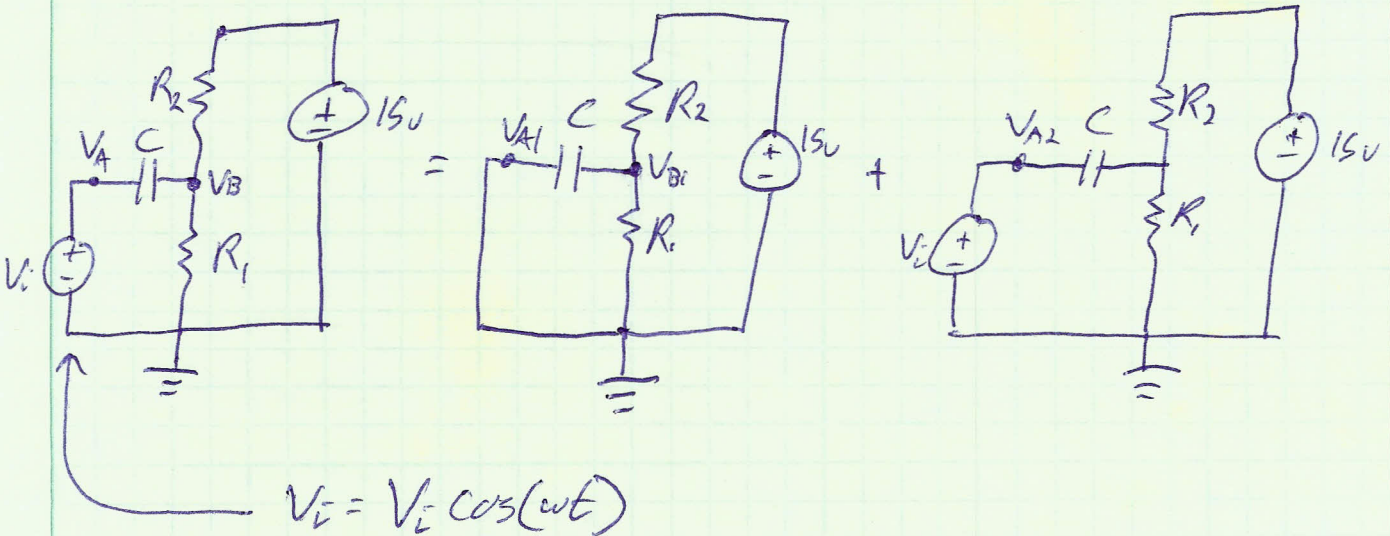
Issues with amplifiers

- BJT must remain in active state
  - if $I_B + \Delta i_B < 0$, it reaches cut-off
  - at high current, it will reach saturation
- The inputs and outputs have unwanted DC components
  - eliminate by capacitive coupling
- The amplifier must be linear
  - trade-off between linearity and power consumption

Capacitive Coupling

- Capacitors are open circuits for DC
- for higher frequencies, $Z = \frac{1}{j\omega C}$
  - we can choose value of C so that impedance is small

Importance of superposition



$V_i = V_i \cos(\omega t)$

Solve the circuit by superposition
- kill each source, and analyze the circuit with just the other source

Circuit #1

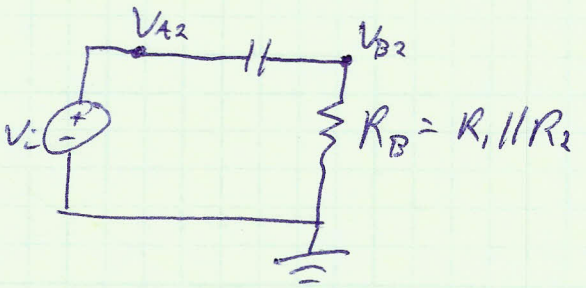
- Only DC source → capacitor is open circuit

$$V_{A1} = 0 \quad , \quad V_{B1} = 15 \frac{R_1}{R_1 + R_2}$$

Circuit #2

- R_1 and R_2 are in parallel

equivalent to :



This is a high-pass filter

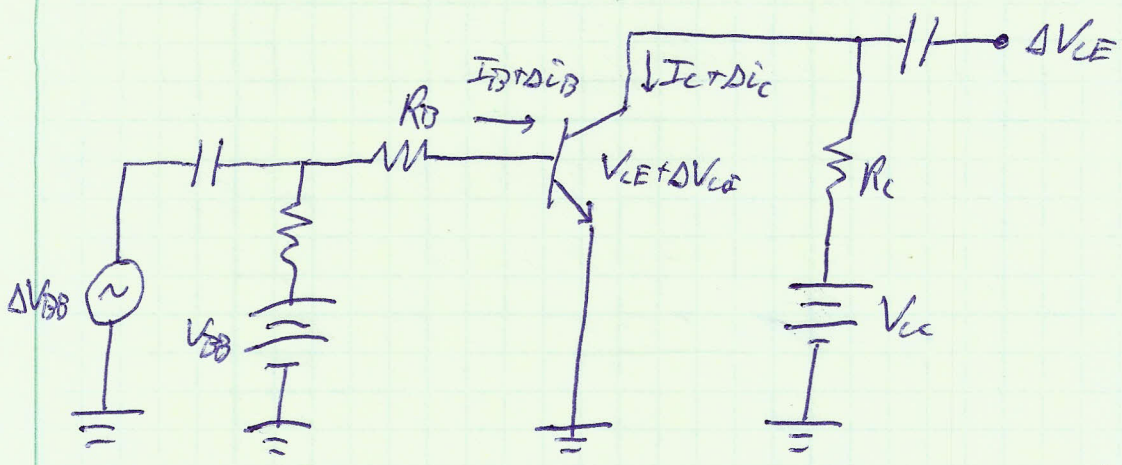
$$V_{B2} = V_i \frac{R_B}{R_B + \frac{1}{j\omega C}} = V_i \frac{j\omega R_B C}{j\omega R_B C + 1}$$

if $\omega R_B C \gg 1$, $V_{B2} \simeq V_i$

$$V_A = V_{A1} + V_{A2} = 0 + V_i \cos(\omega t)$$

$$V_B = V_{B1} + V_{B2} = 15 \times \frac{R_1}{R_1 + R_2} + V_i \cos(\omega t)$$

- capacitor prevents DC voltage from appearing at point A
- point B contains sum of both voltages



- Use capacitors at both the input and output to separate the signals

Notation

- Bias components: V_{BE}, I_B, etc — Upper upper
- signal components: v_{be}, i_b, etc — lower lower
- Total: v_{BE}, i_B — lower Upper

Superposition

- Can only really be used for linear circuits, and these are nonlinear
- with small signal model, we treat the transistor as approximately linear
- we extract the signals in the lower part of the circuit (not inside the transistor)

Fourier analysis

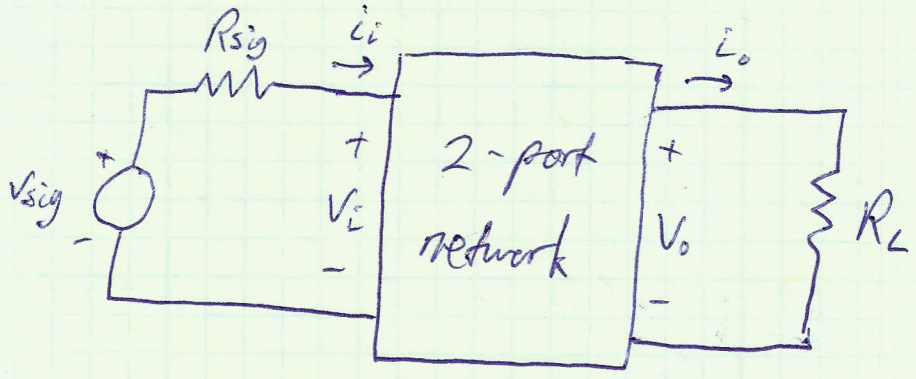
- we used sine waves in our analysis
- signals can always be decomposed into sine waves

DC Amplifiers (vs AC)

- With capacitive coupling we have an AC amplifier
- lower frequency cutoff determined by value of coupling capacitors
- different design needed for DC

Transistor Amplifiers

Two-port network

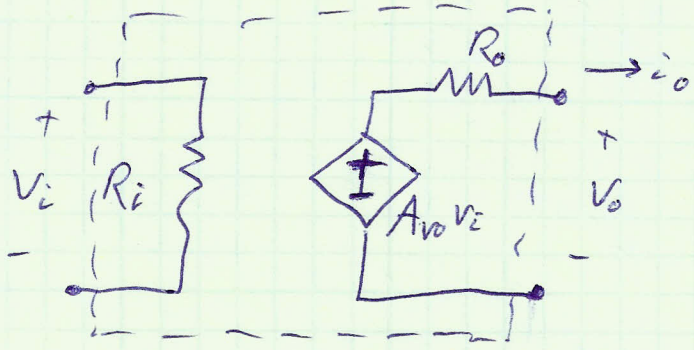


can be modeled with three elements:

- Input resistance $R_i = \frac{v_i}{i_i}$ (depends on R_L in general)
- Output resistance $R_o = \left.\frac{-v_o}{i_o}\right|_{v_i=0}$

  (note - assume v_i applied directly to input port: $v_{sig} = v_i$, $R_{sig} = 0$)
- Open-loop gain $A_{vo} = \frac{v_{oc}}{v_i} = \left.\frac{v_o}{v_i}\right|_{R_L \to \infty}$

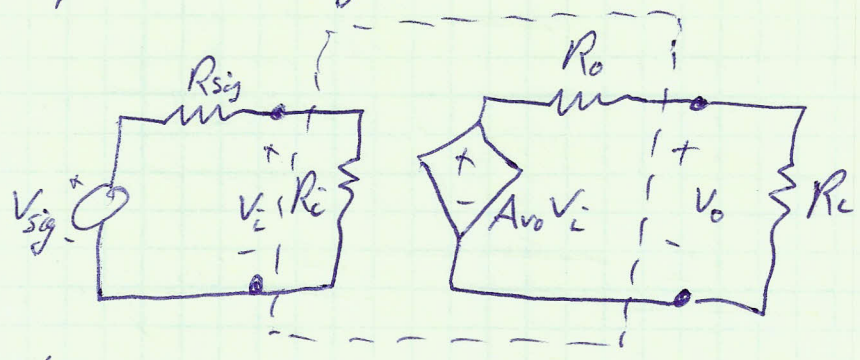
Amplifier Model



Can solve any amplifier circuit once to determine these parameters

Similar to Thevenin theorem

Response to R_{sig} and R_L:



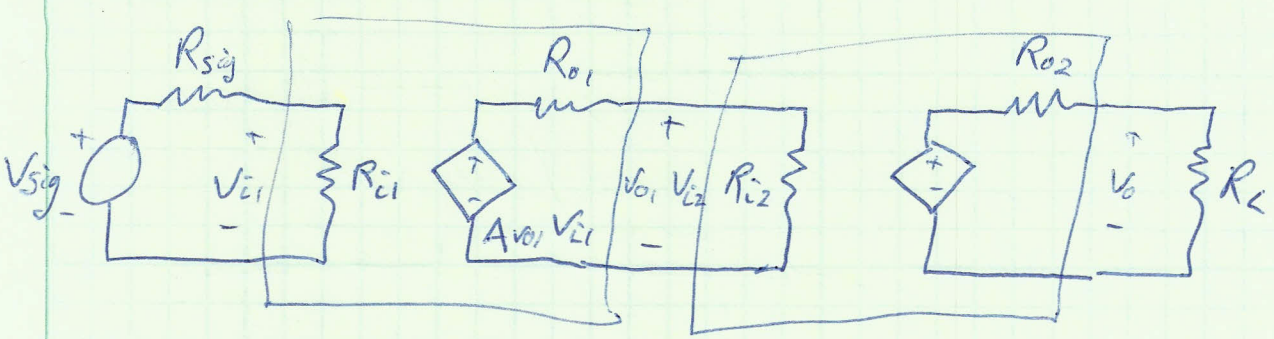
amplifier gain $A_v = \frac{V_o}{V_i} = \frac{R_L}{R_o + R_L} A_{vo}$ (voltage divider at output)

$\frac{V_i}{V_{sig}} = \frac{R_i}{R_i + R_{sig}}$ (voltage divider at input)

$\frac{V_o}{V_{sig}} = \frac{V_i}{V_{sig}} \cdot \frac{V_o}{V_i} = \frac{R_i}{R_i + R_{sig}} \cdot A_v = \frac{R_i}{R_i + R_{sig}} \cdot A_{vo} \cdot \frac{R_L}{R_o + R_L}$

- Note that A_{vo} is the <u>maximum</u> amplifier gain
- to maximize $\frac{V_o}{V_{sig}}$, need $R_i \to \infty$, $R_o \to 0$
  - voltage controlled voltage source is "ideal" amplifier

2-stage amplifier



$$\frac{V_o}{V_{sig}} = \frac{R_{i1}}{R_{i1}+R_{sig}} \times A_{vo1} \times \frac{R_{i2}}{R_{i2}+R_{o1}} \times A_{vo2} \times \frac{R_L}{R_{o2}+R_L}$$

- To maximize voltage gain, input resistance of each stage must be much larger than the output resistance of the previous stage
- Often simpler to calculate A_v instead of A_{vo} ← no load
  ↑ load is present

$$\frac{V_o}{V_{sig}} = \frac{R_{i1}}{R_{i1}+R_{sig}} \times A_{v1}(R_L = R_{i2}) \times A_{v2}(R_L = R_L)$$

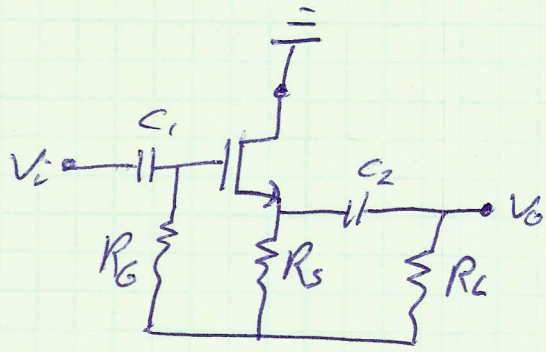
- Note that R_i may depend on R_L

Analysis of Transistor Amplifiers

- Calculate Bias Conditions
- Calculate small signal response
  - find g_m, r_o, (and r_π for BJT) from bias
  - zero the bias sources
  - assume capacitors are short circuits
  - replace transistor with small signal model
  - inspect circuit:
    - if prototype circuit, use formulas for that circuit
    - otherwise, find R_i, R_o, A_v, A_{vo}
- Calculate frequency response
  - we will learn how to calculate low frequency poles due to coupling caps
  - you will learn more details of frequency response in ECE102

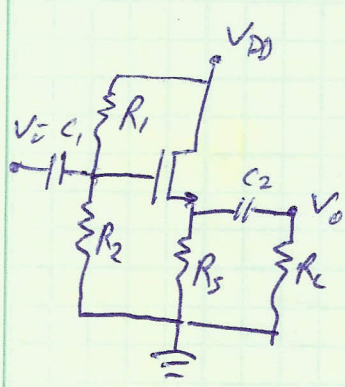
Common Drain and Common Collector Amplifiers

- Common Drain (source follower)

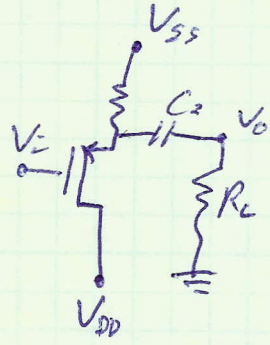


- Note: Drain is grounded for small signals, so it is the "common" terminal of input and output

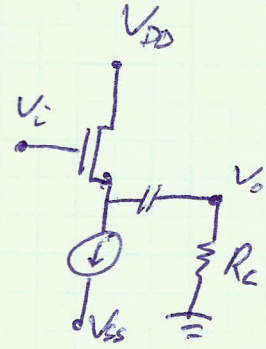
- Several circuits reduce to this form:



$R_G = R_1 \| R_2$

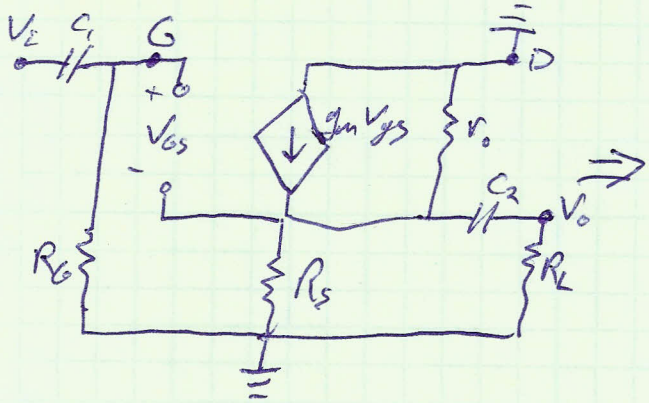


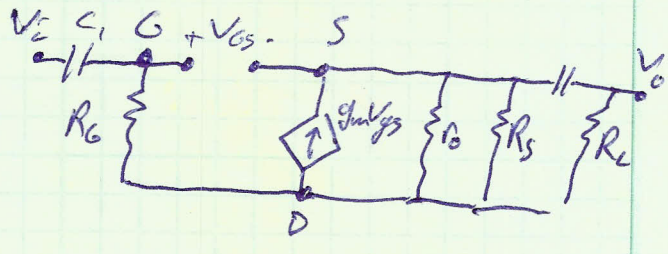
$R_G \to \infty$



$R_G \to \infty$, $R_S \to \infty$

Replace MOSFET with small signal model





- Note that R_S parallel to R_L. In practice, R_S often replaced by the load
- define $R_L' = R_S \| R_L$
- open-loop gain found by setting $R_L' \to \infty$

$v_{gs} = v_i - v_o$

$v_o = g_m v_{gs}(r_o \| R_L') = g_m(r_o \| R_L')(v_i - v_o)$

$$A_v = \frac{v_o}{v_i} = \frac{g_m(r_o \| R_L')}{1 + g_m(r_o \| R_L')} = \frac{g_m r_o R_L'}{r_o + R_L' + g_m r_o R_L'} \simeq \frac{g_m R_L'}{1 + g_m R_L'}$$

↑ use $g_m r_o \gg 1$ to drop this term, then divide top + bottom by r_o

to find open-loop gain, set $R_L' \to \infty$. $r_o \| R_L' = r_o$

$$A_{v_o} = \frac{g_m r_o}{1 + g_m r_o} \simeq 1$$

Because $A_{v_o} \simeq 1$, $v_o = v_s \simeq v_g = v_i$ → output "follows" input voltage

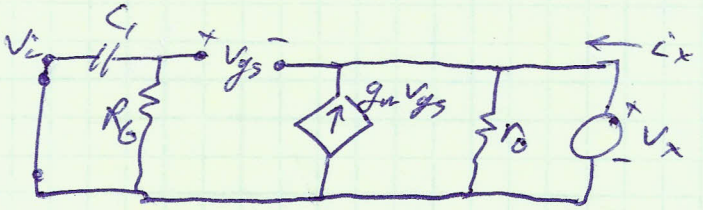
→ called <u>source follower</u>

<u>Input resistance:</u>

$R_i = R_G$ – no analysis needed

<u>Output resistance:</u>

Zero out v_i, then find Thevenin resistance seen at output



take out R_L'

$v_{gs} = v_i - v_x = -v_x$

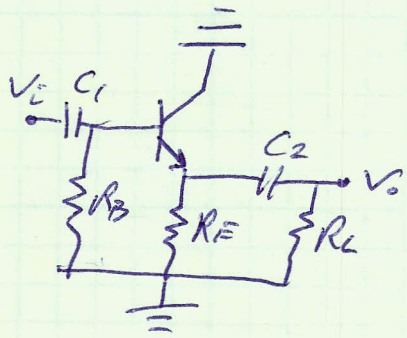
$$i_x = -g_m v_{gs} + \frac{v_x}{r_o} = v_x \frac{g_m r_o + 1}{r_o}$$

$$R_o = \frac{r_o}{1 + g_m r_o} \simeq \frac{1}{g_m}$$ → typically small – a few hundred Ω

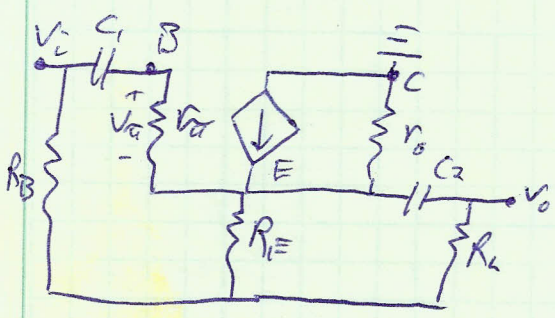
- Source follower has unity gain, but transforms high impedance to low impedance – often used as a <u>buffer</u> or for the final stage in power amplifiers

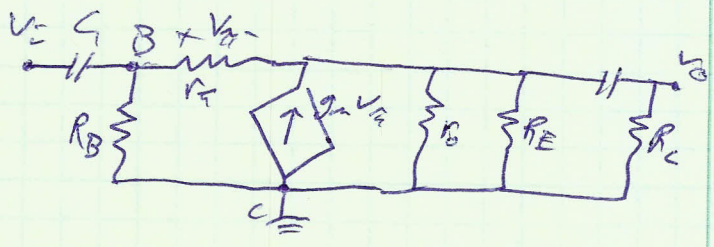
Common Collector or Emitter Follower

- Same basic idea as source follower
- Note we have zeroed out the bias sources
- Many circuits can be reduced to this form
- Define $R_L' = R_E \| R_L$



Small signal model:





note $V_\pi = V_i - V_o$

$i_b = V_\pi / r_\pi$

$g_m r_\pi = \beta \gg 1$ total current flowing through r_o and R_L' is i_b and $g_m V_\pi$

$$V_o = \left(g_m V_\pi + \frac{V_o}{r_o}\right)(r_o \| R_L') \simeq g_m V_\pi (r_o \| R_L') = g_m (r_o \| R_L')(V_i - V_o)$$

$$A_v = \frac{V_o}{V_i} \simeq \frac{g_m (r_o \| R_L')}{g_m (r_o \| R_L') + 1} = \frac{g_m r_o R_L'}{r_o + R_L' + g_m r_o R_L'} \simeq \frac{g_m R_L'}{1 + g_m R_L'}$$

(use $g_m r_o \gg 1$)

$$A_v = \frac{R_L'}{R_L' + r_e} \quad \text{where } r_e \equiv \frac{1}{g_m}, \text{ typically } \simeq \text{ few tens of ohms}$$

$$A_{vo} = \frac{g_m r_o}{1 + g_m r_o} \simeq 1$$

known as Emitter Follower

To find R_i:

$$i_i = \frac{v_i}{R_B} + i_b \quad \text{(KCL)}$$

(KVL)

$$v_i = i_b r_\pi + (i_b + g_m v_\pi)(r_o \| R_L') = i_b\left[r_\pi + (1+g_m r_\pi)(r_o \| R_L')\right]$$

$$i_i = \frac{v_i}{R_B} + i_b = \frac{v_i}{R_B} + \frac{v_i}{r_\pi + (1+\beta)(r_o \| R_L')}$$

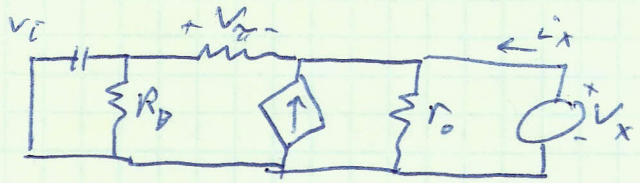
$$\frac{1}{R_i} = \frac{i_i}{v_i} = \frac{1}{R_B} + \frac{1}{r_\pi + (1+\beta)(r_o \| R_L')}$$

$$R_i = R_B \| \left[r_\pi + (1+\beta)(r_o \| R_L')\right]$$

- note R_i depends on R_L → this amplifier is not unilateral

To find R_o:

Zero out v_i, Remove R_L', attach V_x



$$i_x = -g_m v_\pi + \frac{v_x}{r_o} + \frac{v_x}{r_\pi}$$

note $v_\pi = -v_x$

$$\frac{1}{R_o} = \frac{1}{1/g_m} + \frac{1}{r_o} + \frac{1}{r_\pi} \rightarrow R_o = (1/g_m) \| r_o \| r_\pi \simeq 1/g_m = r_e$$

Since $g_m r_\pi \gg 1$, $g_m r_o \gg 1$

- Unity gain, large input resistance, small output resistance