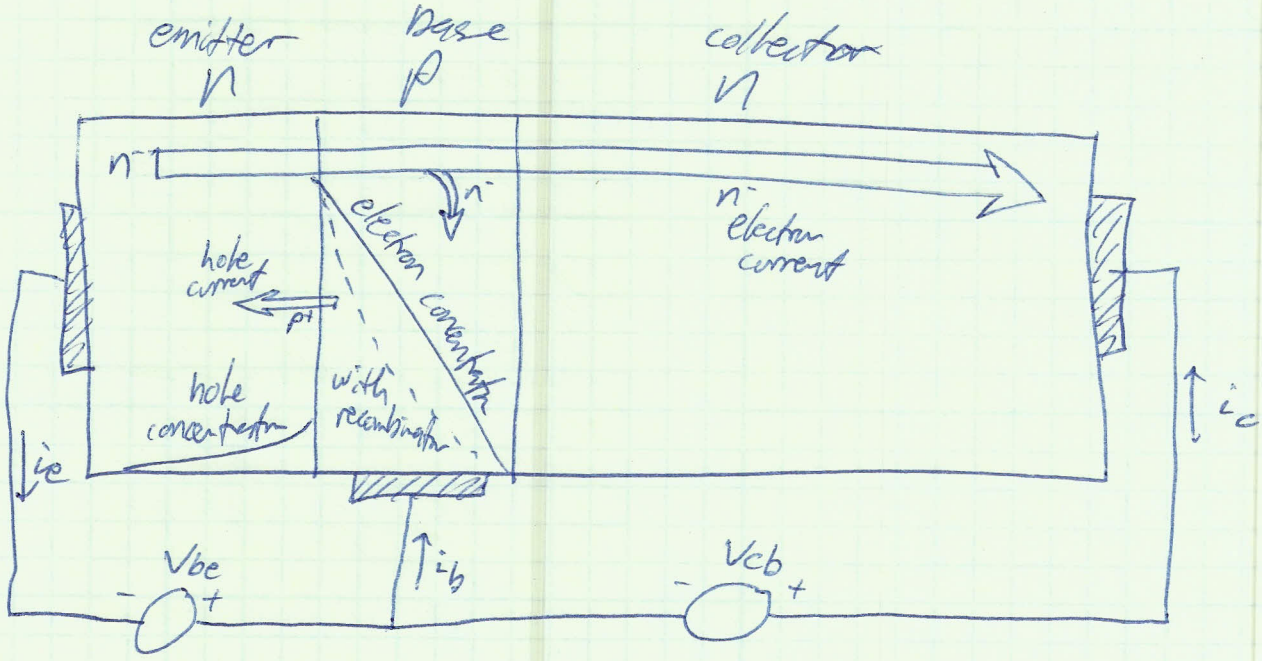
# Bipolar Junction Transistors (BJTs)




six parameters: $i_b$, $i_e$, $i_c$, $V_{be}$, $V_{ce}$, $V_{bc}$

using KVL, KCL: $i_e = i_c + i_b$, $V_{bc} = V_{be} - V_{ce}$

only four independent parameters: $i_b$, $i_c$, $V_{be}$, $V_{ce}$

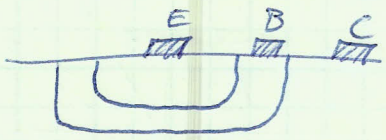
→ these specify <u>iv</u> characteristics of transistor

## Principle of operation:

- In active mode: emitter base junction is forward-biased
  collector base junction is reverse-biased
- Level of doping in emitter is <u>much higher</u> than in the base
  → electron current is <u>much greater</u> than hole current into emitter
- Bias conditions set up a <u>concentration gradient</u> across base
  → very high near emitter, very low near collector
  → causes diffusion current across base
  → electrons that reach collector are swept over to collector contact

- Emitter current is primarily electrons, and a small hole current into base
- Base current is small hole current and small electron recombination current
- Collector current is most of the electrons from the emitter

Typical design: Base is thin, and lightly doped
Emitter is heavily doped




- Note that current flows across base-collector junction even though it is reverse-biased. It is caused by concentration gradient in base, set up by base emitter junction
- Number of holes going into emitter (proportional to $i_B$) is a constant fraction of number of electrons going into base (proportional to $i_C$) This ratio depends on doping and design

$$\frac{i_C}{i_B} = \beta$$ - defined as common emitter current gain

typical value is ~ 200

(about 200 electrons travel for each hole)

| Mode | E-B junction | C-B junction |
|---|---|---|
| cutoff | reverse | reverse |
| active | forward | reverse |
| saturation | forward | forward |

## cutoff mode

B-E junction reverse biased, $i_B = 0 \rightarrow i_C = 0$

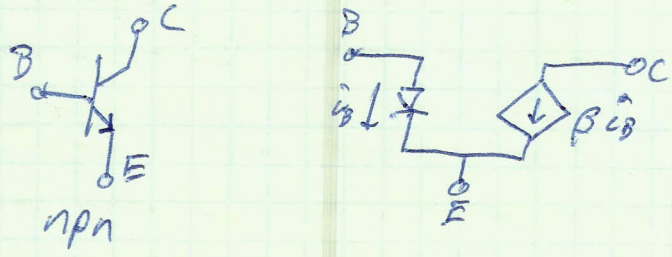
## active mode

most of the current flows to the collector

$$i_C = I_S\left(e^{v_{be}/nV_T} - 1\right) \approx I_S e^{v_{be}/nV_T}$$

$$i_B = \frac{I_S}{\beta}\left(e^{v_{be}/nV_T} - 1\right) \approx \frac{I_S}{\beta} e^{v_{be}/nV_T}$$

model for cutoff and active circuits:




## saturation mode

when $V_{CE} \lesssim V_{DO}$, B-C junction becomes forward biased

extra holes injected into base from collector recombine with electrons

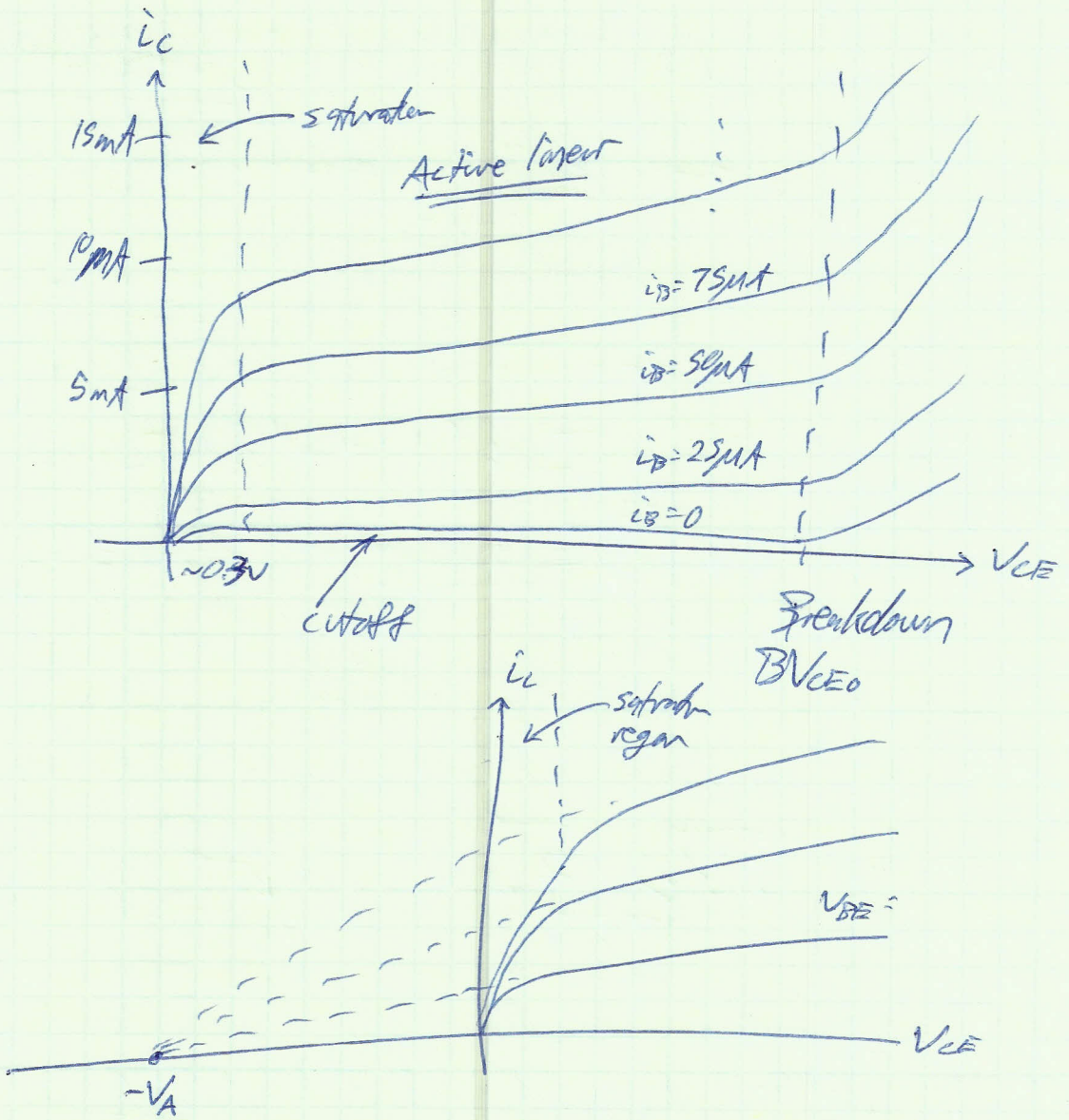
→ reduce collector current

$$i_C/i_B < \beta$$

"soft saturation" may be considered as around $V_{CE} = 0.4V$ ($V_{BE} = 0.3V$)

as transistor behaves similarly to active mode, $\frac{i_C}{i_B}$ not yet reduced significantly

→ slightly forward biased, but not yet to turn-on

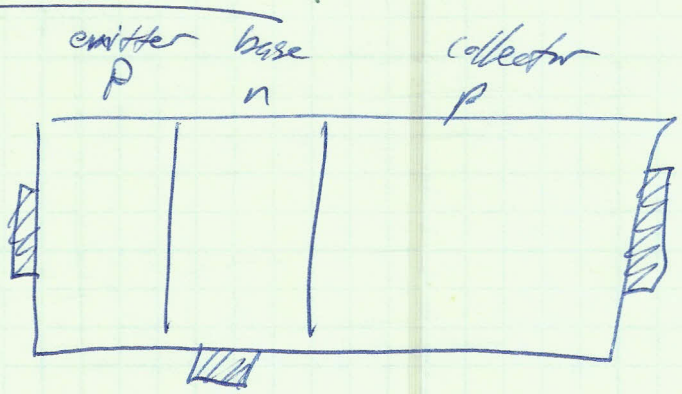


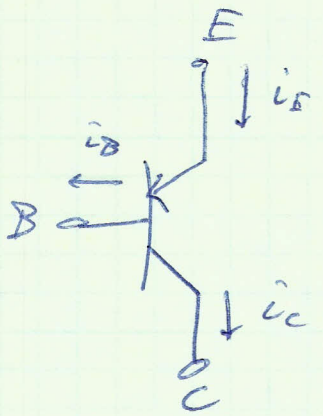

- The slope of the iv curves in the active region is due to the dependence of the depletion region width on $V_{BC}$
- wider depletion region → narrower effective Base width
- $V_A$ known as "Early voltage"
  - typically 50-100 V

$$i_C = I_S e^{V_{BE}/nV_T}\left(1 + \frac{V_{CE}}{V_A}\right)$$

$$i_B = \frac{I_S}{\beta} e^{V_{BE}/nV_T}$$ note $i_B$ equation doesn't change

## PNP transistor




- holes move slower than electrons (lower mobility) so pnp transistors are typically slower
- usually used in pairs with npn transistors

## Summary

cutoff : $i_B = 0$, $i_C = 0$

active : $i_B = \frac{I_S}{\beta} e^{V_{BE}/nV_T}$, $i_C = I_S e^{V_{BE}/nV_T}\left(1 + \frac{V_{CE}}{V_A}\right)$

saturation : $i_B = \frac{I_S}{\beta} e^{V_{BE}/nV_T}$, $i_C < \beta i_B$, $V_{CE} = 0.1 - 0.3\,V$

- known as "large signal model"
- low frequency model – does not include capacitance

# Piecewise Linear, Large Signal model for BJT

## Cut-off

$i_B = 0$ , $v_{BE} < V_{D0}$

$i_C = i_E = 0$

for PNP transistors
$V_{BE} \rightarrow V_{EB}$
$V_{CE} \rightarrow V_{EC}$

## Active

$V_{BE} = V_{D0}$ , $i_B \geq 0$

$i_C = \beta i_B$ , $V_{CE} > V_{D0}$

can ignore Early effect (5% error)
if necessary to include it, use $i_C = \beta i_B \left(1 + \frac{V_{CE}}{V_A}\right)$

for soft saturation, ($V_{CE} \geq 0.4v$) $i_C \simeq \beta i_B$
we can use $V_{CE} \geq 0.4v$ instead of $V_{CE} \geq V_{D0}$

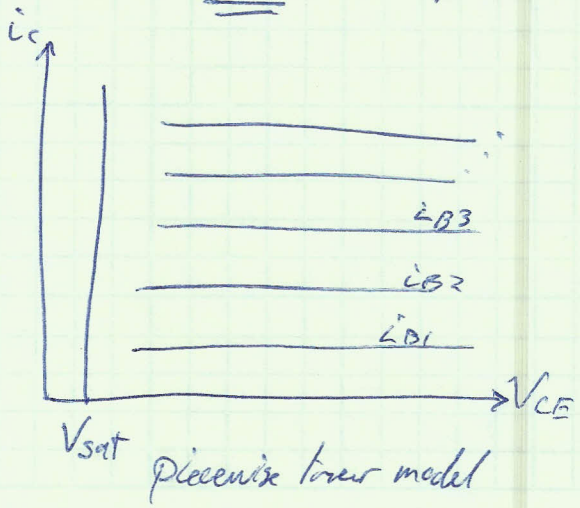
However - difficult to design in this region
- we will still use $V_{CE} \geq V_{D0}$ in this course

Model for saturation mode is complicated - we will use piecewise linear

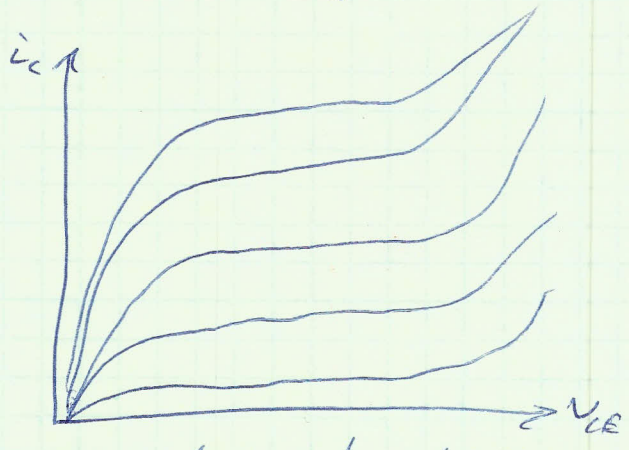
## Saturation mode ($0.1 \leq V_{CE} \leq 0.3v$)

$V_{BE} = V_{D0}$ , $i_B > 0$

$V_{CE} \simeq V_{sat}$ , $i_C < \beta i_B$ use $0.2v$ for $V_{sat}$




piecewise linear model




real i-v characteristic

## How to solve BJT circuits

Just like diode - assume a state, then check assumptions

- Write KVL for BE terminals
- Write KVL for CE terminals
- assume cut-off (simplest)
  - set $i_B = 0$
  - Calculate $V_{BE}$ from BE-KVL
  - ✱ - if $V_{BE} < V_{DO}$, BJT is in cut-off
    - set $i_C = i_E = 0$
    - calculate $V_{CE}$ from CE-KVL → you are done
  - ✱ - if $V_{BE} > V_{DO}$, BJT is not in cut-off
- assume linear mode
  - set $i_E \simeq i_C = \beta i_B$
  - calculate $V_{CE}$ from CE-KVL
- ✱ - if $V_{CE} > V_{DO}$, BJT is in active mode → you are done
- ✱ - if $V_{CE} < V_{DO}$, BJT is not in active mode - it is in saturation
  - set $V_{CE} = V_{sat}$
  - calculate $i_C$ from CE-KVL
  - check that $i_C < \beta i_B$

For PNP transistors, substitute $V_{BE}$ with $V_{EB}$
$V_{CE}$ with $V_{EC}$

Note that $V_{BE}$ not used

In active mode $i_E = i_C + i_B = (\beta+1) i_B$ and $i_E = \frac{\beta+1}{\beta} i_C$

since $\beta \gg 1$, use $i_E = i_C$ for simplicity

Even in saturation mode, $i_C \gg i_B$, $i_E \simeq i_C$