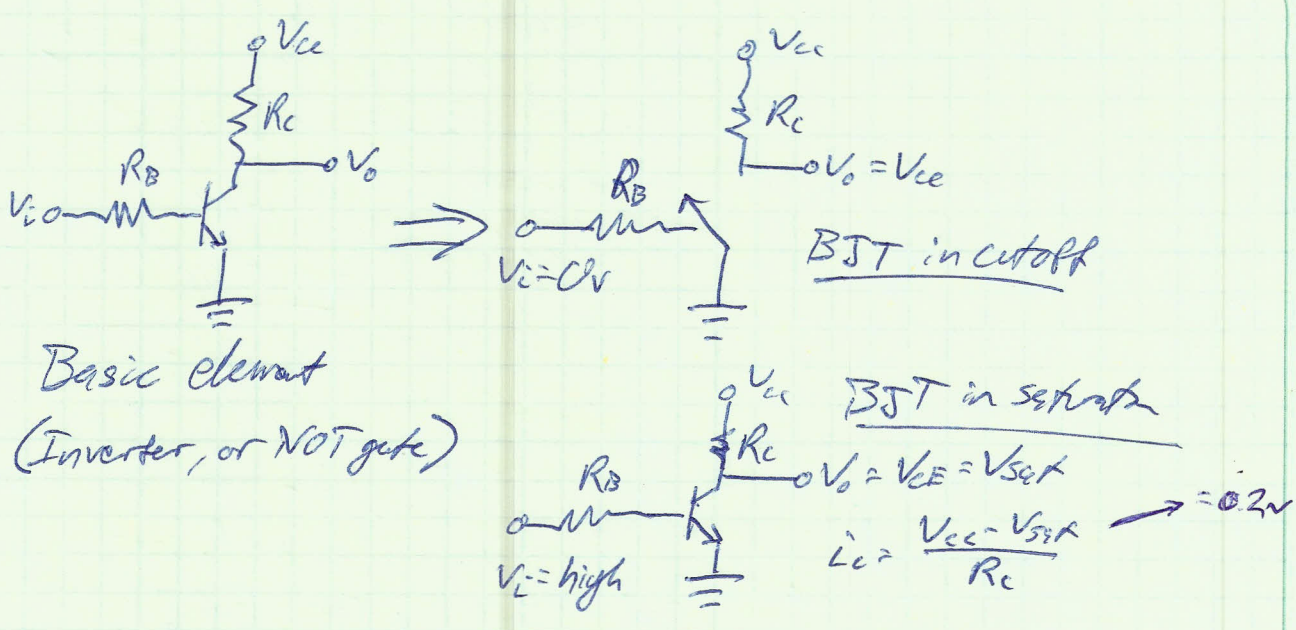
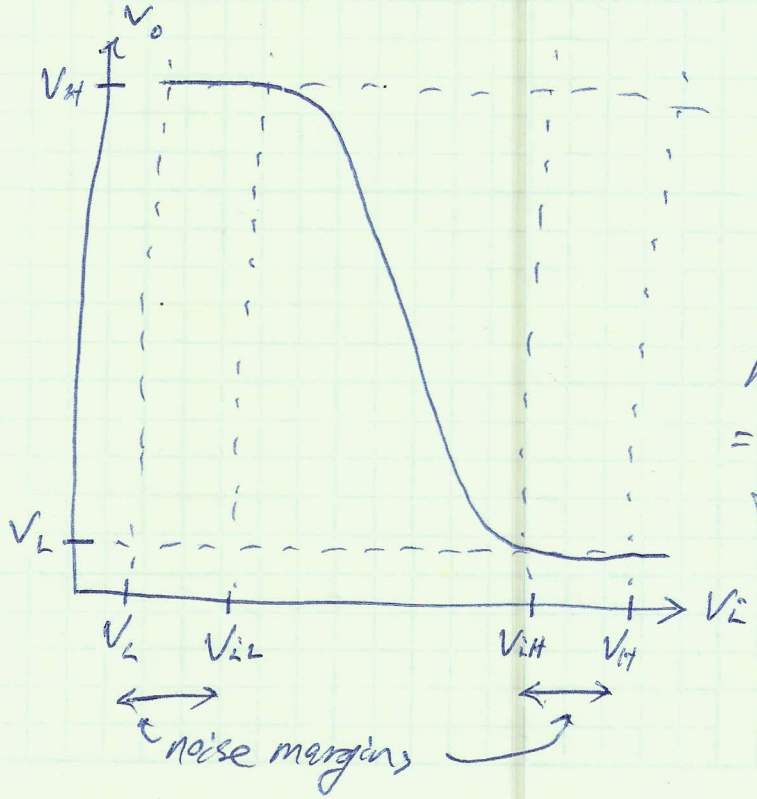
BJT Switches and Logic Gates



- In computer science, logic, etc., "0" = "OFF", "1" = "ON"
- To design logic circuits, we need to worry about actual voltage
- Choose e.g. $V_L = 0V$, $V_H = 5V$
  - must consider noise margin in low and high states

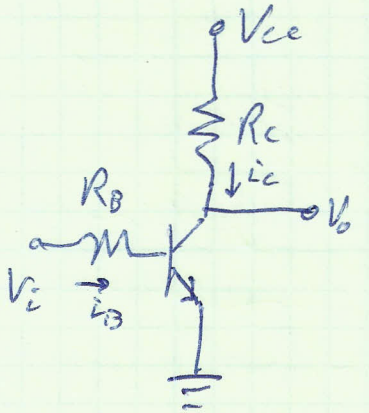
Transfer function of inverter:



low side noise margin = range of inputs V_i that still give $V_o = V_H$

high side noise margin = range of inputs V_i that still give $V_o = V_L$

Resistor - Transistor Logic (RTL)



Inverter circuit

low state $V_L = V_{sat} = 0.2V$

high state $V_H = V_{cc}$

Transfer function: (V_o for any V_i)

BE-KVL:

$V_i = R_B i_B + V_{BE}$

for $V_i < V_{DO}$, CUT-OFF, $i_C = 0$, $V_o = V_{cc}$ (high)

(when $V_i = V_L = V_{sat}$, $V_o = V_{cc} = V_H$)

output high as long as $V_i < V_{DO}$, $\rightarrow$ $\underline{V_{iL} = V_{DO}}$

- assume current just begins to flow at $V_i = V_{DO} \rightarrow i_B > 0$ but small

when $V_i > V_{DO}$, BE junction forward biased

$i_B = \dfrac{V_i - V_{DO}}{R_B}$ - transistor either in active or saturation region

assume saturation: $\left(\dfrac{i_C}{i_B} < \beta\right)$

$i_C = \dfrac{V_{cc} - V_{sat}}{R_C} \longrightarrow i_B > \dfrac{i_C}{\beta} = \dfrac{V_{cc} - V_{sat}}{\beta R_C}$

V_i required to keep transistor in saturation?

$V_i = V_{DO} + R_B i_B > V_{DO} + R_B \dfrac{V_{cc} - V_{sat}}{\beta R_C} = V_{iH}$

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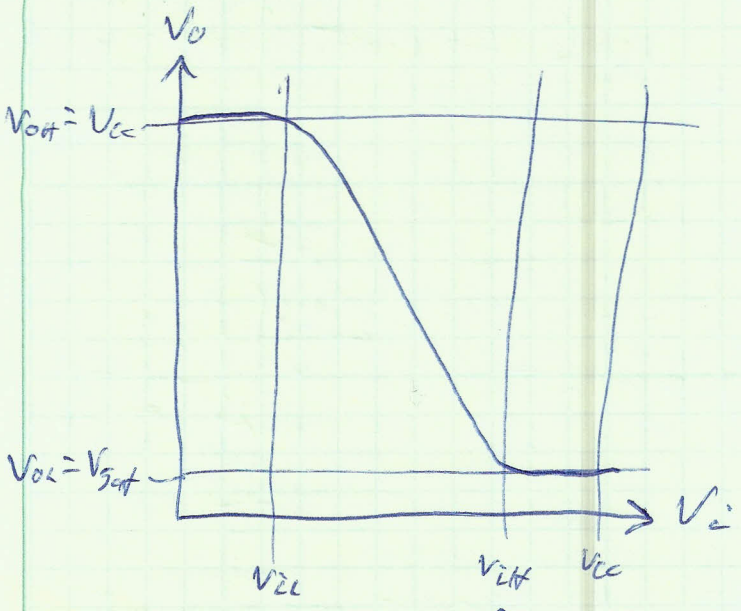
* choose R_B and R_C so that $V_{iH} < V_{cc}$



we can control this value with R_C, R_B

this value is fixed at $V_{DO} \approx 0.7v$

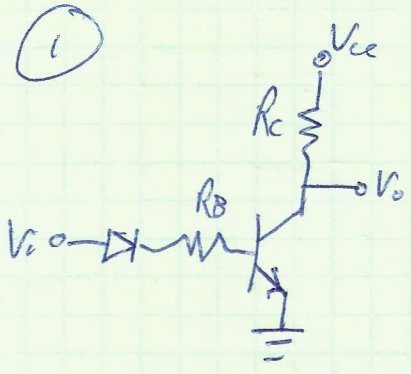
in reality, there will be some conduction at $V_i \approx 0.5v$

- Low side noise margin is only $V_{DO} - V_{sat} \approx 0.3$ to $0.5v$

Two solutions: $\quad V_i = R_B i_B + V_{BE}$

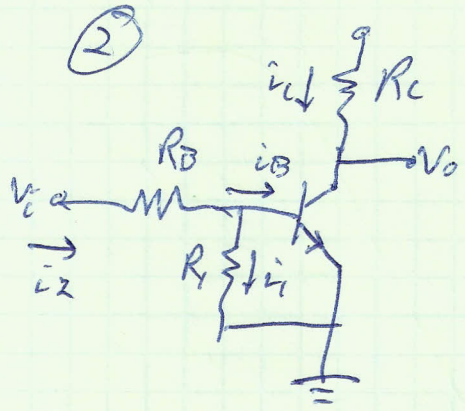
1. add series diode to allow large voltage drop for small current
2. add shunt resistor to allow current in R_B to be $> i_B$

(1)



- Increases V_{iL} to $2V_{DO}$ (and we can add more diodes if necessary)
- Only works well in ICs, where diodes and transistors are matched
- For discrete devices, I_S saturation current 2-3 orders of magnitude larger in diodes than transistors
  - only gives 0.2-0.3 v drop per diode

(2)



$$i_1 = \frac{V_{BE}}{R_1}$$

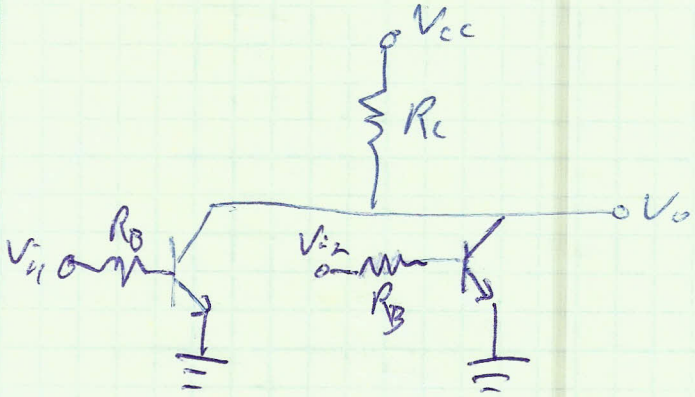
$$i_2 = i_B + i_1 \simeq i_1 = \frac{V_{BE}}{R_1}$$

$$V_{iL} = R_B i_2 + V_{BE} = V_{BE}\frac{R_B}{R_1} + V_{BE}$$

$$V_{iL} = V_{BE}\left(1 + \frac{R_B}{R_1}\right)$$

- for $R_1 = R_B$, we can increase V_{iL} from 0.7 to 1.4 V
- we can now determine V_{IL} and V_{IH} arbitrarily
- typically R_1 does not affect V_{IH}
  - i_B needed for saturation is several times higher than i_1

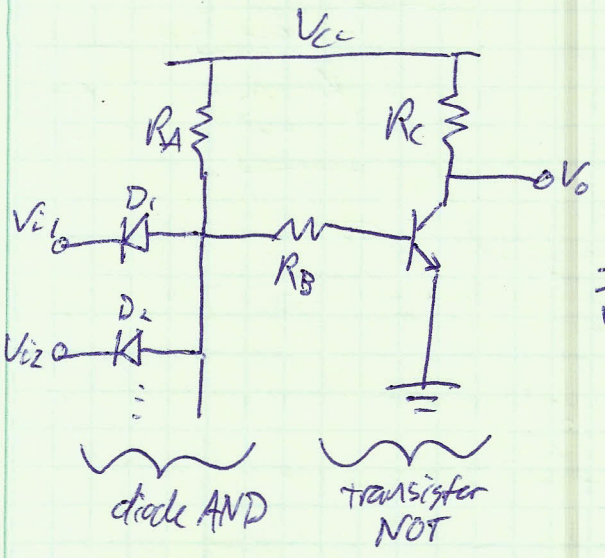
RTL NOR gate:



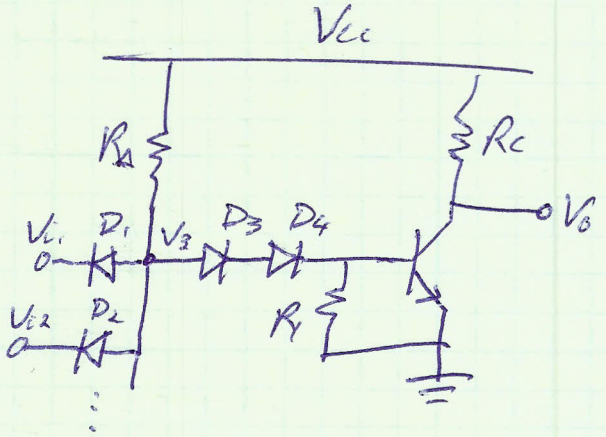
- RTL - first digital logic circuits using transistors
- replaced by diode-transistor logic DTL
  and transistor-transistor logic TTL
  or emitter-coupled logic ECL
- BJT logic is now rarely used because we have CMOS

Diode Transistor Logic (DTL) NAND gate

- constructed with Diode AND + transistor inverter



IC version

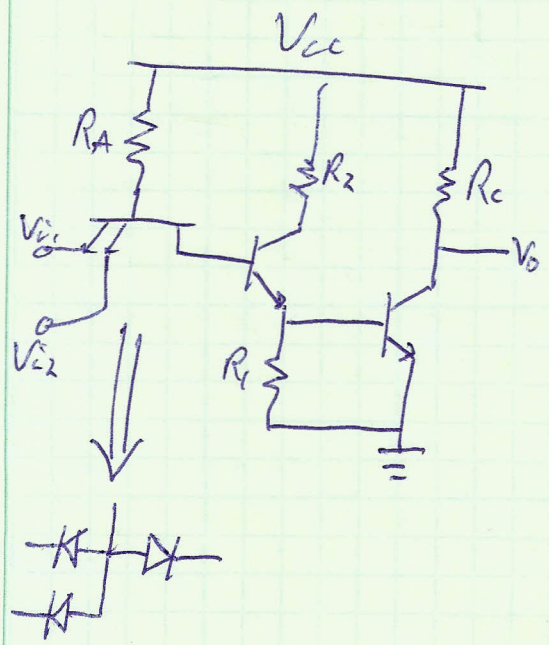


$V_{iH} = 2.1\,V$

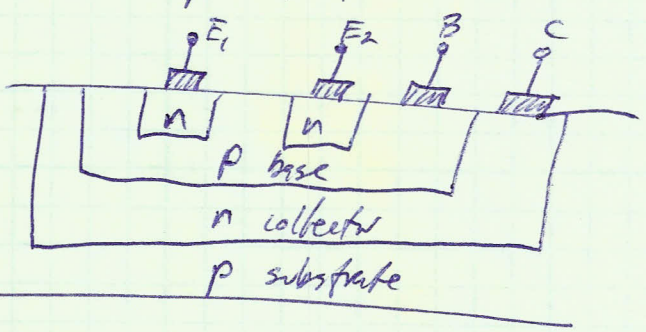
$V_{iL} = 1.4\,V$

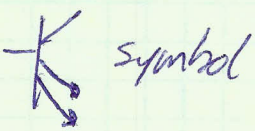
- R_1 is necessary to keep voltage across D_3 and D_4 at 0.7v otherwise current i_B will not be enough, and voltage across each of the junctions will be $\simeq V_3/3$
- Remember, there are 2 current paths - to input, and to output through R_A

Transistor-Transistor Logic (TTL)



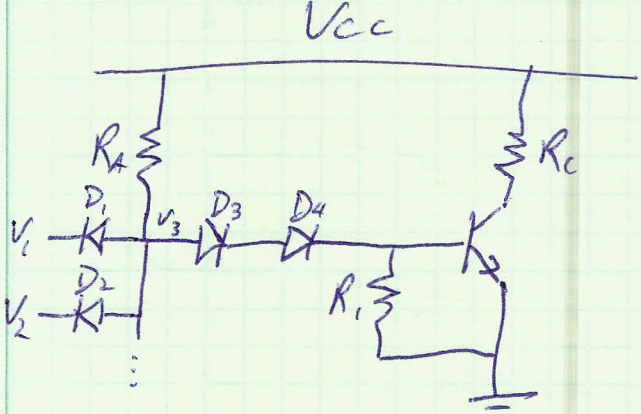
multiple-emitter transistor





Wrap-up of DTL from last lecture

DTL NAND gate



If V_1 or V_2 are low ($V_{sat} = 0.2v$) that diode is ON and V_3 will be 0.7 volts higher. D_3 and D_4 will be OFF. As both are raised to X, V_3 remains at X+0.7

The voltage V_3 required to switch the inverter is

$$V_3 = 0.7 + 0.7 + 0.7 = 2.1$$

(0.7 ↑ D_3, 0.7 ↑ D_4, 0.7 ↑ V_{BE})

So the gate will start to switch at $X + 0.7 = 2.1v$

or $\underline{X = 1.4v} \rightarrow \underline{V_{iL} = 1.4v}$

Solving for V_{iH} takes longer

- determine the edge of saturation for the transistor
- assume saturation, find i_C and i_B
- determine what input voltage gives $i_B > \frac{i_C}{\beta}$
- must consider currents going out through gate input and through resistor R_1