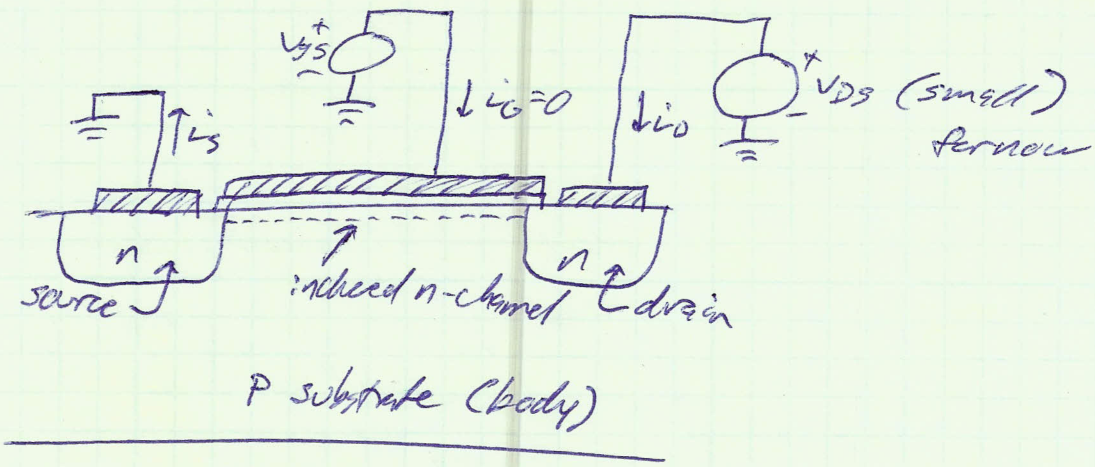
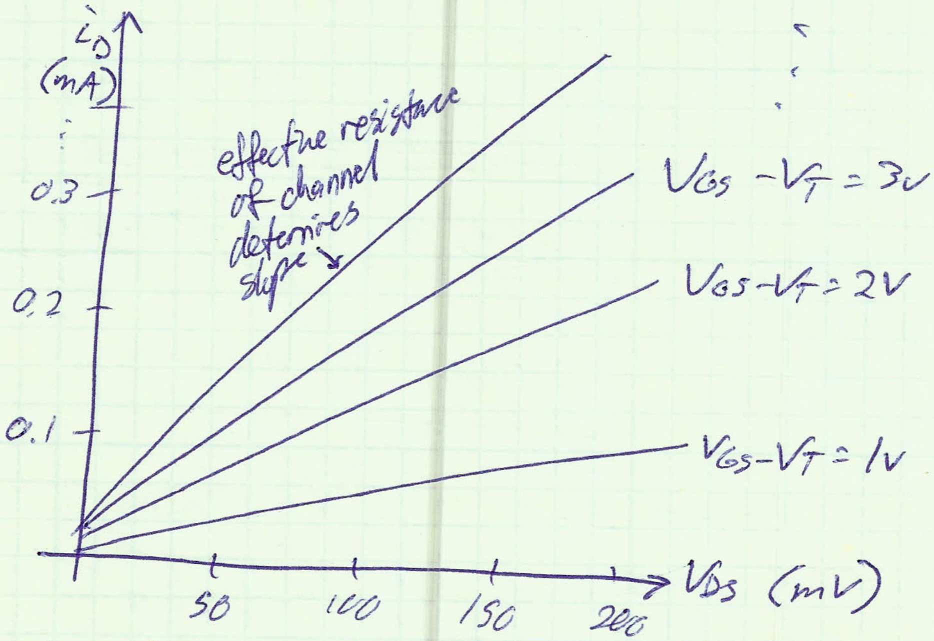
Field Effect Transistors (FETs)

MOSFET = Metal Oxide Semiconductor Field Effect Transistor



- Two n regions deposited within p type substrate
- Gate applied between them, seperated by thin oxide layer (one of the reasons Si is important – forms high quality oxide)
- When voltage is applied to Gate, thin region under gate is depleted
- With higher voltage, thin inversion layer forms – behaves as n-type
  - forms conductive channel between source and drain
  - thickness depends on V_{GS} – proportional to $V_{GS} - V_T$
    threshold voltage
- This is called enhancement type NMOS
  - there is also depletion type
  - there is also PMOS

For $V_{GS} > V_T$ (so that channel is formed)
apply positive voltage to V_{DS}
acts as resistor – value depends on geometry of channel

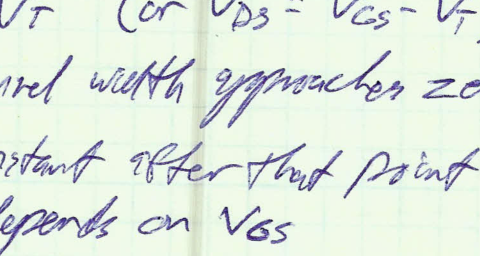


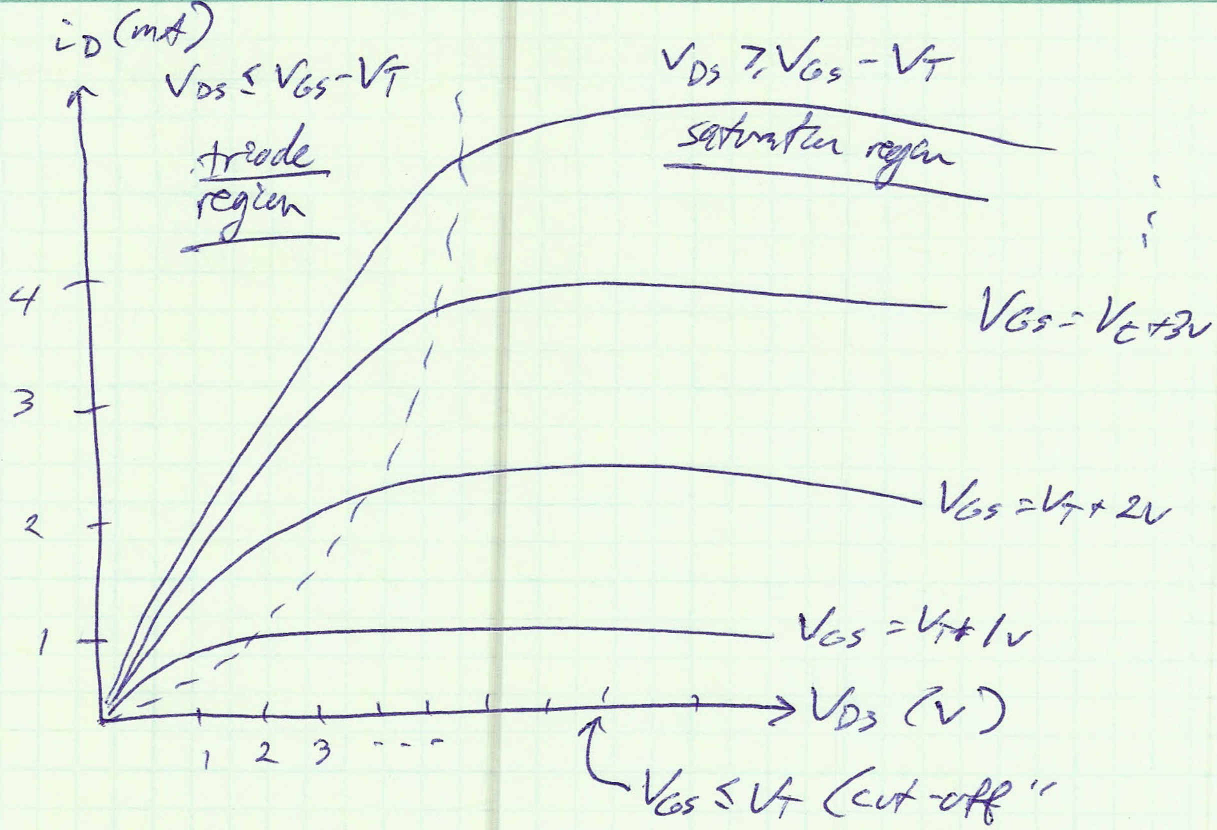
Conductivity increases as $V_{GS} - V_T$ increases

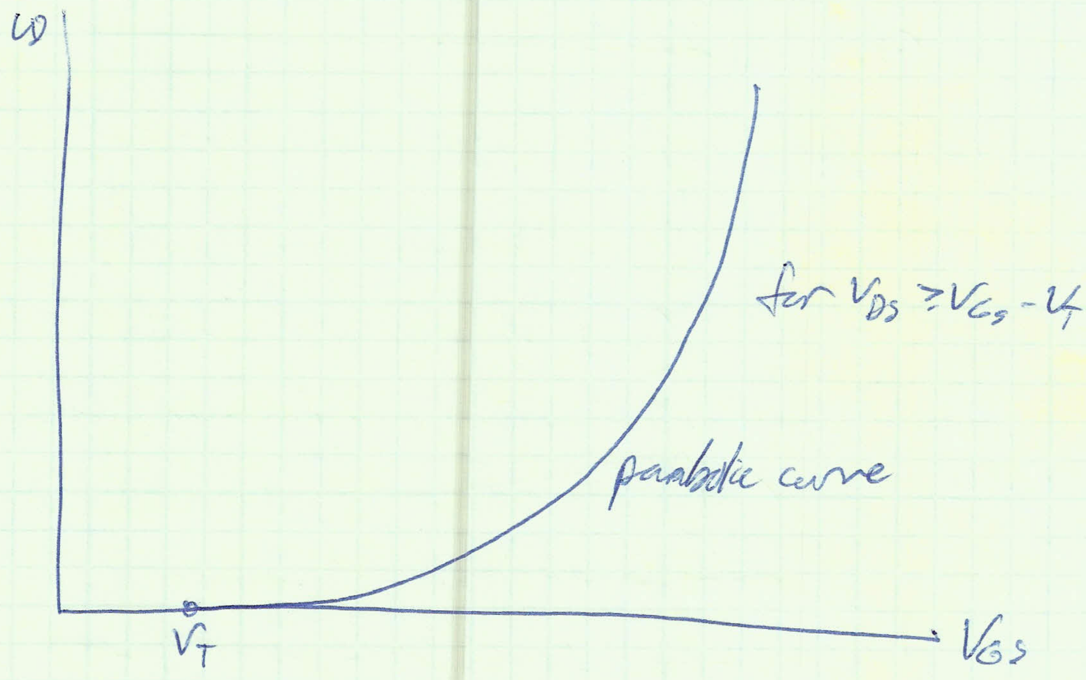
- Now apply larger Drain voltage

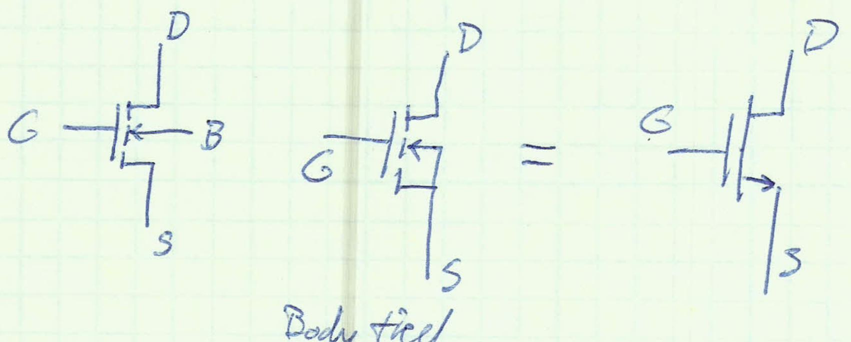
$$V_{GD} = V_{GS} - V_{DS} \ (< V_{GS})$$

- channel near drain is smaller than near source
- when $V_{GD} = V_T$ (or $V_{DS} = V_{GS} - V_T$)
  the channel width approaches zero ("pinch-off")
- Current is constant after that point
  – i_D only depends on V_{GS}
- There is a small effect "channel width modulation"
  similar to Early effect in BJTs

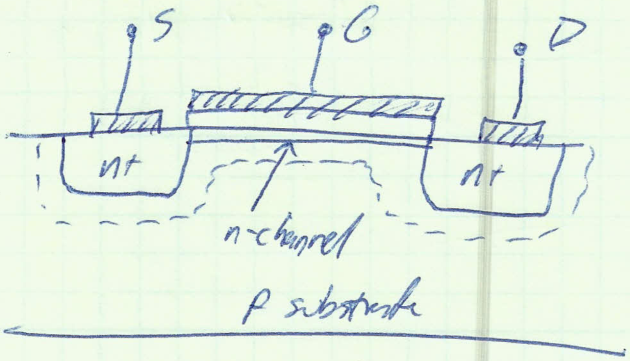








Body tied to source



inversion layer (channel) starts to form at $V_{GS} = V_T$

charge in channel $|Q| = \underbrace{C_{ox}}_{\text{capacitance per area}} \underbrace{WL}_{\text{area}} (V_{GS} - V_T)$

capacitance is typically ~fF

Q per unit length

$$= \frac{|Q|}{L} = C_{ox} W (V_{GS} - V_T)$$

electric field $|E| = \frac{V_{DS}}{L}$

electron drift velocity $= \mu_n |E| = \mu_n \frac{V_{DS}}{L}$

current i_D = charge per unit length × drift velocity

$$i_D = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T) \cdot V_{DS}$$

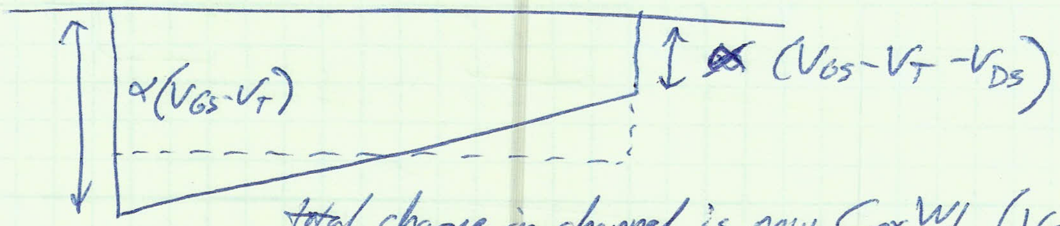
some books use $k_n = \mu_n C_{ox} \frac{W}{L}$

conductance of channel $g_{DS} = \frac{i_D}{V_{DS}} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)$

we call $\mu_n C_{ox}$ the process transconductance parameter $k_n' = \mu_n C_{ox}$

resistance of channel $r_{DS} = \frac{1}{g_{DS}} = \frac{1}{k_n' \frac{W}{L} (V_{GS} - V_T)}$

Now apply larger V_{DS}:

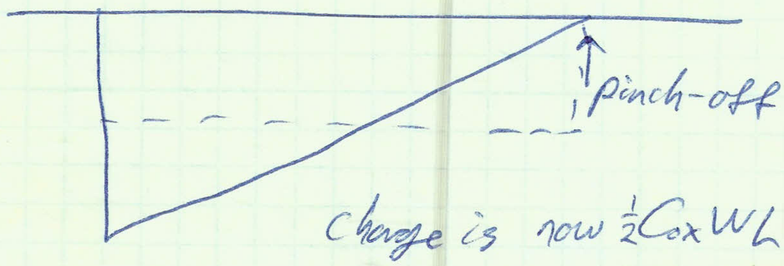


total charge in channel is now $C_{ox} W L \left(V_{GS} - V_T - \frac{1}{2} V_{DS}\right)$

current $\quad i_D = k' \frac{W}{L}\left(V_{GS} - V_T - \frac{1}{2} V_{DS}\right) V_{DS}$

$$i_D = k' \frac{W}{L}\left((V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2\right)$$

when $V_{DS} > V_{GS} - V_T$:



Charge is now $\frac{1}{2} C_{ox} W L\, V_{GS}$

$$i_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_T)^2$$

MOSFET Large Signal Model (NMOS)

Cut-off: $V_{GS} < V_T$, $i_D = 0$

Triode : $V_{GS} > V_T$, $V_{DS} < V_{GS} - V_T$, $i_D = \frac{1}{2} k_n' \frac{W}{L}\left[2V_{DS}(V_{GS}-V_T) - V_{DS}^2\right]$

Saturation : $V_{GS} > V_T$, $V_{DS} > V_{GS} - V_T$, $i_D = \frac{1}{2} k_n' \frac{W}{L}(V_{GS}-V_T)^2(1+\lambda V_{DS})$

- $k_n' = \mu_n C_{ox}$
- λ is for channel length modulation effect
  sometimes quoted as $V_A = 1/\lambda$, similar to Early effect
- some books use $k_n = \mu_n C_{ox} \frac{W}{L}$ or $K_n = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}$
- we use k_n', consistent with Sedra + Smith
- in triode region, behaves as variable resistor

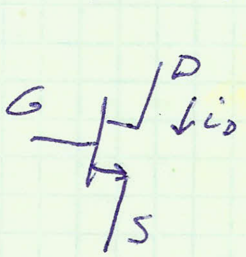
$$r_{DS} = \frac{V_{DS}}{i_D} \simeq \frac{1}{k_n' \frac{W}{L}(V_{GS}-V_T)}$$

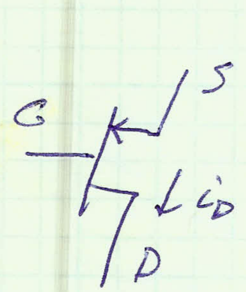
- For PMOS, everything is the same, but reverse all voltages

$V_{GS} \rightarrow V_{SG}$, $V_{DS} \rightarrow V_{SD}$, $V_{Tn} \rightarrow |V_{Tp}|$

(note V_{Tp} is negative)

NMOS PMOS





Important points:

- no current flows into gate - $i_G = 0$
- in cut-off, $i_D = 0$ (however $i_D = 0$ does not mean cutoff, it could just be because $V_{DS} = 0$)
- Saturation mode - called because i_D is saturated
  - equivalent to BJT active mode
- behavior of BJTs + FETs are similar
  - both are off when input is below threshold (V_{D0} or V_T)
  - BJT requires i_B to work, FET has $i_G = 0$

Recipe for solving MOSFET circuits

1) write down GS-KVL and DS-KVL
2) from GS-KVL, calculate V_{GS}
   - if $V_{GS} < V_T \rightarrow$ cutoff, $i_D = 0$, solve for V_{DS} with DS-KVL → Done
   - if $V_{GS} > V_T \rightarrow$ not cutoff
3) assume saturation
   - calculate i_D from device equation for saturation
   - find V_{DS} from DS-KVL, if $V_{DS} > V_{GS} - V_T \rightarrow$ Done
4) if $V_{DS} < V_{GS} - V_T$, in triode mode
   - ~~calculate i_D from triode equation~~
   - ~~find V_{DS}~~
   - substitute i_D from triode equation into DS-KVL
   - calculate V_{DS} (one of two roots will be unphysical)
   - check that $V_{DS} < V_{GS} - V_T$
   - substitute V_{DS} in DS-KVL to find i_D

★ Check examples in notes page 3-25