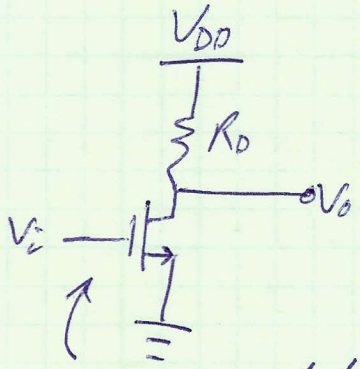
MOSFET Inverters and Switches

NMOS inverter

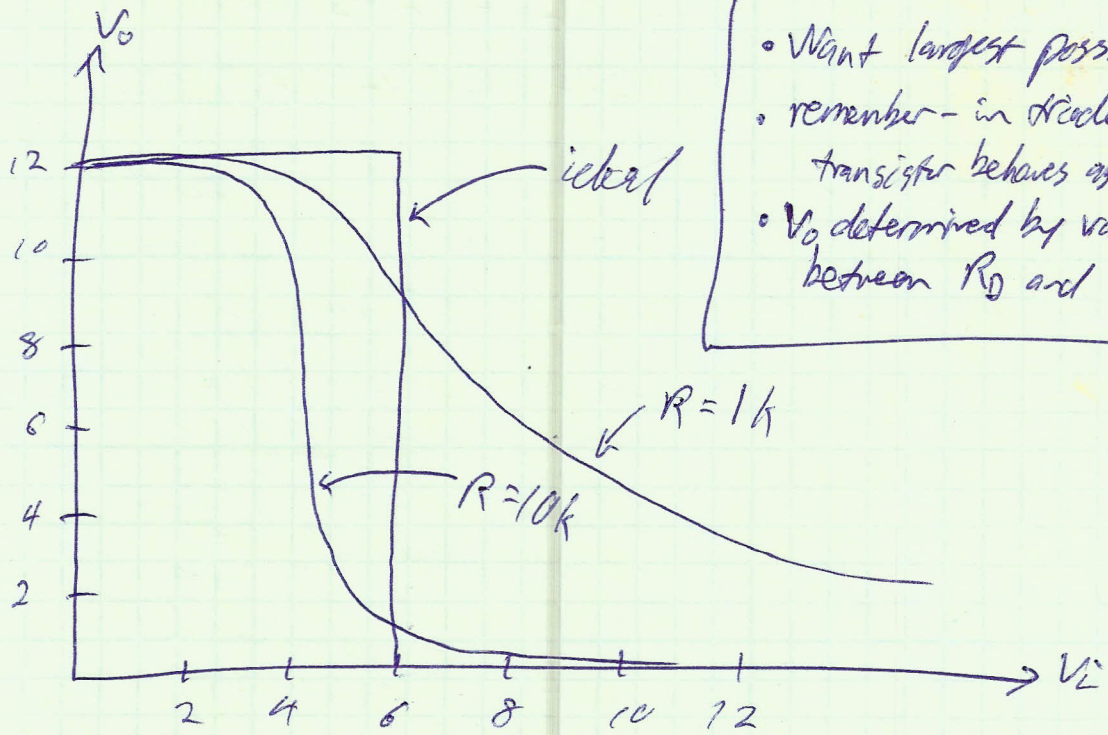


no resistor needed

this is a voltage controlled device

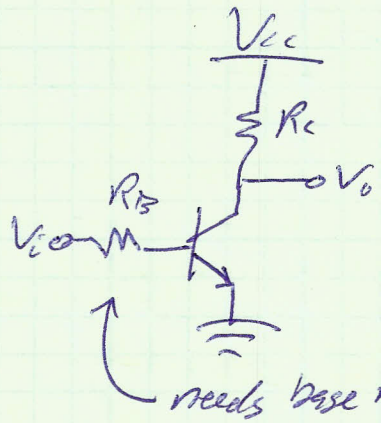
when V_{in} is high, v_o can be anywhere between 0 and $V_{GS} - V_t$ (it's in triode mode)

- V_o is determined by value of R_D



- Want largest possible R_D
- remember - in triode mode, transistor behaves as variable resistor
- V_o determined by voltage divider between R_D and r_{DS} of transistor

BJT inverter

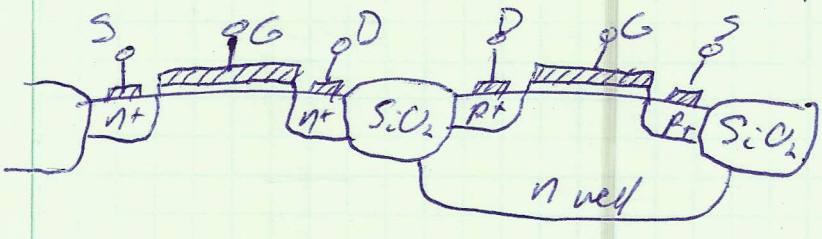


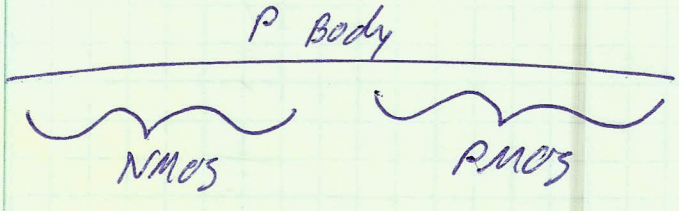
needs base resistor to convert input voltage into current and keep $V_{BE} \simeq V_{D0}$

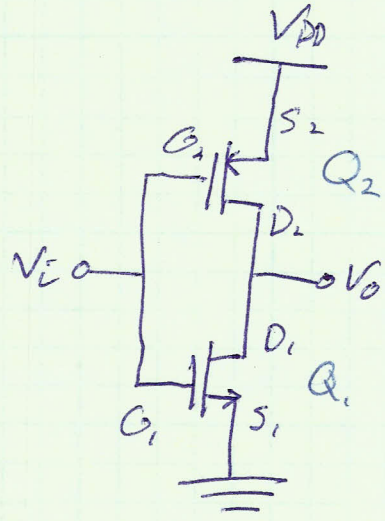
when V_i is high, $V_o = V_{CE} = V_{sat} \simeq 0.2V$

Complimentary MOS (CMOS)

Combine NMOS + PMOS on same chip







Both transistors are designed to have same threshold voltage

$V_{tn} = V_t = |V_{tp}|$

- $V_{GS1} = V_i$, $V_{SG2} = V_{DD} - V_i$, $V_o = V_{DS1} = V_{DD} - V_{SD2}$, $i_{D1} = i_{D2}$

for $V_i = 0$

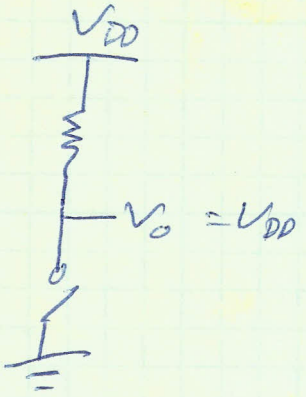
$V_{GS1} = 0 < V_t \rightarrow$ NMOS in cut-off, $i_{D1} = 0$

$V_{SG2} = V_{DD} > V_t \rightarrow$ PMOS is ON, but $i_{D2} = i_{D1} = 0$

Q_2 is in triode mode – acts as resistor

but $i_{D2} = 0 \rightarrow V_{SD2} = 0$

so $V_o = V_{DD}$

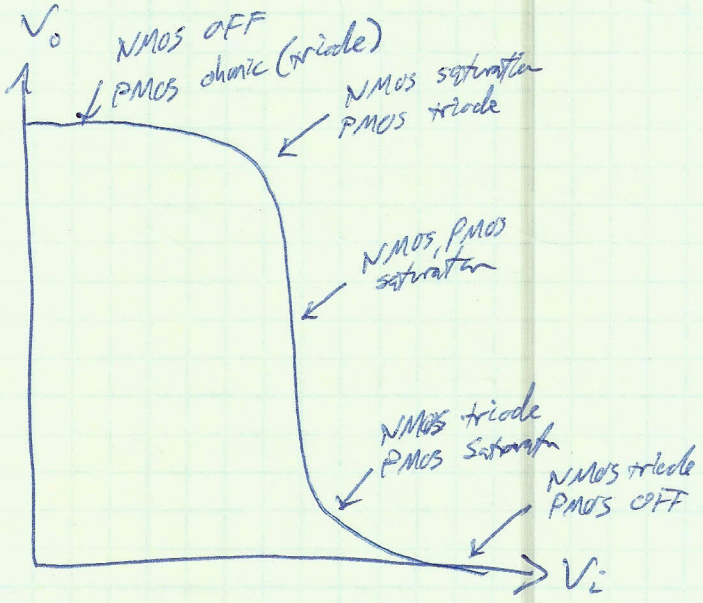


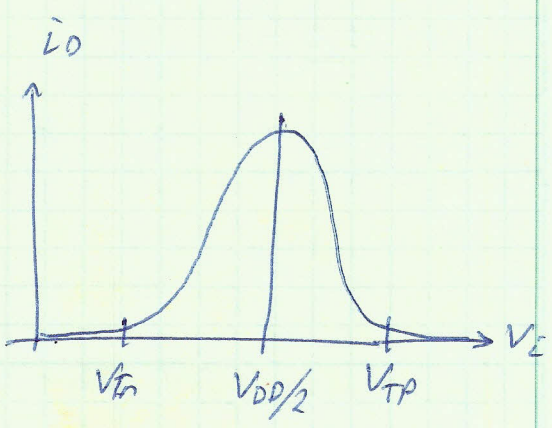
similarly, when $V_i = V_{DD}$, $V_o = 0$

This circuit functions as an inverter

Advantages of CMOS

- No resistors needed - less power consumed, and can be smaller
- ON and OFF levels are all the way at supply and ground
- No current flow in either state (but there is switching current)

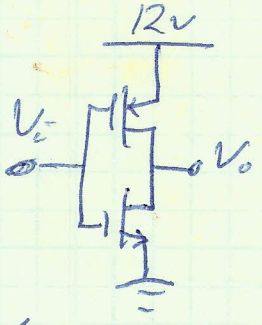




Maximum Current Flow

$$k_n' \frac{W}{L} = k_p' \frac{W}{L} = 0.5 mA/V^2$$

$$V_{DD} = 12V, \quad V_T = 2V$$



when $V_i = 6V$

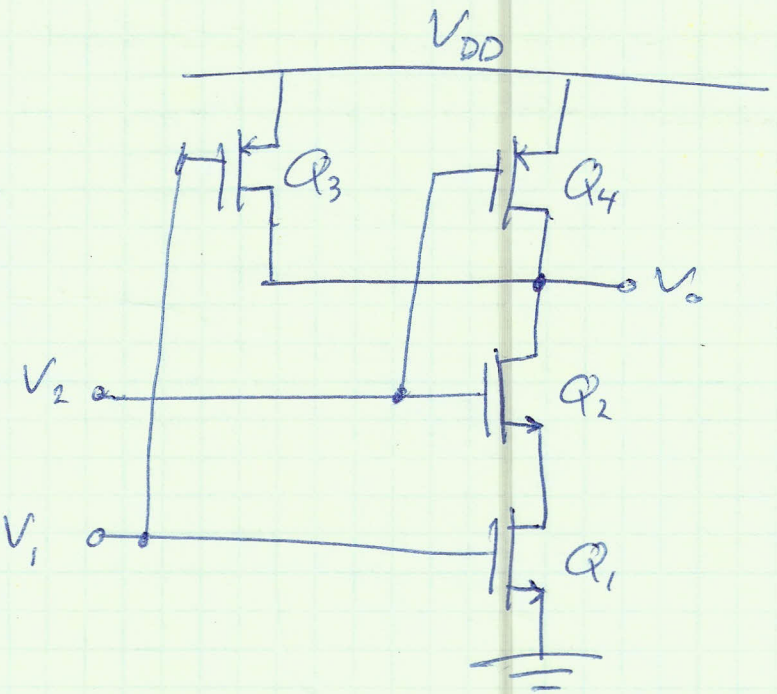
NMOS: $V_{GS} - V_T = 4V \rightarrow ON$
PMOS: $V_{SG} - |V_T| = 4V \rightarrow ON$
} assume saturation

$$i_{D1} = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_T)^2 = 4mA$$

by symmetry, $V_o = 6V$

$V_{DS} > V_{GS} - V_T \rightarrow$ saturation ✓

CMOS NAND gate



Procedure to solve CMOS gates

1) for a set of voltages V_i find V_{GS} for all transistors
   determine which are ON or OFF
2) Set $i_D = 0$ for all transistors that are OFF
   use KCL to find i_D for other transistors
3) look for transistors that are ON but with $i_D = 0$
   these are in triode mode with $V_{DS} = 0$
4) Use KVL to find V_o based on V_{DS}

For $V_1 = V_2 = 0V$

$V_{GS1} = 0 < V_T \rightarrow Q_1$ is OFF $\rightarrow i_{D1} = 0$

current through all transistors is 0

$V_{SG3} = V_{DD} > |V_T|$
$V_{SG4} = V_{DD} > |V_T|$
} Q_3 and Q_4 ON but with $i_D = 0$

Q_3 and Q_4 in triode region, with $V_{SD} = 0$

$\rightarrow V_o = V_{DD}$

For $V_1 = V_2 = V_{DD}$

$V_{SG3} = V_{SG4} = 0 < |V_T| \rightarrow Q_3$ and Q_4 OFF $\rightarrow i_D = 0$

Q_1 and Q_2 ON, but with $i_D = 0 \rightarrow V_{GS} = 0$ (triode)

$\rightarrow V_o = 0$

For $V_1 = 0$, $V_2 = V_{DD}$

Q_1 is OFF and Q_3 is ON
Q_2 is ON and Q_4 is OFF
The lower path (Q_1 and Q_2) is OFF
The upper path (Q_3 or Q_4) is ON

$V_o = V_{DD}$

V_2 \ V_1	0	1
0	1	1
1	1	0

NAND

Review:

BJT:

current-controlled device

cutoff: $V_{BE} < V_{D0} \rightarrow i_C = 0$

active: $V_{BE} = V_{D0}$, $i_C = \beta i_B$

saturation: $V_{CE} < V_{D0} \rightarrow V_{CE} = V_{sat} (\approx 0.2V)$, $i_C < \beta i_B$

PNP works the same way, but all voltages, currents are reversed

FET:

voltage controlled device

cutoff: $V_{GS} < V_T \rightarrow i_D = 0$

saturation: $V_{DS} > V_{GS} - V_T \rightarrow i_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$

triode: $V_{DS} < V_{GS} - V_T \rightarrow i_D = \frac{1}{2} k_n' \frac{W}{L} \left[2(V_{GS} - V_T) \underset{V_{DS}}{\wedge} - V_{DS}^2 \right]$

PMOS works the same way, but all voltages, currents are reversed