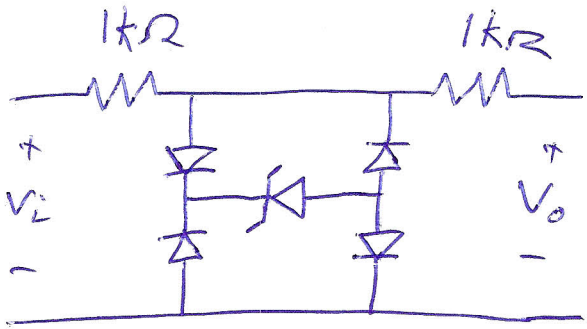
ECE 65 Final Exam Spring 2012

Question #1:

For the circuit shown, the Zener diode has V_Z=5 V. All others are standard silicon diodes

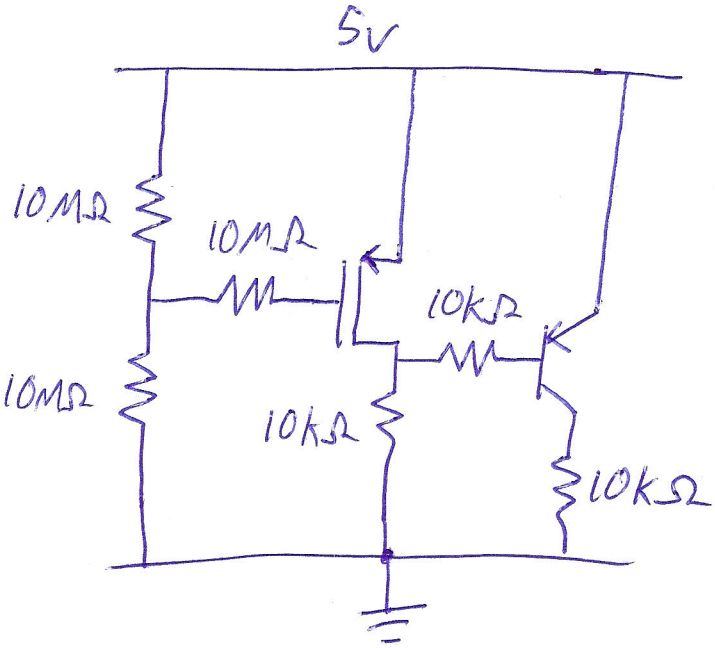
a) Write the transfer function, V_o for all V_i.
b) Plot the transfer function
c) For an input sine wave with 10 V amplitude, sketch the output signal.



Question #2:

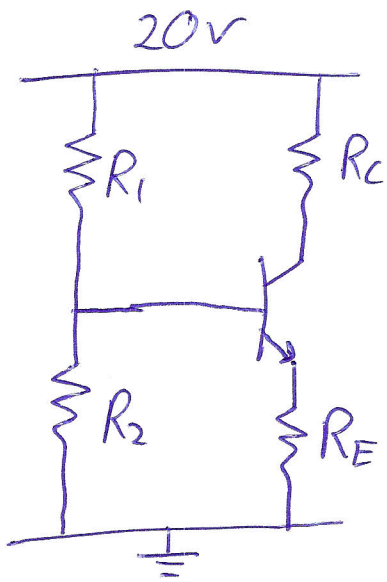
For the circuit shown, assume V_{Tp}=-1V and $\mu_p C_{ox}(W/L)$=1 mA/V^2 for the FET, and β=100 for the BJT. Neglect the Early effect and the channel length modulation effect.

a) Identify the state of the FET
b) Find the value of the drain current I_D
c) Identify the state of the BJT
d) Find the value of the collector current I_C



Question #3:

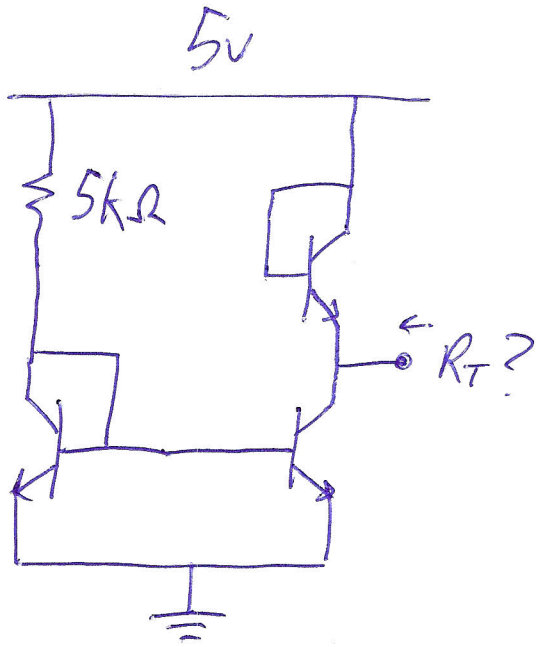
Assume you have an NPN BJT with β=100, and a voltage source of 20 V. Design a bias circuit to provide V_{CE}=10 V, and I_C=2 mA. The bias circuit should be stable with respect to variations in β ranging from 50 to 200, and variations in V_{BE} of 0.1 V. Provide values for all resistors shown.



Question #4:

For the circuit shown, assume that $\beta=100$, *and* $V_A=100$ V. Assume ideality factor n=1.

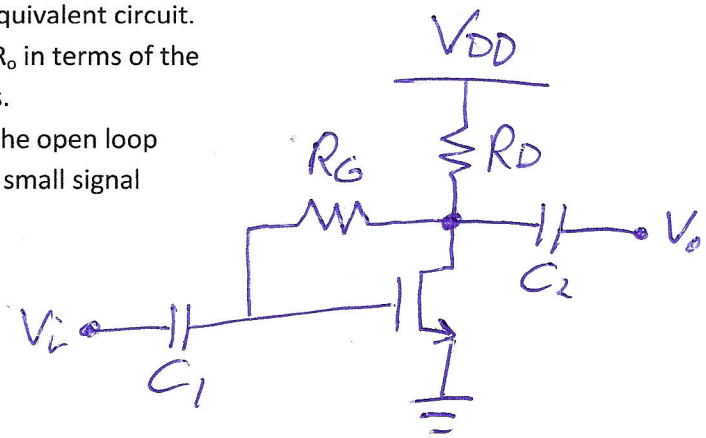
a) Determine g_m, r_π, and r_o for each transistor.
b) Draw the small-signal equivalent circuit.
c) Determine the Thevenin resistance at the node shown.



Question #5:

For the amplifier shown,

a) Draw the small signal equivalent circuit.
b) Find an expression for R_o in terms of the small signal parameters.
c) Find an expression for the open loop gain A_{V0} in terms of the small signal parameters.



Question #6:

For the amplifier shown, assume $\beta=100$ and VA=100 V. Assume ideality factor n=1.

a) Calculate A_{V0}, R_i, and R_o.
b) Calculate the low-frequency cut-off.