ADVANCED FUNCTIONAL MATERIALS

Supporting Information

for *Adv. Funct. Mater.*, DOI: 10.1002/adfm.201400105

Novel Heterogeneous Integration Technology of III–V Layers and InGaAs FinFETs to Silicon

*Xing Dai, Binh-Minh Nguyen, Yoontae Hwang, Cesare Soci, and Shadi A. Dayeh**

Supporting Information

Novel Heterogeneous Integration Technology of III-V Layers and InGaAs FinFETs to Silicon

Xing Dai, Binh-Minh Nguyen, Yoontae Hwang, Cesare Soci, and Shadi A. Dayeh[*]

Extensive studies of atomic layer deposition (ALD) of HfO_2 on Si, InAs and InGaAs/InP, were carried out through the optimization of deposition temperature, growth precursor pulse time (H_2O and Tetrakis(dimethylamino)hafnium (TDMAH)), *ex-situ* chemical and *in-situ* plasma treatment methods. The H_2O source temperature was kept at 20 °C while that of the TDMAH source at 75 °C during all the deposition. The top contacts were patterned by photolithography and deposited with Ni, while planer Al was utilized for bottom contacts on highly-doped p-type Si and planer Ni for InAs. **Figure S1** depicts the trend of leakage current density through 15 nm HfO_2 on Si treated by HF and rinsed in deionized water right before loading into the ALD chamber. The leakage current decreases with increasing deposition temperature from 185 °C to 200 °C. Less reduction is observed between 200 °C and 250 °C, while the leakage dramatically increases when the temperature approaches 300 °C. As a result, further optimizations were based on the deposition temperatures of 200 °C and 250 °C.

[*] Author to whom correspondence should be addressed, E-mail: sdayeh@ece.ucsd.edu

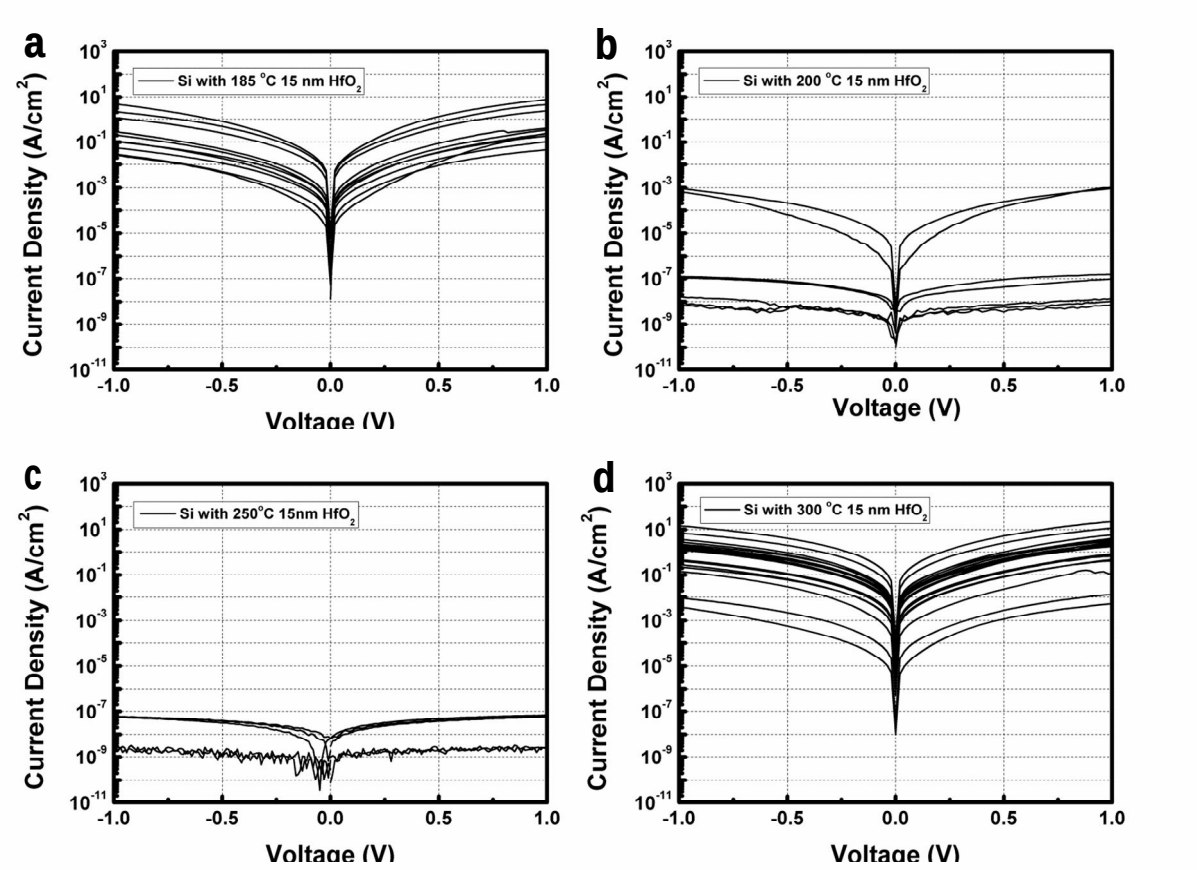
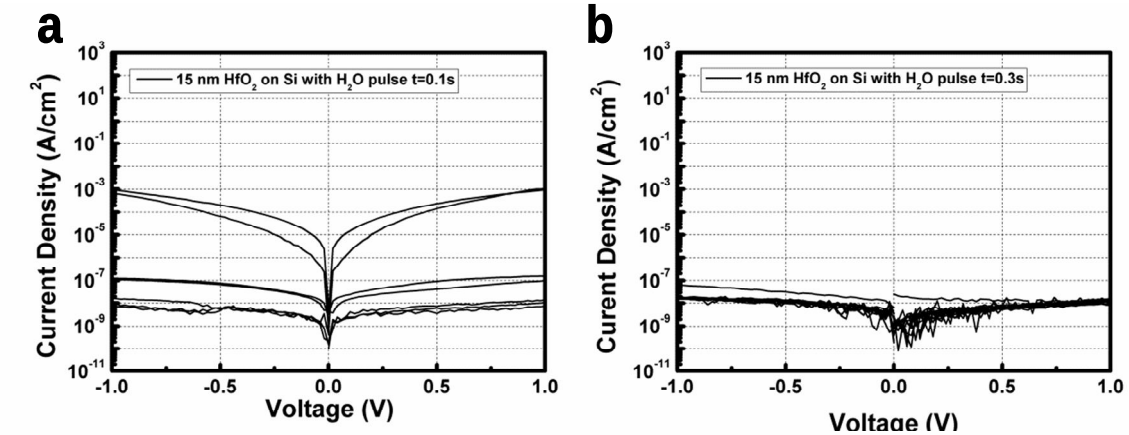


Figure S1. Leakage current density through ALD HfO_2 on Si substrate decreases with deposition temperature rises from 185 °C (a) to 200 °C (b) and stays almost unchanged when it further increases to 250 °C (c). When the temperature reaches 300 °C (d), the leakage current density increases dramatically to 1 A/cm^2 range.

With the fixed temperature of 200 °C and H_2O purge time of 40 s, the pulse time of H_2O was investigated and illustrated in **Figure S2**. The leakage current density first reduces and then increases with increasing pulse time. Consequently, the optimal condition with the minimum leakage current is achieved with 0.3 s H_2O pulse time.



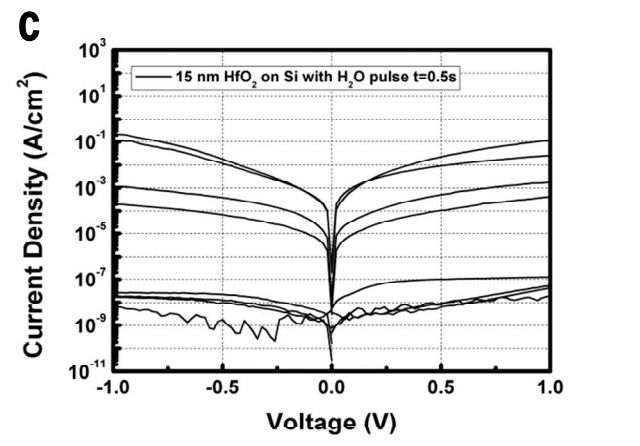


Figure S2. Studies of the impact of H_2O pulse time (a) 0.1 s, (b) 0.3 s, and (c) 0.5 s, on leakage current through 15 nm ALD HfO_2 on Si substrate showing the optimal time of 0.3 s (b) with the purge time of 40 s at 200 °C.

Investigations of the HfO_2 were mostly performed on a Si substrate to adjust the basic insulating properties of the HfO_2 layer on the less challenging Si surface prior to optimizing the HfO_2/III-V interface. The III-V/high-k interface is critical for the FET characteristics and performance. Normally, Al_2O_3 is used as the sole high-k dielectric in III-V transistors or as an intermediate layer between higher-k dielectric and the III-V material, which could effectively improve the interface quality.[1] In the case of our HfO_2 gate dielectric, ex-situ surface preparation methods, including diluted HF only, O_2 plasma and diluted BOE, HCl only, HCl and $(NH_4)_2S$, and diluted BOE and $(NH_4)_2S$, have been studied but were not sufficient to display an obvious suppression of the leakage current on an InAs(100) surface. Alternatively, we investigated the in-situ treatment inside the ALD chamber. The InAs samples were treated with diluted BOE, deionized water and 10% $(NH_4)_2S$, and were then immediately loaded into the ALD chamber with the temperature held at 200 °C. 5 cycles of alternating TMA (stabilized at 20 °C with pulse/purge time of 0.4/5 s) and H_2 plasma (10 s H_2 gas stabilization time before 2 s 'plasma-on' time at 100 W ICP power, followed by 5 s purge time) were performed inside the ALD chamber prior to the HfO_2 growth.[2] The comparison between with and without this in-situ treatment on InAs substrate is illustrated in **Figure S3**. Ex-situ studies were repeated and combined with this in-situ treatment, while the recipe of diluted BOE,

deionized water, 10 min 10% $(NH_4)_2S$, and deionized water provided the best suppression of leakage current.

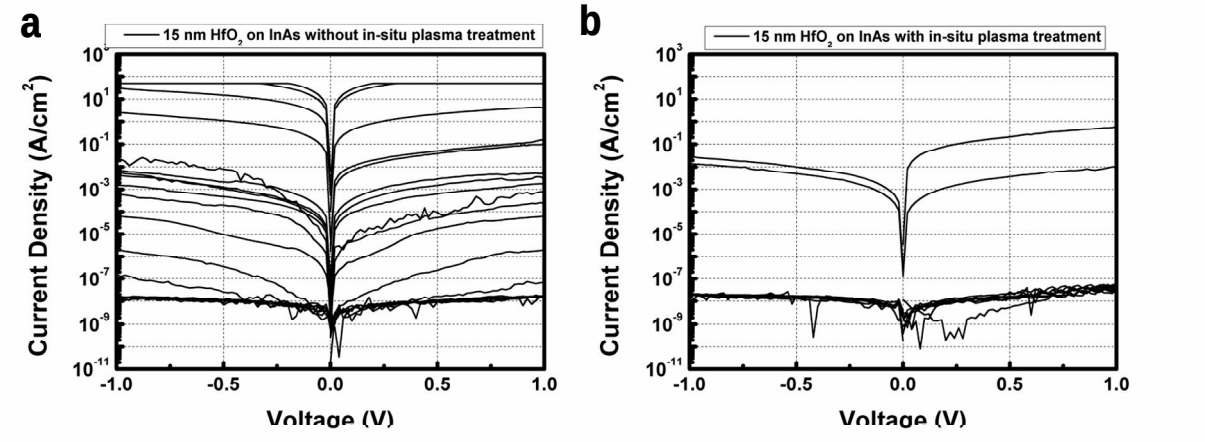


Figure S3. Suppression of leakage current through 15 nm HfO_2 on InAs after 5 cycles alternating TMA and H_2 plasma in-situ treatment in (b) compared with samples without this in-situ treatment in (a).

Utilizing the best ex-situ, in-situ surface treatment methods and the best H_2O pulse time, further investigation was carried out in terms of HfO_2 ALD deposition temperature on InAs(100) surface. Studies of C-V characteristics on the InAs sample were based on two temperatures of 200 ° C and 250 ° C, which were established to show lower leakage current densities on Si surfaces as shown in Figure S1. For ALD HfO_2 on InAs at 200 °C, almost no modulation of the carriers was observed as shown in **Figure S4a**. For ALD HfO_2 on InAs at 250 °C, typical C-V curves showing accumulation, depletion and inversion regimes of the MIS capacitor, were observed in **Figure S4b**. The relative dielectric constant could be calculated based on $C_{acc} = C_{ox} = \varepsilon_{ox}/t_{ox}$. From Figure S4b, we obtain:

$$\varepsilon_r\left(HfO_2\right) = C_{acc} \times t_{HfO_2} / \varepsilon_0 = \left(1.03\times10^{-6} F/cm^2 \times 15\times10^{-7} cm\right) / \left(8.854\times10^{-14} F/cm\right) \approx 17.5 F/cm$$

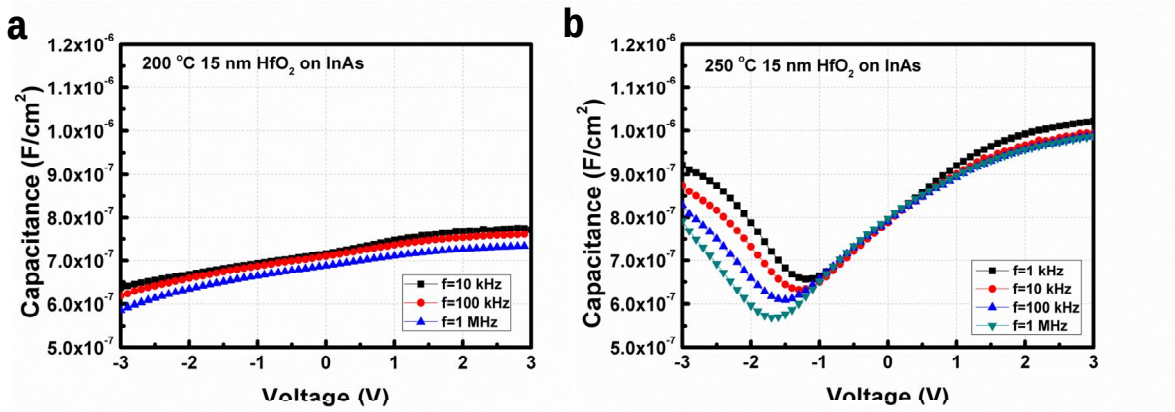


Figure S4. C-V characterization of 15 nm HfO_2 on InAs grown at different temperatures of 200 °C (a) and 250 °C (b), in which (b) shows a reasonable C-V curve indicating clear carrier accumulation, depletion and inversion regions.

The pulse time of TDMAH was studied with a fixed purge time of 15 s, deposition temperature of 250 °C, H_2O pulse/purge time of 0.3/40 s, and best ex-situ and in-situ plasma treatments determined from the studies on HfO_2/InAs interfaces discussed above. In our system, the injection of TDMAH is controlled by a booster function, which includes 0.8 s for pre-empty time and 1.2 s for master fill time for the case of total pulse time of 1.9 s (this is the original pulse time in the recipe, which was used for all the studies mentioned above). The actual TDMAH pulse time is approximately 0.1~0.3 s. As we decreased the pulse time, we simultaneously decreased the time of all other steps in the booster function. **Figure S5** exhibits the C-V characteristics of various TDMAH pulse time, where **Figure S5c** shows the best C-V characteristics with least dispersion in the accumulation regime and the highest normalized capacitance indicating highest high-k dielectric constant than those in **Figure S5a-b**.

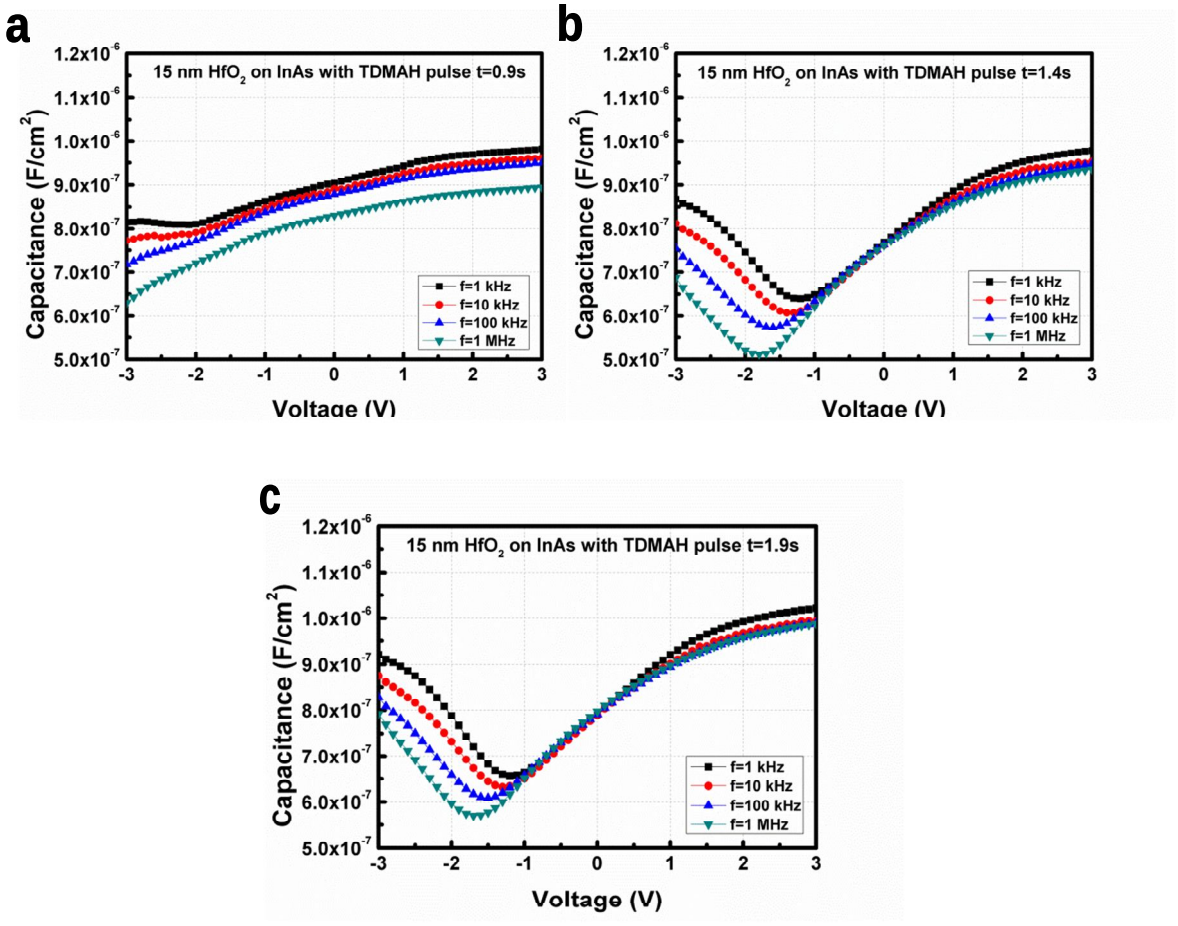


Figure S5. C-V characteristics for different TDMAH pulse times. (a) 0.9 s (b) 1.4 s, and (c) 1.9 s. Better C-V characteristics or HfO_2/InAs interfaces were obtained at higher TDMAH pulses slightly improved dielectric constant for 1.9 s pulse time.

The optimal HfO_2 deposition condition is slightly different on the InGaAs substrate compared with that on the InAs substrate. 50 nm undoped InGaAs is grown on semi-insulating (SI) InP(100) (grown by Intelligent epitaxy), concentric circle patterns were employed in the C-V measurements. Considering the compatibility in InGaAs FinFET gate last process, we have to avoid the formation of Ni-InGaAs alloy starting at 250 °C because pre-gate treatment in BOE will remove (etch away) the alloyed extension. In consequence, a 5 nm thick HfO_2 layer on InGaAs at 200 ° C with all the other optimized criteria was deposited and characterized, and the results are shown in **Figure S6**. The entire accumulation regime was not observed due to the lower voltage sweep range from -1 V to 1 V compared to those

used for InAs above, but a distinctive depletion regime was clearly obtained and these deposition parameters were then adopted in our FinFET fabrication process.

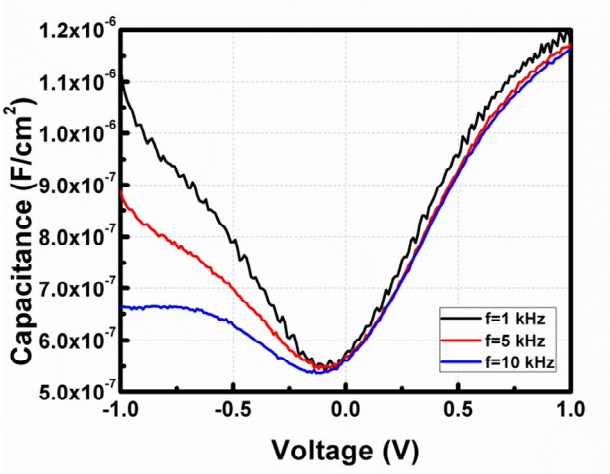


Figure S6. C-V curve of 5 nm HfO_2 deposited at 200 °C on undoped InGaAs on SI InP.

Furthermore, SS^{-1} and DIBL dependence on the thickness of HfO_2 on FinFET devices with a fixed perimeter of 60 nm was investigated. **Figure S7** summarizes the improved characteristics with thinner HfO_2 of 5 nm compared to those with thicker 7.5 nm HfO_2. This demonstrated that better SS^{-1} resulted from enhanced gate control by increasing the gate insulator capacitance. The DIBL in the devices with L_{ch} of 490 nm could be reduced from 340 mV/V to 8 mV/V as exhibited in **Figure S7b**. This comparison predicts that even lower EOT than that used here, perhaps by applying either higher-k material or smaller thickness, could help further scaling of the device channel length with better immunity to short channel effects.

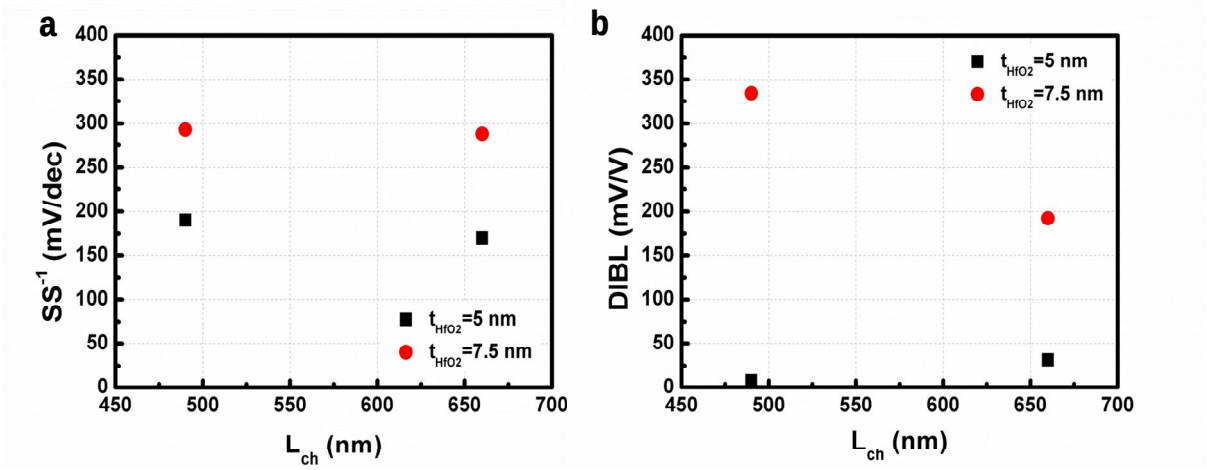


Figure S7. Comparison of SS^{-1} (a) and DIBL (b) vs L_{ch} for devices with 5 nm and 7.5 nm HfO_2.

To elucidate the origin of the SS^{-1} and transconductance degradation with increasing Fin perimeter and at fixed gate length of 450 nm, 3D Silvaco-Atlas simulations were conducted on a set of FinFETs on insulator with perimeters of 85, 100, 130, and 150 nm and a Fin height of 35 nm. An InGaAs Fin channel with n-type doping concentration of 10^{15} cm^{-3} and a positive fixed charge density of 10^{12} cm^{-2} at the InGaAs/HfO_2 interface. The HfO_2 thicknes of consideration was 5 nm. Fig. S8 shows contour plots of electron concentration taken from a cross-sectional cut at the center of the FinFET gate with V_{DS}=0.5 V and V_{GS}=-0.5V (off-state). FinFETs with 85 nm permieter were fully depleted, whereas FinFETs with larger perimeters sustain an appreciable electron density and therefore a conduction path in the regions further away from the tri-gate that contributes to the leakage current. This implies that the body thickness effect plays an important role in performance degradation even at long gate lengths.

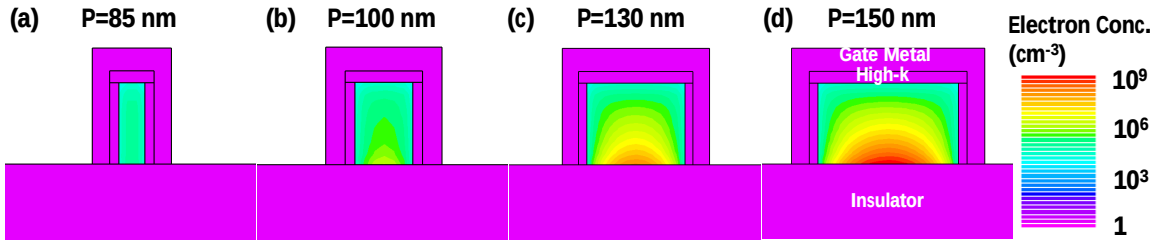


Figure S8. Contour plot of electron concentration at the center of the gate for FinFETs with perimeters of (a) 85 nm, (b) 100 nm, (c) 130 nm and (d) 150 nm, and for a fixed Fin height or 35 nm, obtained from 3D Silvaco simulations and at V_{DS}=0.5 V and V_{GS}= -0.5 V. Thinner FinFETs with smaller perimeters (smaller Fin width) are fully depleted and exhibit sharper SS^{-1}.

References:

[1] J. J. Gu, X. W. Wang, H. Wu, J. Shao, A. T. Neal, M. J. Manfra, R. G. Gordon, P. D. Ye, International Electron Devices Meeting (IEDM) **2012**, 27.6.1.

[2] A. D. Carter, W. J. Mitchell, B. J. Thibeault, J. J. M. Law, M. J. W. Rodwell, Appl. Phys. Exp. **2011**, 4, 091102.