Integration of vertical InAs nanowire arrays on insulator-on-silicon for electrical isolation

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Vertical and electrically isolated InAs nanowires (NWs) are integrated with Si in a technique that bypasses structural defects and transport barriers at the Si–III–V NW interface. Smart-cut® technique is used to transfer a thin InAs layer onto SiO_2/Si and is subsequently used for ordered organometallic vapor phase epitaxy of InAs NWs. The InAs layer in the regions between the InAs NWs is etched resulting in ordered, vertical, and electrically isolated InAs NW arrays. This transfer and fabrication technique enables heteroepitaxy of three dimensional III–V structures on Si and allows the realization of vertical devices with unprecedented control over their architectures. © *2008 American Institute of Physics*. [DOI: 10.1063/1.3013566]

Semiconductor nanowires (NWs) have allowed the realization of several key components for electronic and photonic systems including surround-gate field-effect transistors (FETs),[1,2] light emitting diodes,[3] photodetectors,[4] and waveguides.[5] However, for integrated functional systems, growth or post-growth assembly of NWs at specified locations is necessary but has remained challenging. NW growth at predetermined locations suitable for direct device integration is desired. Typically, e-beam lithography or nanoimprint lithography is utilized to pattern growth seeds at specified locations followed by NW array growth.[6] These arrays can then be used for device fabrication, such as vertical wrap-around gate FETs;[1,2,7–9] however, the presence of the underlying semiconducting substrate precludes electrical isolation and individual addressability of single NWs. NW growth at predetermined locations has also been achieved on (111) sidewall stripes etched on (110) substrates—resulting in the so-called NW bridges.[10–12] Individual addressability may be achieved with this technique but with bulky contacts and added complexity in device fabrication. Postgrowth assembly of individual NWs as well as NW arrays has also been demonstrated. Examples of these are fluidic alignment,[13] electric-field manipulation,[14] Langmuir–Blodgett alignment,[15] and sequential printing of NWs on various types of host substrates.[16,17] While these approaches may be suitable for heterogeneous integration that requires low temperature processing, such as integration to flexible substrates,[16] they may not be suitable for practical fabrication of dense and high performance devices that can compete with current planar devices. It has been argued that future technology nodes should make use of the advancement in mainstream Si technology, and thus, promising high performance devices should be integrated to Si substrates. Demonstrated growth of III–V NWs on Si[18–21] may not represent the ideal candidates for future technology nodes due to the presence of potential barriers at the III–V/Si interface and lack of the ability for addressing single NW devices for multifunctions per chip. In this work, we demonstrate a nonconventional integration scheme for III–V NWs to Si substrates that allows vertical integration, electrical isolation, and individually addressable III–V NWs on Si suitable for three dimensional circuit applications.

III–V NW integration to Si substrates as described here is achieved by a layer transfer technique that combines hydrogen ion implantation and wafer bonding, known as the ion-cut or Smart-cut® process.[22] This approach has been widely used for producing silicon-on-insulator (SOI) wafers. Recently, using this method, III–V materials have been integrated to Si substrates for application in high performance III–V devices on Si substrates, such as waveguide photodetectors[23] and dual junction solar cells.[24] To perform growth of electrically isolated III–V NWs on Si substrates, the Smart-cut® technique is an ideal candidate that allows the formation of an epitaxial III–V base for NW growth on insulator-on-Si.

For these studies, 2 in. InAs (111)*B* wafers were implanted with H ions at 20 keV with a dose of 5×10^{16} cm^{-2} at −15 °C. For high growth yield of vertically aligned InAs NWs normal to the substrate surface, InAs (111)*B* surfaces are preferred.[25,26] The projected range of hydrogen is ~180 nm below the surface. After ion implantation [Fig. 1(a)], the InAs (111)*B* wafer is cut into 1×1 cm^2 chips for wafer bonding. An implanted InAs chip and a Si (100) wafer coated with a thermally grown oxide layer are cleaned using organic solutions and activated using O_2 plasma at 150 W for 30 s.[27] The two pieces are then put into contact at room temperature in air, and the bonded pair is annealed on a hot plate at a temperature of ~60–70 °C for ~10 h to increase the bonding strength. The temperature is then raised to ~120 °C to achieve hydrogen-induced layer exfoliation. The accumulation of trapped hydrogen around the projected range facilitates the formation and development of hydrogen platelets, as illustrated in Fig. 1(c), that eventually lead to exfoliation of the bonded structure near the projected depth [Fig. 1(d)]. The final structure after layer transfer is shown in the cross-sectional field-emission scanning electron microscope (FE-SEM) image of Fig. 1(e) consisting of a ~180 nm thick InAs layer atop a ~70 nm SiO_2 layer on Si. This transferred structure is annealed at 450 °C in air for 1 h under an external applied pressure of

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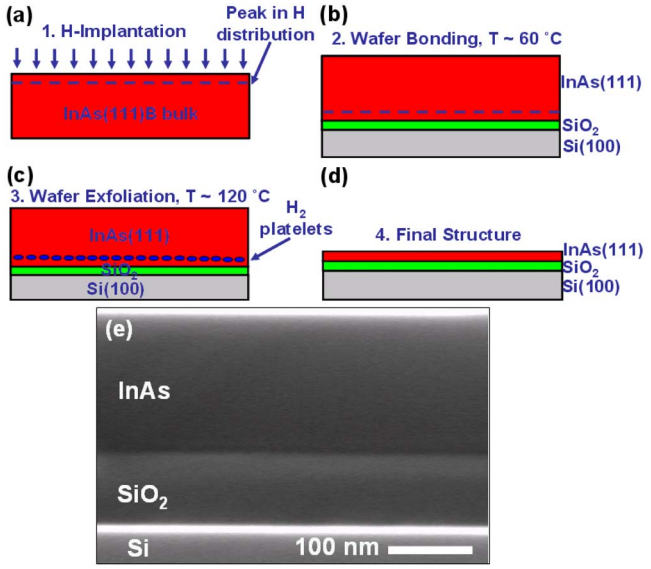

FIG. 1. (Color online) [(a)–(d)] Process flow for ion implantation induced transfer layer to SiO_2/Si. (e) Cross-sectional FE-SEM image of the transferred InAs layer to SiO_2/Si.

1 MPa to further increase the bonding strength for subsequent epitaxial growth.

The spread in the distribution of the implanted hydrogen (i.e., straggle; ~65 nm from SRIM simulations)[28] results in a rough surface morphology directly after the ion-cut procedure. In addition, the hydrogen implantation process results in a damaged crystal structure at the surface.[29] Such damaged and rough surface is not suitable for NW growth due to the presence of abundant nucleation sites that lead to surface growth instead of NW growth. Figure 2(a) shows an atomic force microscope (AFM) topograph of the InAs surface after layer transfer to SiO_2/Si with a rms surface roughness of ~9 nm. When 40 nm diameter Au colloids were deposited atop this surface and organometallic vapor phase epitaxy (OMVPE) growth was performed at conditions optimized for InAs NW growth on InAs (111)*B* surfaces,[26] no NW growth was observed, indicating that surface modification/repair is necessary. To obtain a surface suitable for NW growth, the samples were wet etched in a $HCl:H_2O_2:H_2O$ (100:1:100) solution, followed by thin film OMVPE growth leading to a planarized InAs surface with reduced rms surface roughness of ~3 nm, as shown in the AFM topograph in Fig. 2(b). 40 nm diameter Au colloids were deposited atop the transferred InAs layer and OMVPE growth was performed for 6 min leading to efficient NW growth. Figure 2(c) shows a cross-sectional FE-SEM image at the base of an InAs NW grown on $InAs/SiO_2/Si$. This demonstrates that etching the damaged InAs layer and planarization of the transferred InAs surface enable the growth of InAs NWs on ion-cut transferred layers. In addition, ordered InAs NW growth is also feasible on such layers. For this purpose, e-beam lithography was used to pattern a double layer of positive e-beam resist (MMA/PMMA) followed by e-beam evaporation and lift off for a 25 nm thick Au layer. Consequent OMVPE growth on these patterned substrates leads to ordered InAs NWs grown on $InAs/SiO_2/Si$ with ~60 nm diameter and 4 μm spacing, as shown in the FE-SEM image of Fig. 3(a).

For practical device integration into functional systems, electrical isolation between individual NW devices is necessary. After growth of the NW array shown in Fig. 3(a), another e-beam lithography step is used to pattern resist disks that are aligned and centered on the InAs NW. Wet chemical etching in $HCl:H_2O_2:H_2O$ solution was then used to etch the InAs layer exposing the SiO_2 surface in the unprotected regions. Figure 3(b) shows a FE-SEM image after the InAs etching step illustrating the ordered vertical InAs NW arrays on isolated InAs disks. This constitutes the demonstration of individually addressable vertical NWs, and more importantly, this whole structure is integrated on a Si substrate. Figure 3(c) shows a close up FE-SEM image of an individual InAs NW at the center of an InAs disk on SiO_2 surface that is electrically isolated from other NWs in the array. The diameter of the InAs disk can be controlled by e-beam lithography and can also be used to achieve low resistance Ohmic contacts to the InAs NWs on SiO_2 substrate by metal evaporation directly on the InAs disks for bottom contact formation. This is necessary as InAs NWs grown directly on Si show nonlinear current-voltage (*I-V*) characteristics when current is injected from the NW into the Si substrate and vice versa, due to energy band-edge offsets at the InAs/Si heterointerface.[30] The fabrication and growth processes presented here demonstrate electrical isolation of vertical III–V NWs integrated to Si substrates with a simple geometry and physics of operation for potential devices such as vertical

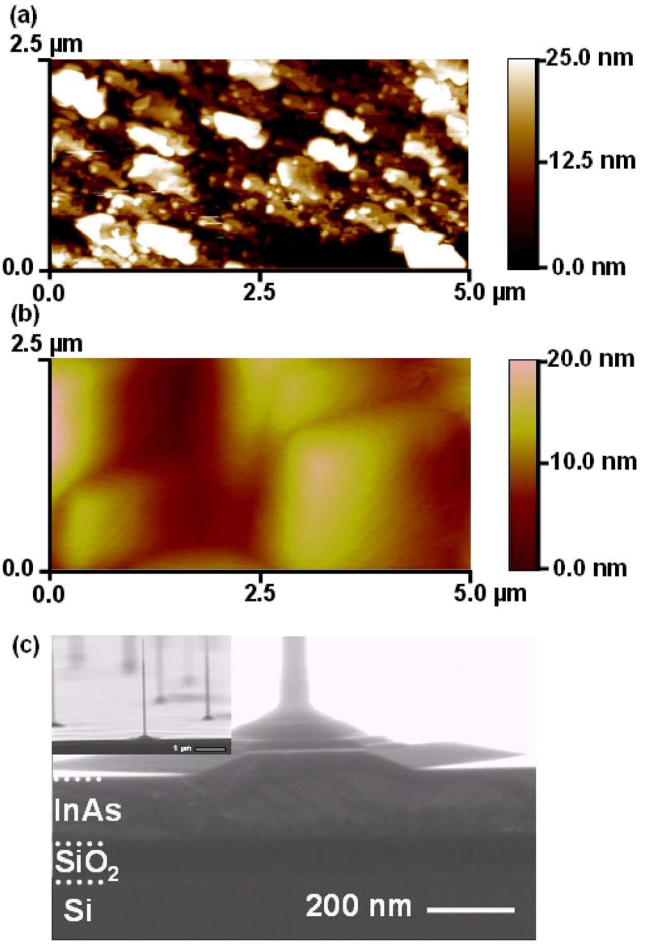

FIG. 2. (Color online) AFM topograph images of InAs on SiO_2/Si (a) directly after ion-cut induced transfer and (b) after wet etching of damaged layer and OMVPE thin film growth. (c) 85° cross-sectional FE-SEM at the base of an InAs NW grown on $InAs/SiO_2/Si$. Inset is FE-SEM image of InAs NWs grown on $InAs/SiO_2/Si$.

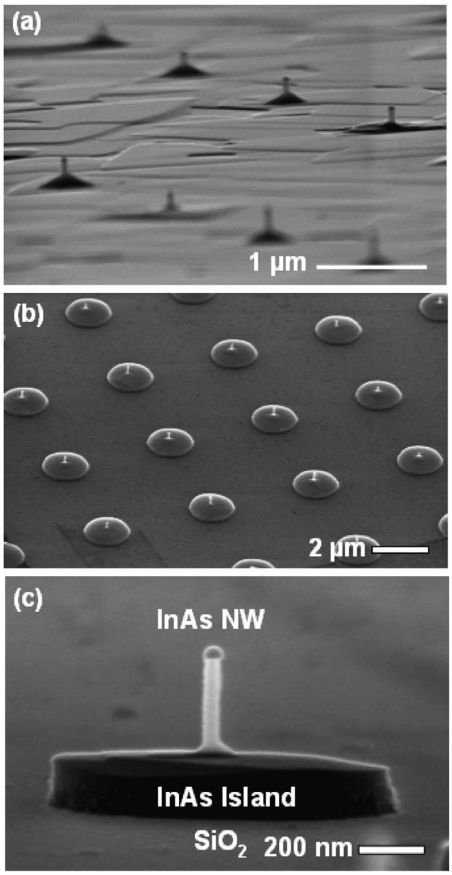

FIG. 3. (a) 85° FE-SEM image of ordered InAs NW arrays grown on $InAs/SiO_2/Si$. (b) 45° angle-view FE-SEM images of vertical and electrically isolated InAs NWs on SiO_2/Si. (c) Zoom-in FE-SEM image of an InAs NW with an InAs island at its base, sitting on SiO_2 substrate and electrically isolated from other NWs for individual NW addressing.

III–V FETs on Si. The set back for this process is the requirement of extremely flat InAs and SiO_2 surfaces. The rms surface roughness for each bonding side needs to be less than 1 nm for the wafer bonding purpose.[31]

In summary, we presented a nonconventional scheme for III–V NW integration to Si substrates that counterparts SOI and extends its concept to high performance III–V NWs on Si. We demonstrate vertical and electrically isolated NWs—as inferred from their structure—with device architecture suitable for practical III–V NW FETs on Si. The capability of III–V NW growth on insulator on Si enables heterogeneous integration to complementary metal-oxide semiconductor (CMOS) technology for hybrid information processing.

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