Advanced core/multishell germanium/silicon nanowire heterostructures: Morphology and transport

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A precise level of control over morphology and transport in germanium/silicon core/multishell semiconductor nanowires is attained by interface engineering. Epitaxial *in situ* growth of such advanced heterostructures is achieved, enabling smooth and crystalline shell quality without *ex situ* thermal or chemical treatment. Transport simulation predicts such heterostructures with engineered energy band-edges will exhibit enhanced on-currents and transconductances over traditional device designs. Based on this synthesis approach, a 2× improvement in experimental hole mobility, transconductance, and on-currents is demonstrated for heterostructures with smooth surface morphologies compared to those with rough surface morphologies and record normalized on-currents for p-type field effect transistors are achieved. © *2011 American Institute of Physics*. [doi:10.1063/1.3574537]

The formation of high quality epitaxial core/shell materials composed of a semiconducting nanowire (NW) surrounded by one or more single crystal shells offers the opportunity for additional control of charge transport in nanostructures.[1–6] While many NW core/shell materials systems have recently gained interest,[7–11] NWs based on the germanium/silicon (Ge/Si) system with its 4.1% lattice mismatch are among the most interesting from technological and basic band gap engineering perspectives.[1,5,12,13]

To avoid issues of Au diffusion which often accompany the synthesis of Ge/Si core/shell NWs, we utilize a growth procedure we have recently introduced that exploits a low temperature axial Si blocking layer to inhibit Au diffusion.[14] Here, we demonstrate *in situ* fabrication of single crystalline Ge/Si multishell radial heterostructured field effect transistors (HFETs) with and without Au diffusion and show how this approach allows NW heterostructure designs with significantly improved transconductances and hole mobilities. Our core/multishell design with engineered composition and doping demonstrate the highest reported maximum on-currents for p-type devices, an aspect of great importance for increased transistor switching speeds.

Figures 1(a)–1(d) show transmission electron microscope images near the center of Ge NWs grown from 10, 30, 50, and 100 nm diameter Au colloids followed by a 2 min Ge shell deposition at a temperature of 410 °C without a Si interfacial barrier layer. Rough NW surface morphology was observed indicative of locally Au-enhanced shell deposition due to Au diffusion on the NW sidewalls. With the addition of the low temperature Si interfacial barrier layer the resultant Ge shell surface is extremely smooth for diameters ≥30 nm as shown in Figs. 1(e)–1(h). For the smallest NW diameter, Au was not found at the tips of those NWs in Figs. 1(a) and 1(e) indicating loss of Au in both cases (with and without a Si blocking layer) during Ge shell growth, as expected for sufficiently small diameters.[14] For the same growth time and temperature, the presence of Au on the NW surface leads to an enhanced growth rate of ~0.375 nm/s [Figs. 1(e)–1(h)] whereas growth of the Ge shell without the presence of Au on the surface proceeds at a growth rate of ~0.21 nm/s [Figs. 1(i)–1(l)]. Thus, the effect of a monolayer of Au on the surface is to both catalyze faster deposition rates and significantly increase surface roughness. For the core/shell NW growth with a Si interfacial barrier layer, the shell sidewall growth is smooth and a slight axial elongation occurs in conjunction with the radial shell deposition. These results demonstrate clear evidence of the effectiveness and importance of this growth procedure in inhibiting Au diffusion on the Ge NW sidewalls for the growth of high quality Ge shell layers. In addition, dopant incorporation through such controlled shell growth allows conformal and uniform distribution of dopant atoms, unlike the longitudinally nonuniform dopant incorporation during nominal NW growth resulting from mixed VLS and VS dopant deposition.[15]

The *in situ* single-growth technique demonstrated in Fig. 1 for Ge/Ge core/shell NWs can also be extended to single crystal Ge/Si core/shell NWs in a single growth run without postgrowth chemical or thermal treatment. Since high temperatures and/or low SiH_4 partial pressures have been found to generally induce Au diffusion on Si NWs,[16] maintaining a SiH_4 partial pressure during transition from the Ge to Si growth temperature, in addition to the low temperature Si barrier layer, was necessary to avoid Au diffusion in the growth of the Si shells. Figures 1(i)–1(k) show a sequence of TEM images of Ge/Si core/shell NWs grown from 10, 30, and 50 nm diameter Au colloids without a Si barrier layer and without maintaining SiH_4 partial pressure during temperature ramp up, which results in Au diffusion and rough Si shell morphology. With a low temperature Si interfacial barrier layer and a SiH_4 partial pressure of 125 mTorr during temperature ramp up, Au diffusion on the Ge NW sidewalls was avoided and single crystal Ge/Si core/shell NWs were grown in a single growth run as demonstrated in Figs. 1(l)–1(n). The Si shell thickness was chosen to be ~3 nm, which is within the coherent critical thickness limit for all Ge

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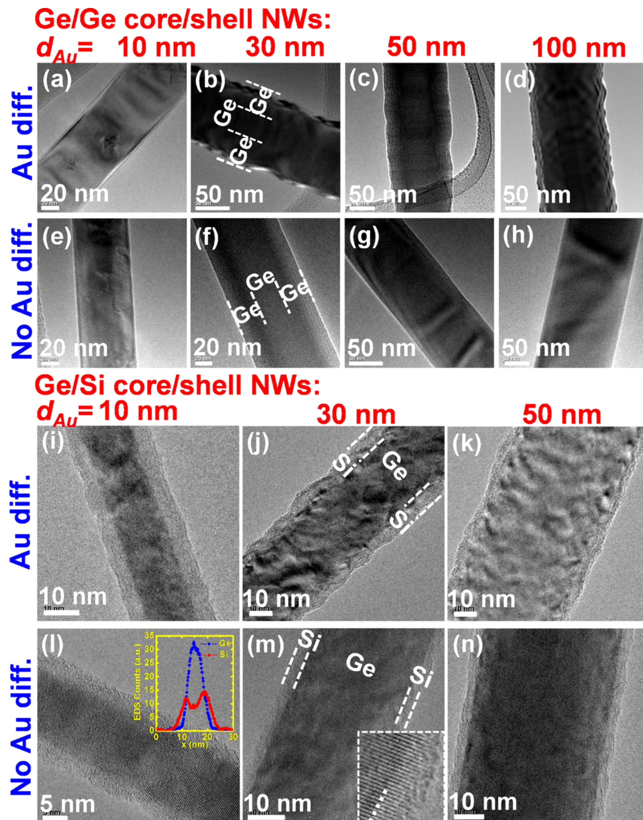

FIG. 1. (Color online) [(a)–(d)] TEM images of Ge NWs grown from Au colloids at 276 °C and subject to temperature ramp up to 410 °C followed by deposition of Ge shells at 410 °C for 2 min [(e)–(h)], same as in [(a)–(d)], however, with a low temperature Si blocking layer step between core and shell growth. [(i)–(k)] TEM images of Ge/Si core/shell NWs without a low temperature Si barrier layer. [(l)–(n)] TEM images of Ge/Si core/shell NWs grown at 276/500 °C with a low temperature Si barrier layer and a SiH_4 input during temperature ramp (10 min) and Si shell deposition (7 min). Inset: (m) is a magnified image near the wire surface. Inset: (l) is an EDX line scan across the diameter of a 16 nm diameter Ge/Si core/shell NW.

core diameters[17] and hence, ensures high crystalline quality of the Si shells without misfit dislocations.

The growth procedure developed here has the advantage of providing multishell growth, fully enabling band gap engineering and control over radial distribution of charge carrier densities to further enhance the performance of Ge/Si heterostructures over previous approaches. To investigate the effects of radial doping profiles on the performance of Ge/Si core/multishell HFETs, we employed three-dimensional (3D) SILVACO ATLAS semiclassical simulations within the framework of the drift-diffusion mode-space method.[18] Three doping situations were considered; (i) 6 nm i-Ge core/1 nm p^+-Ge shell (10^{19} cm^{-3})/2 nm i-Si shell; (ii) 7 nm p-Ge core (2.2×10^{18} cm^{-3})/2 nm i-Si shell; and (iii) i-Ge core/i-Si shell. For the doped core/shell NWs (cases i and ii), the dopant densities were chosen such that the total areal charge density remains constant for direct comparison. A 2 nm Si_3N_4 gate dielectric was used for all three cases.[19]

Figure 2(c) shows the simulated transfer curves for the three situations discussed above. The i-Ge/p^+-Ge/i-Si core/multishell NW heterostructure provides larger carrier density near the Ge/Si interface [Fig. 2(b)] leading to a larger gate capacitance and therefore higher transconductances and on-currents compared to the uniformly doped p-Ge core/i-Si shell case. The i-Ge/i-Si core/shell NWs with no doping is

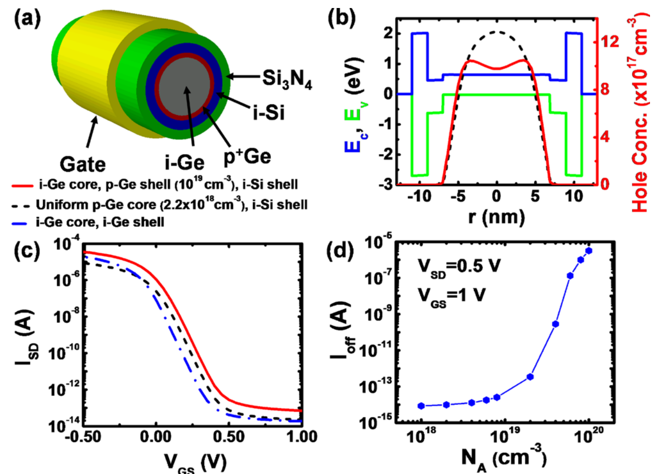

FIG. 2. (Color online) (a) Illustration of a Ge/Si core/multishell NW structure used as an input for Silvaco Atlas 3D simulations. (b) simulations: energy band-edge diagram and free hole density radial distribution for i) 6 nm/1 nm/2 nm i-Ge core/p^+-Ge/i-Si with p^+-Ge$=10^{19}$ cm^{-3} (solid line), and for ii) 7 nm core/2 nm radial p-Ge/i-Si with p-Ge$=2.2\times10^{18}$ cm^{-3} (dashed line), with similar areal doping densities. (c) Simulated transfer curves for the doping scenarios described in text showing higher on-current, and therefore higher transconductance for core/multishell approach. (d) I_{off} for the core/multishell approach as function of Ge-shell acceptor doping density (N_A).

seen to result in the lowest transconductance. Our simulations also indicate that too high of Ge-shell doping levels can lead to high I_{off} [Fig. 2(d)] and show the trade-off between high I_{on} and high I_{on}/I_{off} ratio for optimizing core/shell transistor performance.

These device architectures for multishell NWs with designed doping profiles can be grown with our core/shell growth method described here and the resulting on-current performance is found to give improvements over single shell Ge/Si NW HFETs reported previously.[20] In Fig. 3, we compare the transport properties of i-Ge/p^+-Ge/i-Si core/

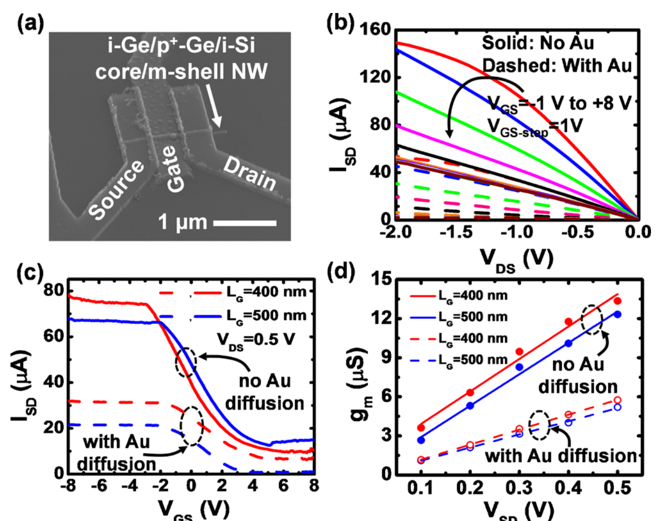

FIG. 3. (Color online) (a) Oblique-angle SEM image of a Ge/Si core/multishell NW HFET. (b) Measured output curves for two devices without (solid lines) and with (dashed lines) Au diffusion both for the same gate voltage steps and same L_G=500 nm. (c) Transfer curves of HFET devices with and without Au diffusion on devices with two different channel lengths showing higher on-currents and transconductances for the case of no Au diffusion. (d) Plot of the transconductance as a function of V_{SD}, the slope of which gives the mobility-capacitance product, which is ~2× higher for the NWs with no Au diffusion.

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multishell NW HFETs grown with and without Au diffusion. Figure 3(a) shows an oblique-angle scanning electron microscope (SEM) image of an HFET device based on a i-Ge/p^+-Ge/i-Si core/multishell NW heterostructure. The output curves from 500 nm channel length HFET devices are shown in Fig. 3(b). The solid lines are measured from heterostructure NWs with no Au diffusion and the dashed lines are obtained from NWs with Au diffusion present on their surface during the core/shell growth. Transfer curves for the same devices as well as for 400 nm channel length HFET devices are shown in Fig. 3(c). The measured on-currents and transconductances from NW HFETs with no Au diffusion are ~2× higher than those measured on NW HFETs with persistent Au diffusion on their sidewalls.

The intrinsic transconductance, $g_m = \mu_h C_g V_{SD} / L_G^2$, where μ_h is the hole mobility, C_g is the gate capacitance, V_{SD} is the source-drain voltage bias, and L_G is the physical gate length.[21] The mobility-capacitance product can therefore be expressed as

$$\mu_h C_g = L_G^2 \, \partial g_m / \partial V_{SD}. \quad (1)$$

Thus, the slope of the g_m versus V_{SD} for the same gate length L_G enables direct comparison of the mobility-capacitance product for the NW devices with and without Au diffusion. Figure 3(d) shows a plot of g_m versus V_{SD} for $L_G = 400$ nm and $L_G = 500$ nm, where the $\mu_h C_g$ product for the case of no Au diffusion is ~2× greater than with Au diffusion. The ratio of the gate capacitances (oxide capacitance in series with the Si barrier capacitance), C_g (no-Au)/C_g (with-Au), is ~1.14.[22] Since the NWs have similar radial dopant profiles, we can conclude that the significant enhancements in transconductances and on-currents for the case of Ge/Si core/multishell NW HFETs with no Au diffusion compared to those with Au diffusion are due to an ~1.75× enhancement in the hole mobilities (μ_h). We note that the contact resistances for both types of wires are much lower than the NW channel resistances, precluding contact resistance effects in the observed output and transfer characteristics in Fig. 3 and the analysis above. Further, core/shell NWs with Au diffusion have lower contact resistances than those grown without Au diffusion, which in turn would lead to higher currents if the mobility for both types of wires were the same, contrary to our experimental observations. The maximum measured current for another device that utilized an $L_G = 400$ nm with a total Ge diameter of 61 nm, was even higher with 122 μA at $V_{SD} = 0.5$ V. The normalized on-current corresponding to the physical dimensions of the device and the applied V_{SD} bias can be expressed as $I_{\max} = I_{SD} L_G / \pi d V_{SD}$. This results in a normalized $I_{\max} = 509$ μA/V, more than two times greater than the previous best value of 211 μA/V.[23] The higher on-currents obtained in our NW multishell devices are enabled by the radial shell doping, which shift the carrier concentrations closer to the gate compared to previous uniform i-Ge/i-Si core/shell NW approaches [Fig. 2(b)]. To achieve even high overall performance of these HFETs, future studies could use higher k dielectric gate insulators, interfaces with lower surface state densities than the Si/Si_3N_4 interfaces used here and conformal wrap-around gates to simultaneously achieve high I_{on}, low I_{off} and steeper turn-on characteristics, however this letter is beyond the scope of this report.

Our growth-by-design approach is demonstrated to further extend electrostatic control in radial FET device architectures for enhanced transport performance by engineering radial energy band-edge and dopant profiles. This controlled epitaxial Si shell growth capability paves the way for experimental determination of the coherent core and shell thicknesses in Ge/Si core/shell NWs and identification of the types of misfit dislocations that arise upon strain relaxation. It will also enable exploration of the influence of strain on charge transport properties without the introduction of additional NW growth and device processing variables such as *ex situ* chemical or thermal treatments.

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