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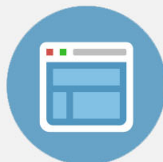
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Atomic layer deposition of platinum with enhanced nucleation and coalescence by trimethylaluminum pre-pulsing

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Conformal coating of metal layers on three-dimensional structures is essential for advanced electronic devices such as storage elements, transistors, and sensors. The quality of atomic layer deposited platinum on oxide surfaces was enhanced by adding pre-deposition pulses of trimethylaluminum (TMA) for improved wetting. With an optimal number of TMA pre-pulses, a 6 nm thick Pt film was perfectly coalesced in contrast to only Pt island formation without TMA pre-pulses. A Pt gate all around Ge/Si nanowire field effect transistor was realized highlighting the potential of this approach for efficient deposition of Pt on 3D nanoelectronic devices. © *2013 AIP Publishing LLC*.
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Atomic layer deposition (ALD) has been utilized to obtain ultra thin and conformal film depositions of various materials for many nanotechnology applications. Its sequential self-limiting reaction after a single monolayer deposition post precursor exposure not only provides a good controllability of thin film growth[1] but also can produce a wide range of materials by various precursors as thoroughly discussed in many review articles.[2–4] Apart from binary and ternary material systems, ALD has shown high quality depositions of transition metals,[5] refractory and noble metals like W,[6] Ta, and Ti,[7] among others. In the case of Pt, the ALD process was developed by oxidizing the organic ligands of trimethyl(methylcyclopentadienyl)platinum(IV), $MeCpPtMe_3$.[8,9] The ALD Pt has been applied in many applications such as in electronic devices as a gate material for metal oxide semiconductor field effect transistors[10] and for catalysis purposes.[11] Recently, it was reported that O_2 plasma enhanced the chemisorption and oxidation of $MeCpPtMe_3$ during the Pt ALD process.[12,13] ALD of Pt by O_2 plasma results in faster growth rate, shorter nucleation delay, higher crystallinity, and wider range of deposition temperatures. However, it still requires several tens of cycles of nucleation delay at the onset of deposition as Baker *et al*. presented in their investigations.[14] Considering the cost of Pt precursors, it is desirable to reduce the Pt film deposition time which can be accomplished by faster nucleation times and shorter precursor pulse times.

In addition to the need for faster deposition rates, Pt ALD needs to be tailored and optimized for specific surfaces. For example, Pt generally does not wet oxide surfaces due to insufficient adsorption sites. This dewetting results in discontinuous Pt island formation followed by eventual coalescence after a large number of pulses to provide enough amount of precursors. Many studies were performed to understand and improve the surface reactions involved in metal ALD deposition.[15] A specific crystal microstructure at the oxide surface[16] and a high temperature anneal[17] showed improvement on the film coalescence of ALD Pt. Lee *et al.* also used piranha solution to increase the density of hydroxyl sites on the oxide surface.[16] W metal which has higher surface energy than Pt was also used in a prior study as an adhesion layer for ALD Pt on oxide surfaces.[18] Similar to Pt, Pd also has long nucleation times on oxide surfaces. Goldstein *et al.* showed improvement of Pd ALD on Al_2O_3 nanoparticles by simultaneous exposure of trimethylaluminum (TMA) during Pd-ALD deposition. TMA was shown by Fourier transform infrared spectroscopy to remove the aluminum hexafluoroacetylacetonate (Al(hfac)*) species that poison the surface and cause a long nucleation period.[19] The TMA surface treatment was shown to improve the wetting behavior and interface properties of gate oxide deposition on III-V semiconductors.[20] In this Letter, the effects of TMA exposure on the coalescence and quality of Pt ALD process on oxide surfaces are presented. Structural and compositional analyses are employed to investigate the features of ALD Pt film with/without TMA exposure. The electrical resistivity as a function of different TMA pulse dosage is measured to support the role of TMA on enhancing the quality of the Pt ALD process. This capability of ALD Pt deposition by TMA pre-treatment for applications in advanced nanoelectronic devices is demonstrated with the fabrication and characterization of functional nanowire transistors with surrounding Pt gates.

A Picosun R-200 plasma enhanced atomic layer deposition (PEALD) system was used to investigate the deposition of Pt and the effects of TMA doses on oxide surfaces. Pt was deposited on two types of surfaces: (i) 1 μm thick SiO_2 layer that was thermally grown on (001) Si substrate for conventional planar thin film assessment as discussed below and (ii) on Ge nanowire (NW) coated with ALD HfO_2 for direct characterization of Pt thickness and conformity on the 3D NW using transmission electron microscopy (TEM). The Ge NW was grown by gold-mediated vapor-liquid-solid technique in a low pressure chemical vapor deposition system.[21] HfO_2 was deposited at 200 °C by sequential pulses of

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tetrakis(dimethylamino)hafnium (TDMAH) and water. The temperature of Pt deposition on all substrates was 300 °C. Prior to Pt deposition, various numbers of TMA pulses (pulse time = 0.1 s) was applied to the sample surface, followed by 6 s of N_2 purge. Ultra high purity N_2 was used for the purge and as a carrier gas for the all sources. The temperature of TMA bubbler was kept at 25 °C. For Pt film deposition, trimethyl(methylcyclopentadienyl)platinum(IV), $MeCpPtMe_3$, (98%, Sigma-Aldrich) and O_2 plasma were sequentially introduced into the reactor. The input pulse time of $MeCpPtMe_3$ (bubbler at 75 °C, N_2 carrier gas with a flow rate of 100 sccm) was 1.9 s, followed by 6 s of N_2 purge. The ALD system has a function of boosting the sources for more efficient deposition. 0.8 s of pre-empty and 1.2 s of master fill of Pt precursor were applied for the boosting function. The actual $MeCpPtMe_3$ pulse time to the reaction chamber was observed to be less than 0.1 s. 80 sccm of O_2 gas flow into the reactor initiated plasma (power = 2000 W) for 10.5 s (2 s for flow stabilization time and 8 s for RF-on-time), followed by 10 s N_2 purge. Scanning electron microscopy (SEM) was used to observe film morphology changes by changing TMA pulse. For compositional analysis, X-ray photoelectron spectroscopy (XPS) was performed (monochromated Al Ka 1486.6 eV x-ray radiation and a source power of 270 W, Kratos Axis Ultra). The resistances of the Pt ALD films were measured by transmission line measurement (TLM) fabricated by photolithography with metal deposition of Ti/Pt/Au (10/50/200 nm). The thickness and the interfacial quality were examined by a Tecnai F30 TEM.

Figs. 1(a)–1(d) show SEM images of ALD Pt film deposited on SiO_2 surface as a function of the number of TMA pre-pulses (0, 20, 40, and 100, respectively) prior to Pt film deposition. For Pt film deposition, the number of $MeCpPtMe_3$ and O_2 plasma cycles was 200 for all cases, which gives ~6 nm Pt film thickness as characterized by TEM. Without TMA pre-pulses, ALD Pt film shows a corrugated structure by several coalesced Pt islands as shown in Fig. 1(a). This indicates that without TMA pre-pulsing, the 200 cycles of Pt ALD process is still in the Pt island-growing regime which is similar to previously reported results for a wide range of Pt ALD cycles.[14] The non perfectly coalesced Pt film morphology is a generally observed behavior at the beginning of the deposition on oxide surfaces. However, when 20 cycles of TMA were pulsed into the chamber prior to Pt deposition, the ALD Pt film became less corrugated (Fig. 1(b)). After 40 cycles of TMA pre-pulses, the Pt film became perfectly coalesced [Fig. 1(c)], which indicates that TMA pre-pulses transitions the Pt deposition from an island-growth regime to a thin film growth regime (see also Fig. 3(c)). Considering that the actual $MeCpPtMe_3$ pulse time is shorter than 0.1 s, this experiment can be classified into the category of "un-saturated pulse region" as described in Ref. 22. We observed that our deposition rate was increased by increasing the Pt precursor pulse time (0.2 s of actual monitored time), indicating that indeed, our experimental conditions (0.1 s of monitored time) belong to the unsaturated growth region. However, in Ref. 23, Zhu *et al.* claimed that Pt ALD film showed mostly granular Pt islands that partially covered the surface when the Pt pulse time was in the unsaturated growth region. Our result, nonetheless, indicates that a certain number of TMA pulses before Pt deposition helps in perfecting Pt coalescence in spite of very short $MeCpPtMe_3$ pulse times.

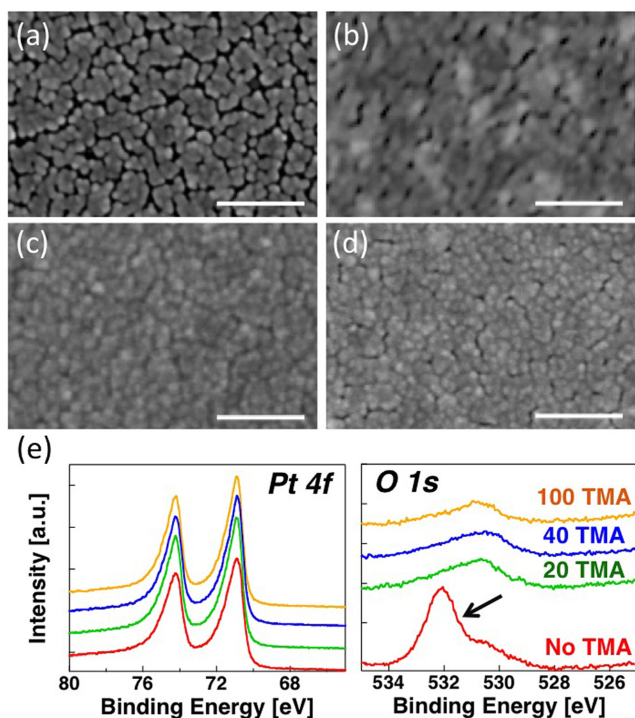

FIG. 1. SEM images of Pt layer (200 cycles of $MeCpPtMe_3$ and O_2 plasma) deposited on SiO_2/Si substrate with (a) 0, (b) 20, (c) 40, (d) 100 TMA pre-pulses. (scale bar: 500 nm) High resolution XPS spectrums of Pt 4*f* and O 1*s* of Pt films were shown in (d) and (e), respectively.

After 100 cycles of TMA pre-pulses, it was observed that the Pt film becomes less coalesced [Fig. 1(d)], suggesting that there is an optimal range of TMA exposure to the surface for thin-film like Pt deposition. Goldstein *et al.*[19] claimed that "oxide surface poisoning" generated from reaction byproducts prohibited the nucleation of ALD Pd and that TMA pre-exposure pulses helped cleaning these byproducts thereby enhancing the nucleation of the ALD Pd film. This characteristic of TMA cleaning effect for the ALD reaction byproducts on III-V compound semiconductor surfaces was also suggested elsewhere.[23] It was previously examined that $MeCpPtMe_3$ tends to preferentially chemisorb on the hydroxyl group on the sample surface.[15] When exposed to TMA, the surface oxide bonds to Al- and form dimethylaluminum (DMA) by releasing H- from OH- and forming CH_4.[24] This surface covered by DMA seems to produce more favorable chemisorption sites for $MeCpPtMe_3$ than hydroxyl groups, consequently resulting in faster nucleation and coalescence of the ALD Pt film. However, as DMA increases on the surface, Al-O-Al bonds could be formed between two adjacent DMAs.[25] In other words, when the number of TMA cycles increases, the possibility of Al-O-Al bonds increases, and the DMA sites which are favorable for $MeCpPtMe_3$ chemisorption decrease accordingly, which agrees with the interpretations of "oxide surface poisoning" by Goldstein *et al.*[19] This agrees well with our results which showed that some range (e.g., 40 cycles) of TMA pulses lead to early coalescence of Pt islands while larger TMA dose (e.g., 100 cycles) causes delayed Pt film coalescence.

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XPS was used to infer information relevant to the interfacial composition as a function of different TMA pulse number. Regardless of the TMA dose, compositions of all Pt films were identical as observed in the XPS spectra [Fig. 1(e)]. The Pt 4*f* peaks for all cases were identical and consisted of several different binding energies (e.g., a shift of Pt 4*f* peaks from Pt-Pt binding energy, about 70 eV, and asymmetric peak slope). This can be caused from organic residues or byproducts during the ALD process. Since no Al peaks were detected in the whole scan range (0 eV–1500 eV), we believe that the Al incorporation from TMA precursor is minuscule and results in negligible effects on the Pt film quality. O 1*s* peaks were identical to each other except for the sample without TMA pre-pulses (see the arrow in Fig. 1(e)). There is an additional peak near 532 eV, which attributes to the SiO_2 layer underneath the Pt layer. Note that for the sample without TMA pre-pulses, the Pt film was island-like as shown in Fig. 1(a); thus, XPS can detect signals from the SiO_2 layer in between the Pt islands. Indeed, the Si 2*p* peaks at 150 eV (not shown) were also detected only in the sample without TMA treatment. This analysis is consistent with the measured low electrical resistivity of the film with TMA doses as shown in Fig. 2(a) and in Table I.

The resistance of the Pt ALD films is plotted in Fig. 2 as a function of L/W, where L is the gap between two adjacent electrodes and W is the width of the electrodes used for the TLM. In Fig. 2, the resistance of the Pt ALD film without TMA dose was divided by 100 to be displayed on the same scale as TMA pre-pulsed samples. High resistivity of the sample without TMA treatment can be expected due to the island-like film morphology in Fig. 1(a). Even though different TMA doses showed slightly different film morphology [Figs. 1(b)–1(d)], their nearly well-coalesced nature resulted in similar resistivity values. Thus, the resistivity of each film could be as low as 2.5 $\mu\Omega$ cm. Low resistivity Pt film can be used for the device purpose as demonstrated in Figure 4 below.

Figure 3 shows high/low magnification TEM images of ALD Pt (200 cycles with 40 cycles of TMA pre-pulses) on

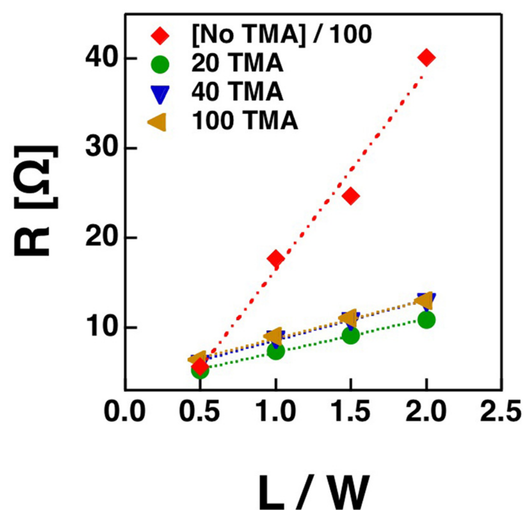

FIG. 2. Resistances [Ω] of Pt films (with different numbers of TMA pre-pulses) are shown as a function of L/W, where L is distance between electrodes and W is a width of electrodes in TLM pattern. Note that the resistance of the sample without TMA was divided by 100 for the purpose of plotting with one of the other samples.

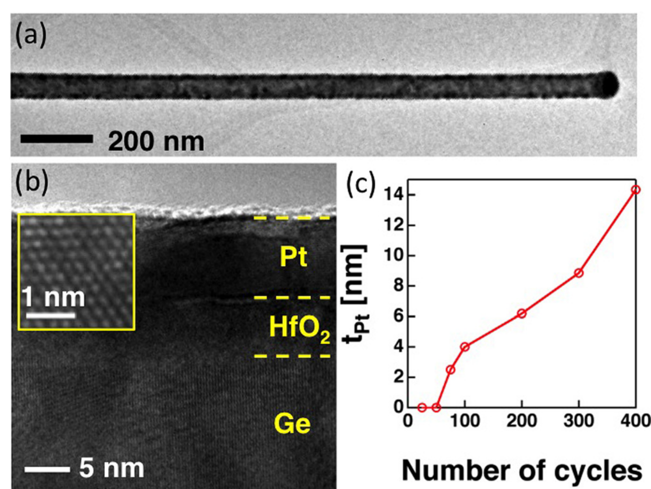

FIG. 3. (a) Lower magnification and (b) higher magnification TEM images of ALD Pt deposited on HfO_2/Ge nanowire with 40 TMA pre-pulses. Inset of (b) shows polycrystalline phase of deposited Pt layer. (c) Thickness of ALD Pt on HfO_2/Ge nanowire as a function of $MeCpPtMe_3$ and O_2 plasma cycles, following 40 TMA pulses.

ALD HfO_2 coated Ge nanowires to observe the microstructure of ALD Pt film, examine the oxide/Pt film interface, and measure the thickness conveniently. The Pt layer completely coalesced across the entire surface of the nanowire as shown in Fig. 3(a). Our ALD was equipped with HfO_2 precursors, which was therefore deposited on the Ge nanowire to provide a consistent oxide surface similar to the SiO_2 surface used for the 2-dimensional planar film (Fig. 1). In addition, the *in situ* process of HfO_2 ALD followed by Pt ALD with/without TMA pre-pulses prohibits undesired contamination at the interface between HfO_2 and Pt such that the TMA dose-dependent interface features could be examined accurately. At high magnification (Fig. 3(b)), sharp and abrupt interface between Pt and HfO_2 was observed. The inset of Fig. 3(b) shows a high resolution TEM (HRTEM) image of the ALD Pt film showing a polycrystalline phase as reported elsewhere.[8] The Pt film thickness measured by TEM was then correlated with different number of $MeCpPtMe_3$ and O_2 plasma cycles as shown in Fig. 3(c) for 40 TMA pre-pulse cycles. With the 40 TMA pre-pulses, the Pt island-growth regime[12,14] can be shifted from more than 200 $MeCpPtMe_3$ cycles [as shown in Fig. 1(a)] down to 50 $MeCpPtMe_3$ cycles. After 50 $MeCpPtMe_3$ cycles, Pt nucleation started and the Pt islands became a coalesced Pt film after nearly 100 cycles. After film coalescence, a linear growth rate was observed (Fig. 3(c)).

To demonstrate the potential application of this ALD Pt deposition technique on high aspect ratio features for nanoelectronic devices, a NW with ALD Pt gate-all-around field

TABLE I. Resistivity [Ω cm] of samples with different numbers of TMA pre-pulses.

Pre-pulses	ρ [$\mu\Omega$ cm]
No TMA	1.3×10^2
20 TMA	2.2
40 TMA	2.7
100 TMA	2.6

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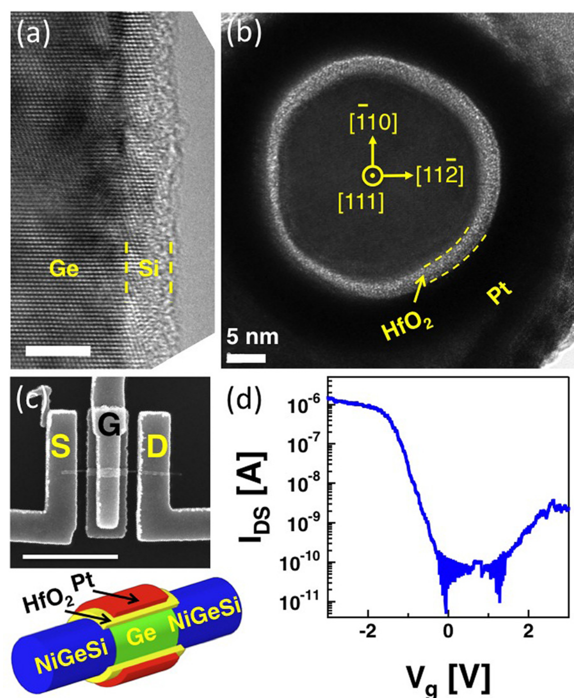

FIG. 4. (a) High resolution TEM image of a Si/Ge core/shell nanowire utilized for gate-all-around FET demonstration. (b) Cross-sectional TEM image of Si/Ge core/shell NW FET with a gate stack of 4 nm HfO_2 and 7 nm Pt (40 TMA pulses, followed by 200 cycles of $MeCpPtMe_3$ and O_2 plasma). (c) Top-view SEM image of the NW FET (top) and a schematic image of processed nanowire inside the FET (bottom). (d) Transfer curve I_{DS} vs. V_g of the NW FET at $V_{DS} = -100$ mV.

effect transistor (FET) was fabricated and characterized. The FET conduction channel consisted of a Ge NW similar to the reference Ge for thickness calibration, but with an additional 3 nm thick Si shell[25] [Figure 4(a)] for enhanced carrier confinement[26] using a growth approach reported elsewhere.[27] The vertically grown Ge/Si core/shell NWs were loaded into the ALD system for ~4 nm of HfO_2 and ~7 nm of Pt (200 cycles) ALD depositions with 40 TMA pre-pulses. These samples were then placed in a vial filled with isopropanol and were subjected to ultrasonic agitation to release the NWs from the growth substrate into the isopropanol solution. Drops of the isopropanol solution containing the NWs were casted on a 200 nm thick Si_3N_4 layer on the Si substrate. The Si_3N_4/Si substrate was pre-patterned with Ti/Au grid marks to locate and record the coordinates of the drop cast NWs for single element device fabrication.

Fig. 4(b) shows a cross sectional TEM image of the core/multiple shell Ge/Si/HfO_2/Pt NW. Except for the Si shell, all other layers were clearly contrasted, with measured thicknesses similar to those desired from the CVD (Ge/Si) and ALD (HfO_2/Pt) depositions. For NWFET fabrication, 130 nm thick and 400 nm wide Cr gate pads were deposited across the NW by using a combination of electron beam lithography and electron beam metal evaporation. This Cr layer also acted as a mask for selective removal of the Pt (using aqua-regia 1 HNO_3:3 HCl) and HfO_2 (using 1% diluted HF) shells for electrical access to the NW channel. A 130 nm thick Ni layer was then deposited on the exposed Ge/Si NW for drain and source contact formation and for electrical leads and pads. The physical separation between the drain and the source was 700 nm, but the actual FET channel length was less than 400 nm by controlling the solid state reaction between Ni and the Ge/Si NW. When annealed at 300 °C, Ni from the drain/source contacts reacted with the NW to form conductive NiGe/NiSi segments that reduced the effective channel length of the un-reacted semiconducting NW from 700 nm to 400 nm. The anneal time was calibrated such that the Ge/Si NW channel was fully overlapped with the Pt/Cr gate, as depicted schematically in Fig. 4(c), to avoid parasitic series resistances for ungated regions. Fig. 4(d) summarizes the characteristics of the Pt-gate-all-around NW FETs at $V_{DS} = -100$ mV. The transistor exhibits a p-type enhancement mode transistor with the on-regime (accumulation) at negative gate voltages where the energy barrier for holes in the valence band is reduced. The increase of I_{DS} at positive gate bias is due to the tunneling of electrons through a narrow electron Schottky barrier at the Ni/Ge contact with an applied positive gate voltage. This ambipolar behavior is an indication that the Pt/Cr gate fully covered the semiconducting Ge/Si channel as desired.[27] The drain/source leakage current as well as the gate leakage current were in the range of 100 pA which is about four orders of magnitude smaller than the drain/source current in the on-regime, showing the effectiveness of the Pt-all around gate in modulating the conductance of the Ge channel.

In summary, we have shown that TMA pre-pulsing is an effective strategy to minimize incubation times in ALD Pt. Without TMA, the Pt island-growth regime on oxide substrates was still observed even for as many as 200 cycles, which was shifted to 50 cycles with TMA pre-pulses and consequent Pt coalescence. XPS data indicated the absence of Al at the Pt/oxide interface, which together with electrical measurements by TLM and morphology characterization by TEM showed high quality Pt layers obtained by our growth method. The potential application of this growth technique was successfully demonstrated with the fabrication of functional Ge/Si gate-all-around NW FETs.

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