FULL PAPER

Structural and Room-Temperature Transport Properties of Zinc Blende and Wurtzite InAs Nanowires

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Here, direct correlation between the microstructure of InAs nanowires (NWs) and their electronic transport behavior at room temperature is reported. Pure zinc blende (ZB) InAs NWs grown on SiO_2/Si substrates are characterized by a rotational twin along their growth-direction axis while wurtzite (WZ) InAs NWs grown on InAs (111)B substrates have numerous stacking faults perpendicular to their growth-direction axis with small ZB segments. In transport measurements on back-gate field-effect transistors (FETs) fabricated from both types of NWs, significantly distinct subthreshold characteristics are observed ($I_{on}/I_{off} \sim 2$ for ZB NWs and $\sim 10^4$ for WZ NWs) despite only a slight difference in their transport coefficients. This difference is attributed to spontaneous polarization charges at the WZ/ZB interfaces, which suppress carrier accumulation at the NW surface, thus enabling full depletion of the WZ NW FET channel. 2D Silvaco-Atlas simulations are used for ZB and WZ channels to analyze subthreshold current flow, and it is found that a polarization charge density of $\geq 10^{13}$ cm^{-2} leads to good agreement with experimentally observed subthreshold characteristics for a WZ InAs NW given surface-state densities in the 5×10^{11}–5×10^{12} cm^{-2} range.

In this paper, we directly correlate the microstructure and room-temperature transport behavior of individual InAs NWs. From transmission electron microscopy (TEM) studies, we distinguished between pure zinc blende (ZB) NWs and wurtzite (WZ) NWs containing stacking faults and small ZB segments. Through detailed device analysis on back-gate NW field-effect transistors (NWFETs), we found insignificant differences in the extracted transport coefficients even though the extrinsic subthreshold characteristics exhibited significantly different behavior for both types of NWs. We show with 2D transport simulations that these differences in subthreshold characteristics can be explained by the presence of polarization charges in the twinned WZ NWs, which compensate surface charges and enable full depletion of the NW channel.

1. Introduction

The vapor–liquid–solid growth of semiconductor nanowires (NWs) has enabled realization of engineered electronic and optoelectronic 1D nanostructures with outstanding promise for device applications.[1] Realization of this promise requires understanding of their growth mechanism,[2] crystal structure,[3] and carrier transport behavior.[4] Understanding the relationships between these NW properties is vital to exploiting their full potential for reliable and reproducible device characteristics. This is particularly important for III–V compound semiconductor NWs for which metastable crystal structures are observed with various growth techniques.[5]

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2. Structural Properties of InAs NWs Grown on SiO_2 and InAs (111)B Surfaces

The InAs NWs were grown in a home-built metal–organic chemical vapor deposition system utilizing Au colloids, trimethyl-indium, and arsine precursors in H_2 carrier gas and a chamber pressure of 100 Torr (1 Torr = 133.322 Pa). The optimal growth conditions for obtaining uniform NW morphology on a SiO_2/Si substrate were found to be a substrate temperature of 350 °C and a molar V/III ratio of 25.[6] Figure 1a shows a typical field-emission scanning electron microscopy (FE-SEM) image of InAs NWs grown on a SiO_2/Si substrate where the NWs grew in random orientations with respect to the surface orientation of the substrate. For a growth time of 15 min, the InAs NW diameters were in the range of 35–80 nm, and their lengths exceed 10 μm, making them suitable for fabricating long channel NWFETs for transport characterization. Figure 1b shows a TEM image of an InAs NW grown on SiO_2/Si. In general, NWs with diameters of ≥40 nm had a twin boundary along their growth-direction axis and exhibited the ZB crystal structure with the ⟨110⟩ growth direction as indicated in the diffraction pattern of Figure 1b. Figure 1c and d show high resolution TEM (HR-TEM) images of the ZB InAs NW taken at two different sections of the twin

Figure 1. InAs NWs grown on SiO$_2$ substrate: a) Top view FE-SEM image. b) Bright field TEM image. The inset is the corresponding diffraction pattern of the same NW indicating a ZB crystal structure with a ⟨220⟩ growth orientation. c,d) Lattice fringes of the same ZB InAs NW with inset FFT patterns of the top and bottom portions showing [011] and [1$\bar{1}$4] pole orientations, respectively. The dashed line in (b–d) highlights the interface between the twinned NW segments.

boundary, which is highlighted by the white dashed line. Fast Fourier transform (FFT) patterns of the TEM data taken at the top (Fig. 1c) or bottom (Fig. 1d) confirmed a common ⟨110⟩ growth direction.

The growth conditions and crystal structure of InAs NWs grown on InAs (111)B substrates were quite different from those on SiO$_2$/Si substrates. The optimal growth conditions for obtaining uniform NWs on InAs (111)B substrates were a growth temperature of 500 °C with a molar V/III ratio of 60.[2f] Figure 2a shows an FE-SEM image of InAs NWs grown on an InAs (111)B substrate where the NWs grew epitaxially normal to the growth substrate. For a growth time of 5 min, the NW lengths were ∼3 μm, and their diameters were ∼55 nm. Figure 2b shows an HR-TEM image of an InAs NW grown on InAs (111)B substrate with its diffraction pattern indicating a WZ crystal structure and [0002] growth direction. It can be noted from Figure 2b that this mostly WZ NW had small ZB segments (one larger section is labeled) in addition to stacking faults perpendicular to the growth-direction axis and twin boundaries separating small ZB sections. Stacking faults were only visible at certain pole-axis orientations, as illustrated in Figure 2c and d, where the NW region near the tip was imaged at the [0$\bar{1}$10] and [2$\bar{1}$$\bar{1}$0] pole directions, respectively. Stacking faults present in these wires were not visible when imaging along the [0$\bar{1}$10] pole. The density of these planar defects was independent of the growth temperature (450–500 °C) and the V/III ratio (20–60), and thus of the NW diameter and morphology, as shown in Figure S1 (Supplementary Information).

Figure 2. InAs NWs grown on InAs (111)B substrate: a) FE-SEM image with a 45°-tilted view. b) HR-TEM image showing lattice fringes with its corresponding diffraction pattern indicating a WZ crystal structure with a [0002] growth direction. Stacking faults are clearly visible and a small ZB segment is highlighted by two white lines. c) HR-TEM image at the InAs/Au tip taken with an electron beam direction (pole) of [0$\bar{1}$10]. d) HR-TEM image of the same NW section in (c) rotated to a pole axis of [2$\bar{1}$$\bar{1}$0] where stacking faults in this section are visible. e) Schematic of the WZ crystal structure with ABAB layer stacking along the [0001] direction. f) Schematic of the ZB crystal structure with ABCA layer stacking along the [111] direction.
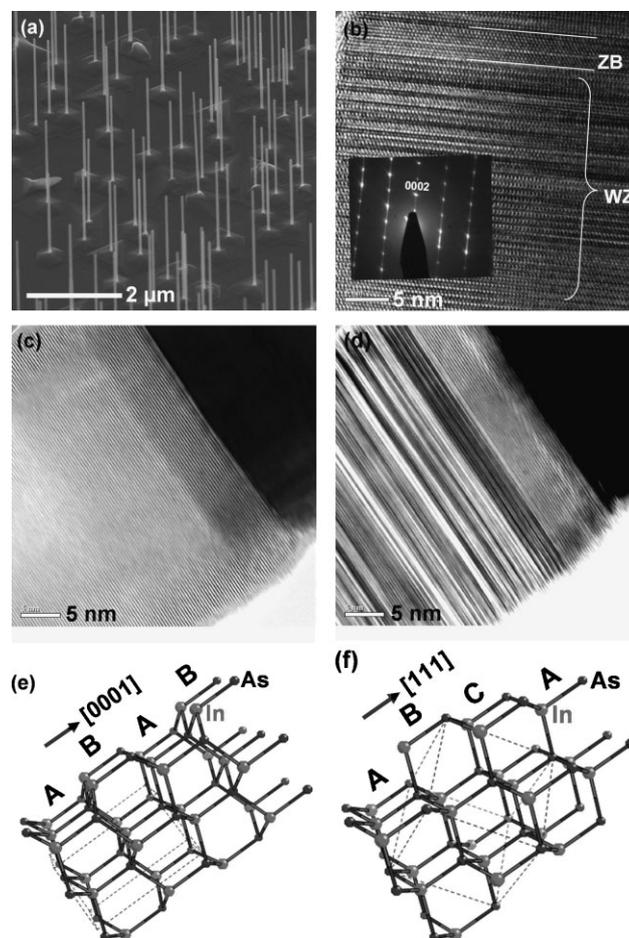
It has been suggested that the surface energies of the NW facets may lead to preferential nucleation at triple phase interfaces, which may favor the formation of WZ NWs for III–V semiconductors at high supersaturations.[7] For InAs NWs/whiskers, nearest-neighbor distances and lattice constants are very close for ZB and WZ crystals[5a] leading to small differences in system energies,[8,9] which in turn results in metastable multiphase structures. During layer by layer growth, a simple change in the atomic stacking sequence from the WZ ABAB to the ZB ABCA structure is sufficient to switch between the two crystal variants, as shown in Figure 2e and f. In general, for growth temperatures of 350 °C or less, ZB InAs NWs have been observed,[5b,6,10] whereas growth temperatures of 390 °C or above resulted in mainly WZ InAs NWs with stacking faults and ZB segments.[5a–c,11]

3. Transport Properties of InAs NWs Grown on SiO₂ and InAs (111)B Surfaces

Back-gate NWFETs fabricated on 100 nm SiO_2/Si using both types of NWs displayed distinct subthreshold characteristics. Figure 3 shows the output and transfer curves for back-gate ZB and WZ InAs NWFETs with equal source–drain separation, $L_{SD} = 3.4\,\mu m$. The inset of Figure 3a shows an FE-SEM image of a representative back-gate InAs NWFET. Since the transport properties, and the extracted transport coefficients thereafter, can be influenced by surface states,[12] the potential between the gate and source, V_{GS}, was swept at a constant rate (50 mV s⁻¹) and in the same direction (from −20 to +20 V) during the measurements of all 17 devices discussed in this paper. In Figure 3, we note the following: i) The ZB NWs exhibited poor subthreshold characteristics with the ratio of the on and off current at $I_{on}/I_{off} < 2$ (Fig. 3c), whereas the WZ NWs show far better subthreshold characteristics with $I_{on}/I_{off} \sim 10^4$ (Fig. 3d). This difference will be the focus of discussion in the following sections of the paper. ii) The measured currents (and current densities) at the same V_{GS} and source–drain potential (V_{DS}) are larger for the ZB NWFETs than for the WZ NWFETs by about one order of magnitude (Fig. 3a and 3b). This is due to differences in contact resistances (R_c) extracted from the transmission line method; the R_c of ZB is 1480 Ω whereas that of WZ is 11 280 Ω (Fig. S2, Supplementary Information).[13] iii) Both types of NWFETs showed an increase in the current at negative V_{GS} values that were below the threshold voltage (V_t), owing to long surface-state trapping/detrapping time constants (on the order of tens of seconds)[12] and ambipolar transport. These trends were observed for all NW diameters (D_{NW}) and L_{SD} values used in the NWFETs. As the channel length increased, the gate transconductance increased as a function of $1/L_{SD}$ (see Fig. S3), and the I_{on}/I_{off} ratio was significantly reduced for WZ NWs, as expected. Figure 4 shows the output and transfer curves of a relatively short-channel WZ InAs NWFET with $L_{SD} = 835$ nm, determined from high magnification FE-SEM images after transport measurements. The output curves in Figure 4a show breakdown characteristics, attributed to impact ionization,[14] for high V_{DS} values of a few hundred mV. The transfer curves of the short-channel NWFET (Fig. 4b) exhibited lower I_{on}/I_{off} ratios (∼10) than those of the long-channel case (Fig. 3d), due to short-channel effects, which become severe at $L_{SD} \sim 1\,\mu m$ for this device structure under ideal conditions, i.e., without taking into account interface state capacitance.[15]

In order to calculate the transport coefficients of these devices, we had to extract the intrinsic output and transfer curves by taking into account the series and leakage resistances. This was done based on a simple DC equivalent model that was previously discussed in detail.[4e,12] Here, the series resistance at the source (and drain) side was $R_c/2$. The leakage resistance, R_{leak}, was calculated from the output and transfer curves for each of the 17 devices under consideration ($R_{leak} \sim 5 \times 10^3$–$1 \times 10^5$ Ω for ZB NWs and 2×10^5–2×10^9 Ω for WZ NWs). These values were dictated by the high I_{off} value for the ZB NWFET and the low one for the WZ NWFET. Table 1 and 2 summarize the NWFETs device dimensions, measured resistance (R) and transconductance (g_m), and extracted mobility (μ) and carrier concentration (n) for all 17 ZB and WZ devices. The average values of the free carrier concentration and mobility are the following: $n_{av}(ZB) = 6.4 \times 10^{17}$ cm⁻³, $n_{av}(WZ) = 8.5 \times 10^{17}$ cm⁻³, $\mu_{av}(ZB) = 2200$ cm² V⁻¹ s⁻¹, and $\mu_{av}(WZ) = 1700$ cm² V⁻¹ s⁻¹. The slight difference in the mobility values and carrier concentration cannot account for the distinct subthreshold characteristics of the ZB and WZ NWFETs.

4. Electronic Structure of WZ/ZB InAs NWs

To explain the difference in the subthreshold characteristics, we instead consider the electronic structure of the WZ/ZB InAs interface. The optical properties of rotationally twinned InP NWs were recently correlated with their twinned crystal structure[16] based on the energy band-edge offsets of the WZ/ZB heterostructure interface.[17] For bulk InAs, the band offsets are $\Delta E_c = 86$ meV for the conduction band and $\Delta E_v = 46$ meV for the valence band with staggered band-edge alignment at the WZ/ZB heterointerface.[17] Photoluminescence measurements of InAs–InP core/shell NWs[18] and InAs$_x$P$_{1-x}$ NWs[11b]

Figure 3. Output characteristics of long channel ($L_{SD} = 3.4\,\mu m$) back-gate InAs NWFETs ($V_{GS} = -20$ to $+20$ V in 10 V steps) made from a) ZB ($D_{NW} \sim 81$ nm) and b) WZ ($D_{NW} \sim 60$ nm) InAs NWs. Inset of (a) is a SEM image of a representative back-gate NWFET device. c) Transfer characteristics of the NW in (a) showing $I_{on}/I_{off} < 2$ and d) of the NW in (b) showing $I_{on}/I_{off} > 10^4$ at $V_{DS} = 0.5$ V. I_{DS} is the source–drain current.

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indicated an energy bandgap increase of $\sim$150 meV (without subtracting strain-induced band shift) and $\sim$120 meV (by extrapolation to pure InAs), respectively. Theoretical predictions of the bandgap increase in WZ with respect to ZB InAs NWs suggest a lower value of $\sim$55 meV,[9] which is close to that calculated for bulk InAs.[17] In this work, we used bulk band-edge offsets as input parameters to a 2D Silvaco-Atlas simulator for

Table 2. Device dimensions and average extracted transport coefficients for the WZ InAs NWFET devices.

Device	L_{SD} [µm]	D_{NW} [nm]	R [kΩ]	g_m [µS]	μ [cm^2 V^{-1}·s^{-1}]	n [cm^{-3}]
C6	4.8	41	60.2	1.0	1330	1.7×10^{18}
C1	3.4	61	28.2	2.2	1980	8.6×10^{17}
C7	3.3	61	34.8	1.8	1350	3.8×10^{17}
C5	2.9	51	44.3	1.2	880	1.2×10^{18}
C4	1.2	53	60.2	5.4	2350	3.3×10^{17}
C8	0.8	57	14.2	4.2	2120	1.0×10^{18}
C2	0.7	45	14	8.4	1990	4.1×10^{17}

calculating the current–voltage (I–V) characteristics of device structures having material compositions and thicknesses similar to those used in experiment.

Figure 5a shows the device structure used in the 2D simulations, which consisted of a highly doped n-type Si substrate used as the back-gate, a 100 nm thick SiO$_2$ layer, and an InAs channel with Ti/Al source–drain electrodes. The device shown in Figure 5a represents the twinned WZ/ZB NWs with a 3.5 nm ZB section inserted every 28.5 nm of WZ sections, which was found to be the average value over the entire length of WZ NWs based on TEM studies. For simulation accuracy, the x-mesh spacing used was 0.8 Å in the ZB segments and 6 Å in the WZ segments, restricting the channel length to a maximum of 400 nm. The energy bandgaps and electron affinities were adjusted such that the band offsets in the WZ/ZB hetero-interfaces were equal to those of the bulk as depicted in Figure 5b.[17] The mobilities and contact resistances that were calculated in the experiment were inputted into the simulator in the case of pure ZB and WZ/ZB channels. A doping density of 5×10^{16} cm^{-3} and donor-type[19] surface-state density (fixed positive charges) of $\sim$10^{12} cm^{-2} were used to obtain free carrier concentration values similar to those extracted from experiments.[20] Large band offsets, such as in the case of InAs NWs with InP segments inserted along their axis, have previously led to improved subthreshold characteristics relative to those of homogenous InAs NWs.[21] Carrying out I–V simulations for the device shown in Figure 5a with these input parameters discussed above (including WZ/ZB band offsets) resulted in similar subthreshold characteristics to those of the pure ZB case. The band offsets for the WZ/ZB channel did not result in enhanced turn off characteristics similar to those obtained in experiment. Thus, band offsets alone cannot explain the significant difference in the subthreshold characteristics between the ZB and the WZ/ZB NWs.

It is known that hexagonal crystals have nonzero spontaneous polarization, which will lead to polarization fields and charges at the opposite {0001} faces of the crystal,[22] as shown schematically in Figure 5c. Such polarization charges have not been considered before in the context of WZ III–V NWs. The presence of these spontaneous polarization charges, which are in the form of sheet charges perpendicular to the direction of current flow, will lead to electric field modulation across the channel length, in the absence (or presence) of any applied external fields. The negative polarization charges will compensate the positive ones that are induced by surface states, which typically result in electron accumulation at the InAs surface.[23] Figure 5d shows a simulated

Figure 4. a) Output characteristics of a relatively short-channel back-gate WZ InAs NWFET with $L_{SD} \sim 835$ nm and $D_{NW} \sim 57$ nm ($V_{GS} = -20$ to $+20$ V in 2.5 V step). b) Transfer characteristics of the same NW in (a) showing $I_{on}/I_{off} < 10^2$ at $V_{DS} = 0.5$ V.

Table 1. Device dimensions and average extracted transport coefficients for the ZB InAs NWFET devices.

Device	L_{SD} [µm]	D_{NW} [nm]	R [kΩ]	g_m [µS]	μ [cm^2 V^{-1}·s^{-1}]	n [cm^{-3}]
D3	4.4	72	10.1	1.5	1610	6.8×10^{17}
D7	3.6	53	12.0	1.8	1730	1.1×10^{17}
D4	3.5	67	58.7	1.2	1360	6.4×10^{17}
D18	3.4	81	35.9	2.8	4010	4.1×10^{17}
D15	3.4	52	82.2	5.1	4630	7.1×10^{17}
D14	1.7	38	27.1	2.7	1460	1.5×10^{18}
D10	1.6	62	7.5	8.8	500	3.5×10^{17}
D5	1.6	74	4.1	4.3	2400	6.0×10^{17}
D13	1.5	97	6.8	3.2	1650	7.4×10^{16}
D8	0.75	56	4.5	8.1	2600	1.3×10^{18}

Figure 5. a) Device structure used for 2D Silvaco-Atlas simulation showing 3.5 nm ZB sections inserted every 28.5 nm of WZ, which was based on the HRTEM image of Figure 3d with a total L_{SD} of 400 nm. b) Energy band-edge profile of a small section along the channel length plotted at thermal equilibrium, showing band-edge discontinuity and alignment at the WZ/ZB interface in the absence of interface charges. c) Spontaneous polarization charge distribution at the WZ/ZB heterointerface. d) Energy-band profile and electric field for the same section in (b), plotted in the presence of 10^{13} cm^{-2} spontaneous polarization charges. The variable, x, refers to the distance from the source electrode.

plot of the field, E_{Field}, and energy band-edge profiles at thermal equilibrium for the device structure in Figure 5a and in the presence of polarization charges at the WZ/ZB heterointerfaces that lead to accumulation and depletion at the opposite faces of the WZ crystals. The spontaneous polarization charge density for WZ InAs has not been calculated before. For hexagonal crystals, such as GaN, AlN, InN, and ZnO, the spontaneous polarization charges are 1.81×10^{13}, 5×10^{13}, 2×10^{13}, and 3.56×10^{13} cm^{-2}, respectively, all of which are comparable to 10^{13} cm^{-2}.[24] Therefore, we assumed here a lower bound of 10^{13} cm^{-2} for

the spontaneous polarization charge density of InAs, which was introduced at the edges of the WZ/ZB segments of the channel in the following simulations. We note that strain-induced piezo-electric charges in the InAs/InP double barrier NW hetero-structures[25] have been used to explain the asymmetry of tunnel resonance peaks with the polarity of applied voltage.[26] In the WZ NWs subjected to these studies, the average lattice spacing of the {0001} planes was 0.3536 nm, deduced from the average of six HRTEM images (Fig. S4); this is 1.1% larger than the bulk value of ZB InAs (0.3498 nm). Using the calculated piezoelectric coefficient for ZB InAs in the (111) direction,[27] we estimated a piezoelectric charge density of $\sim 5 \times 10^{11}$ cm^{-2}, which is 1–2 orders of magnitude lower than that required to observe the experimental subthreshold trends (as we show below) and of typical spontaneous polarization charge density in WZ materials.

5. Spontaneous Polarization Charge Effects in WZ/ZB InAs NWs

Figure 6a and b show contour plots of the free carrier concentration in the simulated ZB and WZ back-gate InAs NWFETs, which were obtained at $V_{GS} = -20$ V, $V_{DS} = 0.5$ V, and a surface-state density of 10^{12} cm^{-2}. In the WZ case, a spontaneous polarization charge of 10^{13} cm^{-2} for the WZ/ZB channel was used. The top portion of the ZB channel still shows electron accumulation, whereas field modulation due to the presence of spontaneous polarization charges in the WZ/ZB case leads to depletion that penetrates throughout the body of the channel. This is further illustrated in Figure S5 (Supplementary Information), which shows line-cut profiles of carrier density and energy band-edge diagrams along the x- and y-directions. Figure 6c–f show the output and transfer curves (at $V_{DS} = 0.1$ V) for both device structures. Similar trends to those obtained in experiment were reproduced in these simulations. Specifically, it can be seen that the ZB channel resulted in poor subthreshold characteristics and the WZ channel resulted in $I_{on}/I_{off} > 10$, which is consistent with that obtained experimentally for the short-channel InAs NWFET case shown in Figure 4b. The current increase for negative V_{GS} values below V_t was due to hole inversion at the gate side of the channel (Fig. S5c–d, Supplementary Information), which resulted in ambipolar transport (transient effects were not considered in these simulations). The lower current values in the simulations for both ZB and WZ/ZB channels were most likely due to the underestimated mobilities in our measurements[12] and the different geometry between them. Nonetheless, the experimentally observed trends in the subthreshold characteristics were reproduced in simulation when the effect of spontaneous polarization charges was taken into account.

The spontaneous polarization charge density that was used in the simulations discussed above was 10^{13} cm^{-2}. To obtain a better understanding of what polarization charge density is required to deplete the InAs channel in the WZ/ZB NW, we performed a set of simulations to calculate the I_{on}/I_{off} ratio while changing the surface-state density in the range of 1×10^{11}–5×10^{12} cm^{-2} and assuming a spontaneous polarization density of 5×10^{11}–1×10^{14} cm^{-2}. Figure 7 shows the results of these simulations,
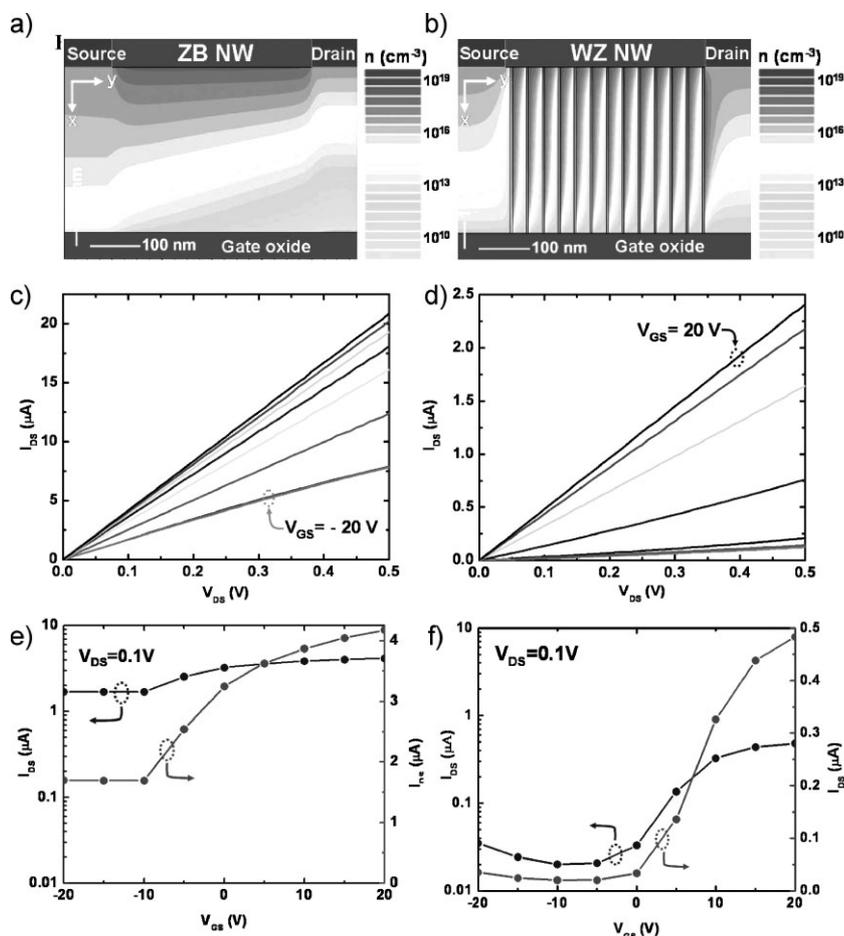
Figure 6. 2D simulation results showing contour plots of carrier concentration across the length and depth of an InAs slab within a) pure ZB device and b) a WZ/ZB InAs heterostructure device. The contour plots were extracted at $V_{DS} = 0.5\,V$ and $V_{GS} = -20\,V$, and they show stronger depletion in (b) penetrating deeper across the channel body. Output characteristics for c) ZB devices and d) WZ/ZB devices with $V_{GS} = -20$ to $+20\,V$ in $+5\,V$ steps. Transfer characteristics at $V_{DS} = 0.1\,V$ for e) ZB devices and f) WZ/ZB devices. The trends observed in the output and transfer curves are similar to those experimentally obtained for the fabricated FETs showing stronger depletion for the WZ devices with ZB segments inserted across the channel length. The current was normalized to a $60\,nm \times 60\,nm$ slab with $L_{SD} = 400\,nm$.

6. Conclusions

In summary, we have correlated the microstructure and transport properties of individual InAs NWs to elucidate the origin of dramatic differences in subthreshold current for NWFETs fabricated from InAs NWs grown on SiO_2/Si and InAs (111) B substrates. From NWFET measurements and analyses, we found that pure ZB NWs grown on SiO_2/Si exhibit poor subthreshold characteristics when compared to WZ NWs with small ZB segments grown on InAs (111)B. We attribute this difference to the presence of spontaneous polarization charges at the WZ/ZB interface. These polarization charges create negative fields that lead to depletion of the NW surface, surpassing carrier accumulation caused by interface charges. This is confirmed by 2D Silvaco-Atlas simulations in which the trends in the subthreshold characteristics for WZ/ZB NWs have been reproduced only when polarization charges of $\sim 10^{13}\,cm^{-2}$ at the WZ/ZB interface were inserted. These results provide new insights and considerations into the design of electronic devices utilizing VLS-grown InAs NWs.

7. Experimental

Growth: InAs NW growth was performed in a horizontal home-built organometallic vapor-phase epitaxy (OMVPE) reactor at a pressure of 100 Torr (1 Torr = 133.322 Pa) with trimethylindium (TMIn) and arsine (AsH_3) precursors in 1.2 slm (standard liters per minute) H_2 carrier gas. Au colloids (40 nm diameter, Ted Pella, California, USA) were dispersed from solution on cleaned substrates pretreated with poly-L-lysine, which were then loaded into the OMVPE reactor. The temperature was ramped up at a rate of $\sim 2\,°C\,s^{-1}$, and allowed to stabilize at the growth temperature in a H_2 atmosphere. The reaction precursors were introduced for the duration of the growth run, after which AsH_3 flow was maintained during the cool down period for 2 min followed by a 2 min H_2 purge; the reactor was then left with a N_2 atmosphere until sample removal. For uniform NW growth, a temperature of 350 °C and a molar V/III ratio of 25 were found to be optimal for NW growth on SiO_2/Si surfaces, whereas a temperature of 500 °C with a V/III ratio of 60 were found to be optimal for NW growth on InAs (111)B surfaces.

Device Fabrication and Characterization: The grown NWs were then sonicated in ethanol solution for 7 s to suspend them in the solution and were then transferred to a 100 nm SiO_2/n^+Si substrate with a prepatterned indexed grid with alignment marks. Optical microscopy was used to determine the location of the randomly dispersed NWs on this grid structure. Patterning of contacts using electron beam lithography followed by 15 nm/85 nm Ti/Al metallization and a standard liftoff process were used to create ohmic contacts to the NWs. Current–voltage characteristics were then obtained with an HP 4155 semiconductor parameter analyzer (California, USA) in air at room temperature. The device dimensions were measured after electrical measurements under the highest attainable magnification using an FEI XL 30 FE-SEM (Oregon, USA) operating at 30 kV acceleration voltage.

again for a back-gate 400 nm InAs channel with a 100 nm thick SiO_2 layer. For a surface-state density $\leq 2.5 \times 10^{12}\,cm^{-2}$, a polarization charge density of $\sim 10^{13}\,cm^{-2}$ was required to obtain significant current modulation in the InAs channel. This value is dependent on the width of the ZB segments (3.5 nm considered here) and their density across the channel length. The values of surface-state density are comparable to what has been previously estimated for InAs NWs,[12,20,21] and those of the spontaneous polarization charge density are also comparable to what has been obtained for hexagonal crystals.[24] As the density of spontaneous polarization charges was increased, surface accumulation was further compensated, and the threshold voltage shifted toward 0 V. High densities of polarization charges ($n_{pol} \geq 4 \times 10^{13}\,cm^{-2}$) resulted in complete depletion of the InAs channel, which explains the reduction in the I_{on}/I_{off} ratio for $n_{pol} \geq 10^{13}\,cm^{-2}$.

Figure 7. Plot of I_{on}/I_{off} as a function of polarization charges at the WZ/ZB heterostructure for different surface-state (fixed positive charge) density values simulated for $V_{DS} = 0.1$ V and $V_{GS} = +20$ V (I_{on}) and $V_{GS} = -20$ V (I_{off}). A polarization charge density of $\sim 10^{13}$ cm^{-2} or higher was required to obtain strong current/carrier modulation in the channel for reasonable values of surface-state densities.

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