Scanning gate microscopy of InAs nanowires

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Scanning gate microscopy, in which a conductive probe tip in an atomic force microscope is employed as a local, nanoscale top gate contact, has been used to characterize local carrier and current modulation effects in a 45 nm diameter InAs semiconductor nanowire grown by metal organic chemical vapor deposition. Measurement of current flow in the nanowire as a function of tip position reveals that for both positive and negative tip bias voltages, carrier and current modulation is strongest when the probe tip is near the source and drain nanowire contacts, reaching a global maximum approximately 100–200 nm distant from the source contact and a secondary maximum a similar distance from the drain contact and decreasing at greater tip-contact distances. This effect is explained, with verification by numerical simulation, as a consequence of the capacitance between the tip and the source and drain contacts as a function of tip location. Measurement of transconductance as a function of tip position reveals that the transconductance is approximately 80%–90% greater near the source contact than at the center of the nanowire. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2746422]

Recent years have witnessed an explosion of interest in semiconductor nanowires as building blocks for a variety of nanoscale electronic[1–3] and optoelectronic[4–6] devices. Among these, the semiconductor nanowire field-effect transistor[7,8] has drawn particular interest, both as a vehicle for basic investigations of electronic structure and carrier transport and as a potential future high-performance electronic device for large-scale integrated systems.[9] InAs is of particular interest for these applications[3,10] due to its small energy band gap and consequent high electron mobility[11] and large quantum confinement energies. However, scaling of such devices to the nanoscale dimensions at which the desired levels of performance can be achieved will require detailed characterization and understanding of carrier transport and modulation behavior in nanowires.

To this end, scanning gate microscopy (SGM) has been employed to characterize local carrier modulation behavior in a variety of material systems and device structures.[12,13] In this technique, a conductive probe tip is used in an atomic force microscope (AFM) as a local, positionable gate contact to a transistor channel region to which source and drain contacts have been fabricated and electrical current flowing between the source and drain is measured as a of the position and voltage of the probe tip. We have used SGM to characterize local carrier and current modulation behavior in InAs semiconductor nanowires grown by metal organic chemical vapor deposition (MOCVD). A strong dependence of the effectiveness of current modulation by the conducting probe tip on position is observed, with modulation being maximized approximately 100–200 nm from the source and drain contacts, and strongest near the source contact. Quantitative analysis reveals an increase in transconductance of 80%–90% for gating near the source contact compared to the midpoint between the source and drain.

The InAs nanowires employed in these studies were grown by MOCVD on thermally oxidized Si substrates, upon which colloidal Au nanoparticles ~40 nm in diameter had been deposited. The nanowires were unintentionally doped *n* type, with diameters in the range of 40–100 nm. Following sonication to release the nanowires into solution, the nanowires were deposited onto a 600 nm SiO_2 layer produced by thermal oxidation on a n^+ Si (001) substrate. Electron beam lithography followed by 15 nm Ti/85 nm Al metallization and a standard lift-off process was used to create source and drain Ohmic contacts to the randomly positioned nanowires. The well-known phenomenon of Fermi-level pinning above the conduction-band edge of InAs (Ref. 14) enabled ready formation of low-resistance Ohmic contacts to the InAs nanowires. After fabrication of the Ohmic contacts, 20 nm SiO_2 was sputtered on top of the sample to act as an insulating layer separating the probe tip from the InAs surface.

Scanned probe measurements were performed using a Digital Instruments/Veeco Dimension 3100 scanning probe microscope with a Nanoscope IIIa controller. A specially designed custom sample holder was used to enable wire bonding between the source and drain contact pads on the sample and wiring to external electronics for measurement of current flow within the nanowire. A schematic diagram of the experimental geometry is shown in Fig. 1. A metal-coated scanning probe tip to which a dc voltage V_g was applied served as the positionable gate contact to the nanowire. A dc bias voltage V_{ds} was applied between the source and drain contacts with the source contact grounded, and the resulting current I_{ds} measured as a function of the tip position and bias voltage.

Figure 2(a) shows an AFM topograph of an InAs nanowire and the source and drain Ohmic contacts to the wire, from which a channel length of ~1 μm and a nanowire diameter of 45 nm (corresponding to the nanowire height measured by AFM) can be determined. Figures 2(b)–2(f) show SGM images of current flow within the nanowire, obtained for $V_{ds}=+0.3$ V and V_g ranging from −4 to +4 V. All SGM images shown were obtained at a scan frequency of 0.3 Hz,

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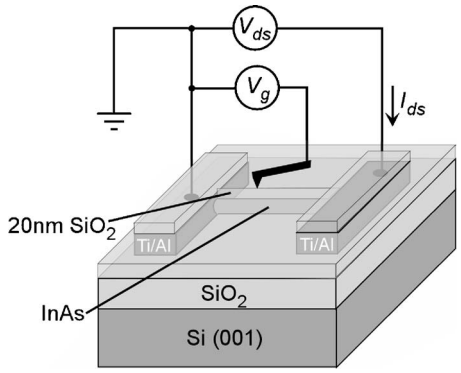

FIG. 1. Schematic diagram of probe tip and sample geometry, and electrical biasing configuration for SGM measurement.

corresponding to a tip scan speed of 1.8 μm/s. For $V_g < 0$ V, we see from Fig. 2(b) and 2(c) that, as expected, electrons are depleted from the *n*-type InAs nanowire in the vicinity of the probe tip and current flow is correspondingly reduced (dark contrast). At $V_g = 0$ V, we see from Fig. 2(d) that negligible modulation of nanowire current flow occurs. For $V_g > 0$ V, Fig. 2(e) and 2(f) show that additional electron accumulation in the InAs nanowire is induced by the positively biased probe tip, leading to an increase in current flow

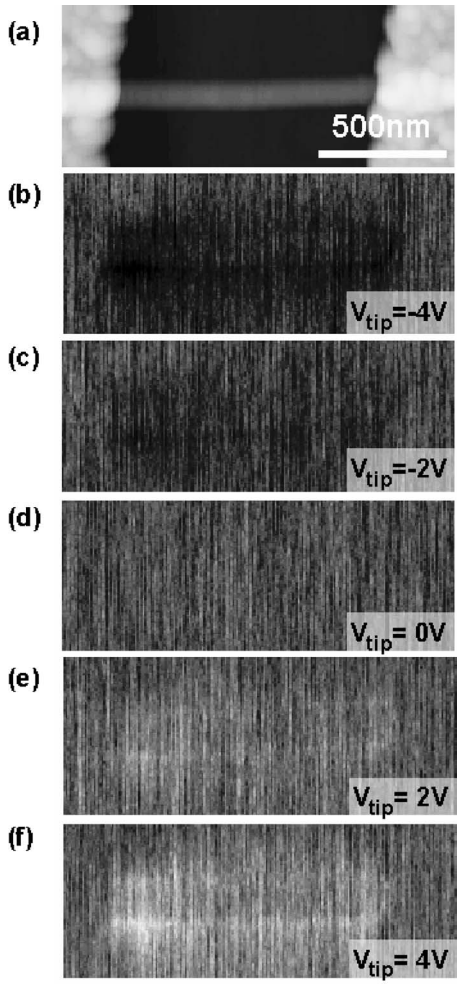

FIG. 2. (a) AFM topograph of InAs nanowire and Ti/Al source and drain Ohmic contacts. [(b)–(f)] SGM images of nanowire current for tip bias voltages of –4, –2, 0, and +4 V, all obtained for $V_{ds} = +0.3$ V. The gray scale corresponds to 4.12 μA (dark) to 4.47 μA (bright).

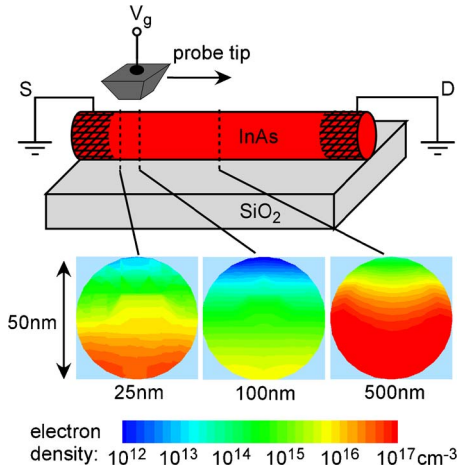

FIG. 3. (Color online) Schematic diagram of probe tip and nanowire geometry and biasing arrangement employed in numerical simulations, and of computed electron density profiles, shown within the nanowire cross section, directly below the probe tip with the tip positioned 25, 100, and 500 nm from the source (*S*) contact.

(bright contrast). In all the SGM images, we also observe that the nanowire current modulation is greatest near the edges of the nanowire, rather than directly atop the nanowire axis. We attribute this effect to a combination of the increase in effective tip-sample contact area in the former position, and the possibility that the insulating SiO_2 layer is thinner on the sides of the wire than on top.

We also observe in Fig. 2 that at both positive and negative tip biases, carrier modulation is stronger when the tip is near the source and drain contacts, and diminishes toward the midpoint between the two. The strongest current modulation occurs when the probe tip is approximately 100–200 nm from the contacts. This suggests that, as the distance between the probe tip (gate) and a macroscopic wire contact is reduced, the total gate capacitance, and consequently the degree of carrier modulation in the wire, increases as well. This behavior is highly plausible, as the electric field within the nanowire arising from the potential difference between the probe tip and the macroscopic contact should increase as the lateral tip-contact separation becomes sufficiently small.

To verify this explanation, we have conducted numerical simulations using ISE simulation software[15] of an InAs nanowire 50 nm in diameter with metal contacts separated by a nanowire length of 1 μm. A donor concentration of 5×10^{16} cm^{-3} is assumed, with an additional donor density of 1×10^{18} cm^{-3} introduced within a 5 nm thick shell at the nanowire surface to simulate the effect of the InAs surface accumulation layer.[14] A conducting probe tip in the shape of a truncated pyramid with a tip size of 30 nm at its apex is positioned 20 nm above the nanowire, and the electron density within the nanowire is computed for a tip bias voltage $V_g = -5$ V as a function of tip distance from the source contact. Shown in Fig. 3 are a schematic diagram of the simulation geometry, and cross-sectional plots of the computed electron density within the nanowire directly below the probe tip, with the tip positioned 25, 100, and 500 nm from the source contact. We see that depletion of electrons within the nanowire is indeed stronger at a tip position ~100 nm from the contact compared to that when the tip is at the nanowire midpoint. In addition, carrier modulation in the

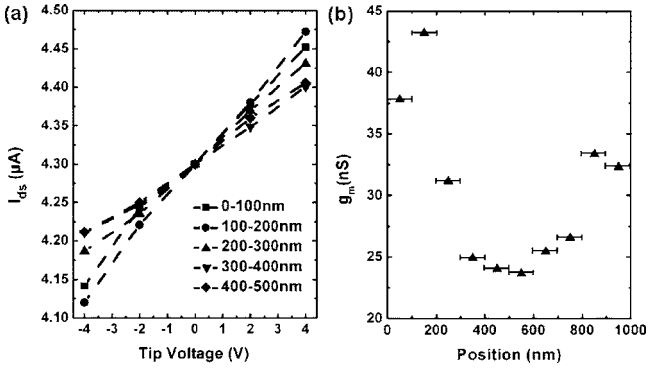

FIG. 4. (a) Nanowire current I_{ds} vs V_g for tip-source contact distance shown in 100 nm intervals, for positions from the source contact to the nanowire midpoint. (b) Transconductance g_m as a function of tip-source contact distance, for a device with source-drain separation of 1 μm.

nanowire is reduced very close to the source contact, due to screening of the tip voltage by the metal contact.Thus, we would expect modulation of current flow through the nanowire by the probe tip to be greatest near the source and drain contacts, least near the midpoint between these, and also reduced at probe tip-contact distances comparable to the tip radius—expected in these studies to be ~20–50 nm. These are precisely the behaviors observed experimentally, as shown in Fig. 2.

A more quantitative portrayal of the tip gating effect and its dependence on position is given in Fig. 4. Specifically, Fig. 4(a) shows current data extracted from a series of SGM images as a function of tip bias voltage for several different distances between the tip apex and the source contact. Each point shown is obtained by averaging the measured current in the nanowire over a 100 nm interval along the length of the nanowire, as indicated. The transconductance $g_m \equiv dI_{ds}/dV_g$, corresponding to the slope of each line in Fig. 4(a), is then a measure of the effectiveness of the probe tip in modulating current flow in the nanowire. We see that the transconductance peaks for the interval corresponding to distances of 100–200 nm from the source contact, is slightly lower 0–100 nm from the contact, and decreases steadily as distance to the source increases.

Figure 4(b) shows the transconductance as a function of tip distance from the source contact, confirming the trend revealed in Fig. 4(a) and showing the corresponding increase in g_m as the tip approaches the drain contact, located approximately 1 μm from the source contact. We see that g_m increases by 80%–90% as the tip moves from the midpoint between the source and drain contacts to 100–200 nm from the source contact. It should be noted that the quantitative values obtained here are specific to InAs nanowires ~45–50 nm in diameter, as the detailed electrostatic behavior of the probe tip-nanowire system and carrier transport characteristics within the nanowire are expected to be diameter dependent. Furthermore, we observe that, the maximum transconductance attained near the drain contact appears to be lower than near the source contact. This behavior is evident from both the plot in Fig. 4(b) and the images shown in Fig. 2. The simple capacitance model discussed above does not account for this behavior; however, it is a possible that near the source contact, modulation of the nanowire potential by the probe tip strongly modulates the barrier for injection of electrons from the metal contact, while near the drain contact, carriers accelerated by the channel potential created by V_{ds} are less likely to be strongly affected by the additional potential modulation induced by the probe tip. Similar behavior has been observed in SGM studies of carbon nanotubes.[16] An additional possibility is that modulation of carriers that may undergo ballistic or near-ballistic transport within 100–200 nm of the source contact,[17] could lead to increased transconductance relative to modulation of carriers undergoing conventional drift-diffusion motion.

In summary, we have used scanning gate microscopy to characterize modulation of current flow in a 45 nm diameter InAs semiconductor nanowire by a gate contact as a function of the gate voltage and position. As expected, we observe electron depletion and reduced current flow for negative gate bias voltages, and electron accumulation with corresponding increased current flow for positive gate bias. In addition, we find that modulation of current flow is strongest when the gate is positioned approximately 100–200 nm from either the source or the drain contact, with the effect being slightly larger near the source contact. Indeed, a variation in transconductance up to 80%–90% is observed as the gate contact is moved from the midpoint between the source and drain contacts to the point of maximum current modulation near the source. This behavior can be interpreted via numerical simulation of the probe tip-nanowire-contact structure. We expect that these observations should contribute to the understanding of carrier transport behavior at the nanoscale, and the design of highly scaled nanowire-based devices.

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[1] L. Samuelson, M. T. Bjork, K. Deppert, M. Larsson, B. J. Ohlsson, N. Paneva, A. I. Persson, N. Skold, C. Thelander, and L. R. Wallenberg, Physica E (Amsterdam) **21**, 560 (2004).
[2] D. D. Ma, C. S. Lee, F. C. K. Au, S. Y. Tong, and S. T. Lee, Science **299**, 1874 (2003).
[3] C. Thelander, T. Martensson, M. T. Bjork, B. J. Ohlsson, M. W. Larsson, L. R. Wallenberg, and L. Samuelson, Appl. Phys. Lett. **83**, 2052 (2003).
[4] M. H. Huang, S. Mao, H. Feick, H. Yan, Y. Wu, H. Kind, E. Weber, R. Russo, and P. Yang, Science **292**, 1897 (2002).
[5] F. Qian, S. Gradecak, Y. Li, C. Wen, and C. M. Lieber, Nano Lett. **5**, 2287 (2005).
[6] X. Duan, Y. Huang, R. Agarwal, and C. M. Lieber, Nature (London) **421**, 241 (2003).
[7] Q. Wang, A. Javey, R. Tu, H. Dai, H. Kim, P. Mclntyre, T. Krishnamohan, and K. Saraswat, Appl. Phys. Lett. **83**, 2432 (2003).
[8] J. Xiang, W. Lu, Y. Hu, Y. Wu, H. Yan, and C. M. Lieber, Nature (London) **441**, 489 (2006).
[9] S. Jin, D. Whang, M. C. McAlpine, R. S. Friedman, Y. Wu, and C. M. Lieber, Nano Lett. **4**, 915 (2004).
[10] Y. Doh, J. A. van Dam, A. L. Roest, E. P. A. M. Bakkers, L. P. Kouwenhoven, and S. D. Franceschi, Science **309**, 272 (2005).
[11] S. Dayeh, D. Aplin, X. Zhou, P. K. L. Yu, E. T. Yu, and D. Wang, Small **3**, 326 (2007).
[12] M. A. Topinka, B. J. LeRoy, S. E. J. Shaw, E. J. Heller, R. M. Westervelt, K. D. Maranowski, and A. C. Gossard, Science **289**, 2323 (2000).
[13] A. Bachtold, M. S. Fuhrer, S. Plyasunov, M. Forero, E. H. Anderson, A. Zettl, and Paul L. McEuen, Phys. Rev. Lett. **84**, 6082 (2000).
[14] C. A. Mead and W. G. Spitzer, Phys. Rev. Lett. **10**, 471 (1963).
[15] Integrated Systems Engineering (ISE), Technology CAD (TCAD) software products, covering processing, device modeling, circuit and systems simulation, up to package simulation.
[16] M. Freitag, Y. Zhou, A. T. Johnson, and W. F. Smith, Appl. Phys. Lett. **79**, 3326 (2001).
[17] X. Zhou, S. A. Dayeh, D. Aplin, D. Wang, and E. T. Yu, Appl. Phys. Lett. **89**, 053113 (2006).