Axial bandgap engineering in germanium-silicon heterostructured nanowires

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Large composition changes along the nanowire axial direction provide an additional degree of freedom for tailoring charge transport in semiconductor devices. We utilize 100% axial composition modulated germanium to silicon semiconductor nanowires to demonstrate bandgap-engineered Schottky barrier heterostructured field-effect transistors that outperform their homogenous counterparts. The built-in electric field in the channel provided by the compositional change and asymmetric Schottky barrier heights enables high carrier injection in one transport direction but not the other, resulting in high on-currents of 50 μA/μm, 10^7 I_{on}/I_{off} ratios, and no ambipolarity in transfer characteristics. © *2011 American Institute of Physics*. [doi:10.1063/1.3634050]

One compelling aspect of the vapor-liquid-solid (VLS) approach is the ability to modulate doping and composition along the length of the nanowire (NW) during its layer-by-layer growth. This control of material composition along the NW axis enables energy band-edge engineering for additional control over charge transport.[1] Compositionally, heterostructured field effect transistor (FET) devices present opportunities to simultaneously achieve high on-currents, reduced off-currents, and steep inverse subthreshold slopes.[2,3] Due to differences in precursor decomposition and growth temperatures for Ge and Si NWs,[4] the composition modulation in VLS grown Ge/Si axial heterostructures has been typically limited to less than ~30%.[5,6] While abrupt Ge-Si heterostructure NWs were demonstrated using a solid Au-Al alloy as growth seed,[7] the very short heterostructured segments for the second, much slower solid phase part of the growth (~3 nm Ge segment) as well as radial over-coating of the first segment limits their suitability for device applications.

We have developed a growth process that allows the synthesis of 100% composition modulation in Ge-Si heterostructure nanowires using VLS growth and provides individual segment lengths that are suitable for device fabrication.[8] To demonstrate the opportunities enabled by such compositional modulation along the transport direction, we introduce a device architecture for semiconductor NWs that, unlike tunnel FETs (TFETs),[9–11] transfers the active portion of the device from the less abrupt Ge-Si heterostructure interface within the NW to the abrupt metal-semiconductor interfaces at the NW ends. This approach removes the device requirement of a sharp Ge-Si hetero-interface and instead exploits the different injection/collection barrier heights and built-in electric field in the channel provided by the compositional change, enabling high carrier injection in one transport direction but not the other. Using this approach, we demonstrate NW heterostructure transistor characteristics that are better than those obtained from transistors made on individual homogenous segments, exhibiting high on-currents, high on/off ratios, and no ambipolarity in transfer characteristics.

Figure 1(a) shows a high angle annular dark field (HAADF) scanning tunneling electron microscope (STEM) image and elemental composition maps of a Au seeded VLS grown Ge-Si axial NW heterostructure with 30 nm diameter Si segment and 80 nm diameter Ge segment. The composition change from 10% to 90% deduced from Si-K signal is ~60 nm for the 30 nm diameter NW (Fig. 1(b)), with no noticeable Si over-coating on the Ge segment of the NW (Fig. 1(c)). The Ge tail is due to the finite Ge solubility in the liquid Au seed which acts as a reservoir from which the Ge is released during the initial growth of the Si segment, resulting in a graded Ge-Si interface.[4] The graded hetero-interface however does not prohibit exploiting the full band-offsets with the contacts on each side of the interface for bandgap-engineered devices.

The NW devices were grown by an all *in situ* process with a p^+ doped Ge NW shell ($N_A \sim 10^{19}$ cm^{-3}) on i-Ge core, followed by an undoped axial Si segment and then heterostructure Schottky barrier FETs (H-SBFETs) were fabricated. The i-Ge core was grown at a temperature of 280 °C and GeH_4 partial pressure, $P_i[GeH_4] = 0.6$ Torr, after which the p^+ doped shell was grown during the temperature ramp up to 400 °C with $P_i[GeH_4] = 0.5$ Torr and $P_i[B_2H_6] = 0.11$ mTorr. The Si segment was grown at ~430 °C with $P_i[SiH_4] = 1.4$ Torr. These heterostructured NWs often exhibit a kink in the Si segment, which is associated with a $\Sigma 3$ (111) coherent twin boundary (TB) that runs along the axis of the Si segment.[8] Such TBs are known to have no influence on the electronic properties of semiconductor materials,[12] which is evident in our case by the complete turn-off of FET devices fabricated on Si segments with TBs. At slower growth rates (pressure reduced to 0.84 Torr), the kinking can be further reduced; and the corresponding single crystalline interface between Ge and Si for an unkinked heterostructure is shown in Fig. 1(d).

Ni source and drain contacts were deposited without thermal treatment followed by a plasma enhanced CVD

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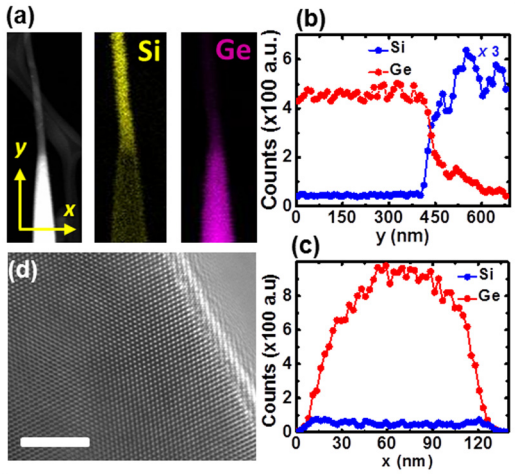

FIG. 1. (Color online) (a) HAADF-STEM image and elemental maps of a Ge-Si axial NW heterostructure with 30 nm diameter Si segment and 80 nm diameter Ge segment. (b) Energy dispersive spectral (EDS) line scan along the length of the wire in (a) showing transition from pure Ge to pure Si. The linear variation in thickness in the tapered pure Ge segment has been corrected for the Ge-L EDS signal. (c) EDS line scan across the diameter of the Ge segment showing no Si radial deposition on the Ge sidewalls during growth of the Si segment. (d) HRTEM at the Ge to Si transition region (scale bar is 5 nm).

10 nm SiN_x gate dielectric layer ($\epsilon_r \sim 2$–3; equivalent oxide thickness of ~13–20 nm) and Ti/Au top-gate electrode. Overlap between the gate and either the source or drain was avoided to eliminate gate leakage currents. In the case of no gate overlap, the gate leakage current was of the order of a few pA for the devices presented here. Ni is known to result in different hole barrier heights of ~0.4 eV for Si and ~0.15 eV for Ge.[13] Structures were initially fabricated on the individual Si and Ge segments to establish their FET characteristics. Contacts made only to the Si NW segment show rectifying behavior in their output characteristics (Fig. 2(c)) and ambipolar behavior in their transfer characteristics (Fig. 2(a)) as expected, with higher current at negative gate voltages compared to positive gate voltages (due to a smaller hole barrier than electron barrier, Figs. 3(c) and 3(e)). For the Ge NW, the doping and channel currents are high (Figs. 2(a) and 2(b)) and thus there is no current modulation over a large gate bias range, indicating no modulation of the channel or the thin barrier at the Ni-Ge contacts which displays ohmic-like behavior (Fig. 2(b)).

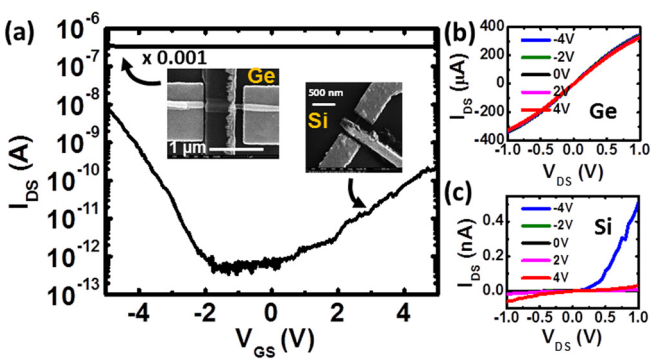

FIG. 2. (Color online) Transfer curves at $V_{SD} = 1$ V (a) and output characteristics (b), (c) of reference Si and Ge NW devices (SEM images are shown inset).

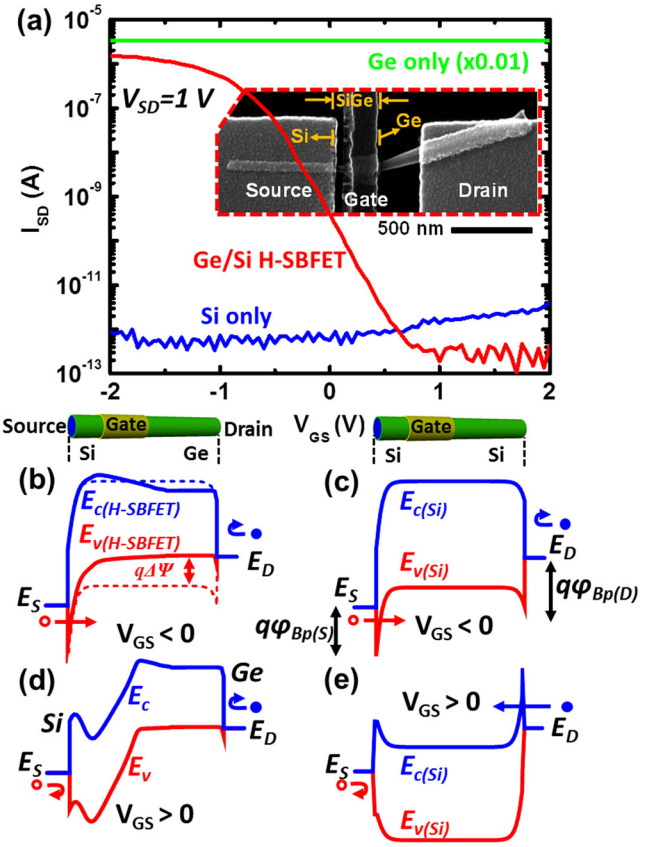

FIG. 3. (Color online) (a) Transfer curves of a p^+ Ge–Si NW heterostructure Schottky barrier FET showing 10^7 I_{on}/I_{off} ratio. Inset is an SEM image of the device with a source-gate spacing of ~40 nm, gate length of ~200 nm, and gate-drain spacing of ~260 nm ($V_{SD} = 1$ V). Transfer curves of homogenous Ge and Si devices are shown for reference. (b) and (d) simulated energy band-edge diagrams, extracted from the center of the NW channel, illustrating H-SBFET device operation where V_S is applied to the Si side (left, labeled as source) using the same gate configuration as in (a). Dotted band-diagram corresponds to that of a homogenous Si channel illustrating reduced potential for a Ge drain compared to a Si drain. (c) and (e) Similar to (b), (d), but for a homogenous Si channel illustrating lower field in the channel in (c) compared to (b) and therefore the lower drive currents for Si SBFET compared to the Ge-Si H-SBFET.

In contrast, a Si-Ge heterostructure NW device exhibits a seven orders of magnitude current modulation for the same source-drain bias voltage (Fig. 3(a)). All three devices (Si, Ge, and Si-Ge) have ungated channel regions to minimize the contribution of gate leakage current to I_{SD}. The maximum on-current for the device shown in Fig. 3 is 50 μA/μm at $V_{SD} = 1$ V with no ambipolar behavior and 10^7 I_{on}/I_{off} ratio, and with a nearly constant inverse subthreshold slope of ~200 mV/decade for different V_{SD} biases. The high on-current observed in the Ge-Si heterostructure compared to that of the homogeneous Si devices (Fig. 2) results from the graded valence band in the Si to Ge transition which provides an additional field that can assist hole injection at the Si source. The band diagrams in Fig. 3 for the H-SBFET (b) and (d) and for a uniform Si channel (c) and (e) are extracted from Silvaco Atlas 3D Poisson solutions for the device structures shown as top panels (b) and (c) in Fig. 3 with the same dimensions, composition, and doping to those used in our experiment. The magnitude of the total potential drop across the valence band at the edges of the source and drain can be expressed as

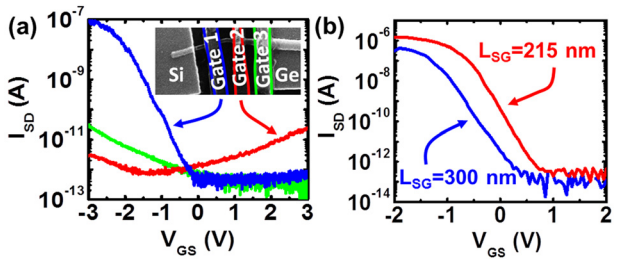

FIG. 4. (Color online) (a) SEM image shows multiple-gate device on a single Ge-Si axial NW heterostructure. Transfer curves with V_D applied to the Si side and gate voltage applied to gates 1, 2, and 3. Current modulation as function of V_{GS} is strong near the Si side of the device (gate 1), and is weak on the Ge side of the device (gates 2 and 3). (b) Transfer curves for Ge-Si devices with two different source-gate distances.

$$|E_{v(S)} - E_{v(D)}|/q = V_{SD} + \Delta E_{(Ge-Si)}/q + \varphi_{Bp(S)} - \varphi_{Bp(D)}, \quad (1)$$

where V_{SD} is the applied source-drain voltage, $\Delta E_{v(Ge\text{-}Si)} \sim 0.57$ eV is the valence band offset between Ge and Si for a (111) surface,[14] $\varphi_{Bp(S)}$ is the hole barrier height at the source side of the device, and $\varphi_{Bp(D)}$ is the hole barrier height at the drain side of the device. This potential drop is valid irrespective of the nature of doping in the channel which determines the profile of the valence band. For the case of a homogenous Si device (ignoring series resistances), $|E_{v(S)} - E_{v(D)}|/q = V_{SD}$, whereas for a device with Si source and Ge drain with Ni contact barriers, $|E_{v(S)} - E_{v(D)}|/q = V_{SD} + 0.82$ V. This added potential drop in the valence band exceeds what can be applied through a homogenous Si material and is enhanced by the choice of the different barrier heights at both terminals of the device $(\varphi_{Bp(S)} - \varphi_{Bp(D)}) > 0$, and leads therefore to the enhanced on-currents compared to the homogenous Si NW SBFET. The presence of the highly doped Ge drain enhances this potential drop further by reducing the potential near the Ge drain and making the contact electrically transparent. We note that a highly doped Si drain would not be as effective in lowering the potential in the NW near the drain compared to the highly doped Ge drain. The simulated band-diagrams in Fig. 3 illustrate the difference in operation between the Ge-Si NW H-SBFET and the Si SBFET. The larger hole barrier height of Si compared to Ge near the drain imposes a negative slope of the valence band near the drain which in turn leads to a backward field that opposes hole transport toward the drain. The increased channel potential and backward field near the drain reduces I_{on} for the Si channel compared to the heterostructured one. The interpretation of a gated Schottky barrier heterostructure FET is supported by another device with multiple gates placed along the channel of the Ge-Si axial NW heterostructure where transconductance is shown to be maximal for the gate placed on the Si segment of the device near the Ni contact (Fig. 4(a)). In addition, based on our H-SBFET interpretation of the barrier modulation at the Si source, the gate field and therefore the measured on-current should be reduced as the source-gate (L_{SG}) spacing increases, and this effect is observed experimentally and shown for two devices in Fig. 4(b).

Our Ge-Si heterostructure NWs add the important ability to accommodate band-offsets and built-in electric fields in the conduction or valence bands, separately at the source or drain sides of the SBFET, by proper selection of metal-semiconductor barrier heights with the metal contacts. This is in dramatic contrast to symmetric Schottky barrier FET devices on Ge,[15] Si,[16] or asymmetric Schottky TFETs,[17] all of which show high leakage currents in the off state. Further, asymmetric p^+-Si—i-Si Schottky TFETs were found to have reduced off-currents but not enhanced on-currents, as is available from our graded H-SBFET.[17] Device results presented here utilize asymmetric barrier heights on the two ends of the Ge-Si heterostructure NW along with the built-in electric field to achieve enhanced performance in Schottky barrier field effect transistors. Such heterostructured NWs expand the available range of advanced architectures for next generation semiconductor devices.

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