Radial heterostructured nanowires offer the possibility of engineering surface effects, strain, energy band-edge, and modulation-doping of one-dimensional structures with unprecedented control for novel electronic and optoelectronic devices. However, synthesis of germanium/silicon (Ge/Si) core/shell nanowire heterostructures is typically accompanied by unwanted gold (Au) diffusion on the nanowire sidewalls, resulting in rough surface morphology, undesired whisker growth, and detrimental performance of electronic devices. Here, we provide new understanding of this Au diffusion on nanowires and report a novel growth procedure allowing in-situ synthesis of Ge/Ge and Ge/Si core/multi-shell nanowires by engineering a blocking growth interface between the growth-mediating Au seed and the nanowire sidewalls. The result is excellent surface morphology and no Au diffusion, enabling the controlled epitaxy of advanced core/multi-shell nanowires with improved transport
characteristics, as demonstrated by field effect transistors with enhanced on-current performance.

1. Introduction

The formation of high quality epitaxial core/shell materials composed of a semiconducting nanowire (NW) surrounded by one or more single crystal shells offers the opportunity for new control of charge transport in nanostructures.\(^1\) By forming shells of different materials and interfaces\(^2\) or electrical conduction type on NWs, the local strain,\(^3\) quantum size,\(^4\) and electronic band offset effects\(^5\) can be used to tailor the spatial distribution of charge carriers and achieve novel opto-electronic device properties.\(^6\) For example, an intrinsic NW core with a doped inner shell surrounded by a second passivating shell can confine a high density of charge carriers in an outer cylinder for stronger gate control while maintaining lower surface scattering. This precise level of control can allow the formation of high-mobility and high on-current devices for optimal transistor performance. While many NW core/shell materials systems have recently gained interest,\(^7\) NWs based on the Ge/Si system with its 4.1% lattice mismatch are among the most interesting from both technological and basic bandgap engineering perspectives.

While both Si and Ge NWs are readily grown by the vapor-liquid-solid (VLS) method using liquid Au alloy droplets as the catalytic growth medium, the required temperatures for wire or shell growth are quite different (~300°C for Ge and 500°C for Si).\(^12\) This disparity in synthesis temperatures has previously resulted in highly detrimental Au diffusion when growing shells at higher temperature, such as for the Ge core/Si shell heterostructures.\(^13\) To inhibit Au diffusion on NW sidewalls, previous approaches have either introduced O\(_2\) during growth\(^14\) or etching of the Au seed ex-situ prior to growing Si shells,\(^15\) both of which
introduce contaminants that adversely affect the NW properties. Here we provide new understanding of this Au diffusion on nanoscale structures and solve the problem by the low temperature formation of a Si barrier segment between the liquid Au catalyst and Ge NW before the shell growth. This novel approach is shown to effectively block the otherwise rapid Au diffusion along the Ge surface at the required shell growth temperatures. We demonstrate through chemical and structural analysis the detrimental consequences of this diffusion without a blocking layer, its nanoscale diameter dependence, and the effectiveness of our solution to this problem. Early studies on the synthesis of Ge/Si core/shell NWs utilized a high temperature ex situ anneal after amorphous Si shell deposition to produce single crystal shells.\cite{7} Based on our new approach, we demonstrate its benefit by the in situ fabrication of single crystalline Ge/Si multi-shell radial heterostructured field effect transistors with and without Au diffusion and show how this approach allows new NW heterostructure designs with significantly improved transconductances and hole mobilities. Our core/ multi-shell design with engineered composition and doping has demonstrated the highest reported maximum on-currents for p-type devices, an aspect of great importance for increased transistor switching speeds.

2. Analysis and Blocking of Au Diffusion on Ge Nanowires

Optimized growth of the Ge NW cores was performed in a two-step temperature process\cite{16} in which the Ge NW growth is initiated near the Au-Ge eutectic point (~ 360 °C) and the temperature was quickly ramped down to ~ 280 °C to reduce material deposition on the NW sidewalls and maintain one dimensional (1D) growth mediated by the liquid Au-Ge catalytic nanoparticles. Figure 1 A-D shows post-growth transmission electron microscope (TEM) images near the tips of different diameter Ge NWs grown using this procedure. For core/shell NW growth, it is generally desired to stop the axial elongation of the NW core and
initiate vapor-solid (thin-film) growth on the NW sidewalls.\cite{17} For this process, the growth temperature has to be raised sufficiently for decomposition of the precursor molecules used for shell deposition and for Si the shell deposition temperature is typically well above the Au-Ge eutectic temperature. As the temperature is ramped up, it is energetically favorable for atomic diffusion of Au from the Au-Ge liquid growth seed to occur along the NW sidewalls (Fig. 1E-H). Note that from Fig. 1A-H, we show that Au diffusion on the Ge NW sidewalls occurs after growth of the Ge NW core during the ramp up to a temperature that is suitable for Si or Ge shell growth, and is to be distinguished from previously reported high temperature or low pressure NW growth conditions where Au diffusion\cite{18,19} can occur concurrently with NW growth. In addition, atomic hydrogen passivation which as been noted to cause de-wetting of Au on Si surfaces\cite{20} doesn’t inhibit Au diffusion on the Ge NW surfaces, as deduced from our temperature ramp experiments to the Si growth temperature in H₂ or GeH₄ ambient where in both cases we observed Au diffusion to still occur.

Since Si surface facets have a higher surface energy than Ge,\cite{21} Au diffusion on the Si surface is expected to be less facile than on the Ge surface. Thus, the introduction of a thin Si layer beneath the Au growth seed is anticipated to create a barrier to the Au diffusion down the Ge NW sidewalls. This Au-NW interface energy difference for the Ge and Si NW surface facets should help to stabilize the Au seed at the NW tip. Deposition of such an interface layer was thus carried out at a low temperature to prevent the onset of Au diffusion along the Ge NW surface. We employ the catalytic effect of the Au nanoparticle to locally decompose SiH₄ at the Ge NW growth temperature (276 °C). When the temperature was ramped to 410 °C, no Au diffusion occurred as depicted in Fig. 1I-L, in dramatic contrast to the situation where no Si interfacial barrier layer was grown (Fig. 1E-H).

To further elucidate and verify the role of the Si interfacial layer in blocking Au diffusion on the Ge NW surface, high angle annular dark field (HAADF) scanning
transmission electron microscopy (STEM) analysis of the 30 nm diameter Ge NWs was performed as shown in Figure 2. For the as-grown NW (Fig. 2A), no Au was observed on the NW sidewalls and energy dispersive x-ray (EDX) spectra ~ 100 nm below the Au seed (marked as point 1 in Fig. 2A) showed only the Ge-L peak (spectrum 1 of Fig. 2D). For the Ge NW that was subject to the 410 °C temperature ramp (Fig. 2B), textured bright dots corresponding to Au nanoparticles on the NW sidewalls are visible and the corresponding EDX spectra showed both Ge-L and Au-M peaks (Fig. 2D, spectrum 2). For the case where a SiH₄ flow was introduced at 276 °C prior to a temperature ramp in vacuum to 410 °C (Fig. 2C), no bright dots were observed on the NW sidewalls, in contrast to the situation in Fig. 2B, and the EDX spectra from the NW sidewalls showed only a Ge-L peak (spectrum 3 of Fig. 2D). EDX spectra taken directly underneath the Au seed for Fig. 2C showed Si-K and Au-M peaks, as expected, supporting the inference that a Si-rich interfacial layer inhibits Au diffusion. Detailed EDX analyses on several other NWs (Fig. S1) have shown that the Au growth seed is Si-rich and that a Si-rich GeSi interfacial layer underneath the Au quickly diminishes to pure Ge, a few 10’s of nm below the Au growth seed.

The complete loss of Au in the case of the smallest Ge NW diameter in Fig. 1E indicates that the Au diffusion on the Ge NW sidewalls is of kinetic origin. To support this argument and further understand the role of the Si blocking layer in eliminating Au diffusion on Ge NW sidewalls, we use the den Hertog et al. kinetic treatment to determine the lowest energy surface for a Au-Ge monolayer to exist at either the NW tip or the NW sidewalls.\[22\] The chemical potential difference $\Delta \mu$ of a monolayer of Au-y eutectic, where $y$ can be either Ge or Si, from the NW surface to its tip can be expressed as:

$$
\Delta \mu = \mu_{\text{Surf}}^{\text{Au-Ge}} - \mu_{\text{Tip}}^{\text{Au-Ge}} = \frac{2 \Omega}{d} \left( \sigma_{\text{Au-Ge}^{(y)}}^{(s_{\text{on}y^{(s)}})} - 2 \sigma_{\text{Au-Ge}^{(y)}}^{(\text{eutectic})} \right) + 4 |\Delta \mu| x_{\text{Au}} \times x_{\text{Ge}}^{(s_{\text{on}y^{(s)}})}, \quad (1)
$$
where $\Omega_{\text{Au}}$ is the atomic volume of Au, $d$ is the NW diameter, $\sigma_{\text{Au-y}^{(1)}}^{s}$ is the surface energy density of a monolayer of liquid Au-y alloy on the solid y NW surface, and $2\sigma_{\text{Au-y}^{(\text{eutectic})}}^{s}$ is the surface energy density of a monolayer of Au-y in the molten growth seed, $\Delta H$ is the enthalpy of mixing of Au and y, and $x_{y}$ is the compositional fraction of y in Au. In equation (1) a negative $\Delta \mu$ implies Au diffusion is energetically favored and arises as the first term, which is negative, and increases at smaller diameters. The Au-Ge and Au-Si temperature-dependent surface energy densities\cite{23} and enthalpies of mixing,\cite{24,25} as well as the diameter-dependent Au seed composition\cite{26} are taken into account in the present case. The addition of the diameter-dependent Au seed composition to the den Hertog model shifts the negative $\Delta \mu$ region for Si to smaller diameters, increasing the stability for Au on Si compared to Ge as shown in Figure 3, consistent with our observed results. We also note that the first term in equation (1) increases rapidly at very small diameters, leading to a negative $\Delta \mu$ and enhanced Au diffusion, consistent with the observed greater loss of Au from the NW tip at smaller diameters as shown for Ge in Fig.1(E-H). It is worth noting that at small diameters, the commonly observed growth orientation is [110] and [211],\cite{27} which typically results partly in lower energy \{111\} facets\cite{28} than the \{110\} facets of [111] oriented NWs. This will also lead to an increased negative $\Delta \mu$ value and rapid Au diffusion for smaller diameter NWs. This analysis combined with the experimental results is consistent with the Au diffusion on the Ge NW sidewalls being of kinetic origin.

Without the use of a Si interfacial barrier layer total loss of Au from the Ge NW tip and diffusion on the NW sidewalls also occurs for the case of larger NW diameters for longer annealing times at the same temperature. For example, a temperature ramp to 410 °C in 5 min followed by cooling to room temperature was observed to result in Au diffusion a distance of ~700 nm down the sidewalls of a 30 nm diameter Ge NW from the Au tip (Figure 4, see also
Fig S3 for higher magnification images), whereas holding the temperature constant at 410 °C for an increased time of 10 min with everything else kept the same resulted in Au diffusion throughout the entire NW length of ~ 2.3 µm (Fig. 4 D-F, see also Fig S4 for higher magnification images). Annealing to different peak temperatures after deposition of the Si layer indicated that the Si interfacial layer can block Au diffusion up to a temperature of ~ 490 °C at which point Au dots begin to appear on the NW surface (Fig. S5).

3. Ge/Ge and Ge/Si Core/Shell Nanowire Growth

The presence of a Si interfacial layer to block Au diffusion has a dramatic effect on the subsequent growth of Ge and Si shells for heterostructured NWs. Such growth of high quality shells allows the realization of radial doped structures which can spatially alter and confine carriers, leading to improved performance of device structures such as enhanced on-currents or reduced surface scattering in NW FETs. In this case, dopant incorporation through controlled shell growth allows conformal and uniform distribution of dopant atoms, unlike the longitudinally non-uniform dopant incorporation during nominal NW growth resulting from mixed VLS and VS dopant deposition.\[29\] Additionally, we suggest these structures could be implemented in high density radial p-n junction Ge-based infrared detectors that benefit from longitudinal energy absorption and radial charge carrier separation and lead to enhanced performance of radial photodetectors, similar to that proposed for radial solar cells.\[30\] Figure 5A-D show TEM images near the center of Ge NWs grown from 10, 30, 50, and 100 nm diameter Au colloids followed by a 2 min Ge shell deposition at a temperature of 410 °C without a Si interfacial barrier layer. Rough NW surface morphology was observed indicative of locally Au-enhanced shell deposition due to Au diffusion on the NW sidewalls. With the addition of the low temperature Si interfacial barrier layer discussed above, the resultant Ge
shell surface is extremely smooth for diameters \( \geq 30 \) nm as shown in Fig. 5E-H. For the smallest diameter NW, Au was not found at the tips of those NWs in Fig. 5A and Fig. 5E indicating loss of Au in both cases (with and without a Si blocking layer) during Ge shell growth, as expected for sufficiently small diameters from equation (1). For the same growth time and temperature, the presence of Au on the NW surface leads to an enhanced growth rate of \( \sim 0.375 \) nm/s (Fig. 5E-H) whereas growth of the Ge shell without the presence of Au on the surface proceeds at a growth rate of \( \sim 0.21 \) nm/s (Fig. 5I-L). Thus, the effect of a monolayer of Au on the surface is to both catalyze faster deposition rates and significantly increase surface roughness. We note that despite the rough surface morphology in the presence of Au, these NW shells maintain single crystal epitaxial growth throughout the core/shell structure (Fig. S6). For the core/shell NW growth with a Si interfacial barrier layer, the shell sidewall growth is smooth and slight axial elongation occurs in conjunction with the radial shell deposition (Fig. S6). These results demonstrate clear evidence of the effectiveness and importance of this growth procedure in inhibiting Au diffusion on the Ge NW sidewalls for the growth of high quality Ge shell layers.

The *in-situ* single-growth technique developed here for Ge/Ge core/shell NWs can also be extended to single crystal Ge/Si core/shell NWs in a single growth run without post-growth chemical or thermal treatment. Since high temperatures and/or low SiH\(_4\) partial pressures have been found to generally induce Au diffusion on Si NWs,\(^{[31]}\) maintaining a SiH\(_4\) partial pressure in addition to the low temperature Si barrier layer was necessary to avoid Au diffusion in the growth of the Si shells. Figure 5 I-K shows a sequence of TEM images of Ge/Si core/shell NWs grown from 10, 30, and 50 nm diameter Au colloids without a Si barrier layer and without maintaining SiH\(_4\) partial pressure during temperature ramp-up, which results in Au diffusion and rough Si shell morphology. With a low temperature Si interfacial barrier layer and a SiH\(_4\) partial pressure of 125 mTorr during temperature ramp up,
Au diffusion on the Ge NW sidewalls was avoided and single crystal Ge/Si core/shell NWs were grown in a single growth run as demonstrated in Fig. 5 L-N. The Si shell thickness was chosen to be $\sim 3$ nm, which is within the coherent critical thickness limit for all Ge core diameters\cite{32} and hence ensures high crystalline quality of the Si shells without misfit dislocations.

4. Radial Bandgap Engineering in core/multi-shell Ge/Si Nanowires

The growth procedure developed here has the advantage of providing multi-shell growth, fully enabling band-gap engineering in the radial direction. The resulting control over the radial distribution of charge carrier densities can further enhance the performance of Ge/Si heterostructures over previous approaches.\cite{33} For instance, an $\text{i-Ge/p}^+\text{-Ge/i-Si core/multi-shell NW heterostructure (Figure 6A)}$ provides larger carrier density near the Ge/Si interface as determined by Silvaco 3D simulations\cite{34} (Fig. 6B) leading to a larger gate capacitance and therefore higher transconductances and on-currents than a uniformly doped $\text{p-Ge/i-Si or i-Ge/i-Si core/shell NWs in heterostructure field-effect transistors (HFETs).}$

To investigate the effects of radial doping profiles on the performance of Ge/Si core/multi-shell HFETs, we employed 3D Silvaco Atlas semi-classical simulations within the framework of the drift-diffusion mode-space method. In this formalism, quantum confinement effects are captured by solving Schrodinger’s equation in the transverse (radial) direction and 1D transport equations are solved for each allowed energy subband. Carrier densities and currents are computed afterwards by integrating over all allowed energy subbands and weighting with the square of the corresponding wave function. Three doping situations were considered: (i) 6 nm i-Ge core/ 1 nm p$^+$-Ge shell ($10^{19}$ cm$^{-3}$)/ 2 nm i-Si shell; (ii) 7 nm p-Ge core ($2.2\times10^{18}$ cm$^{-3}$)/ 2 nm i-Si shell; and (iii) i-Ge core/ i-Si shell. For the doped core/shell
NWs (cases i & ii), the dopant densities were chosen such that the total areal charge density remains constant for direct comparison. A 2 nm Si$_3$N$_4$ gate dielectric was used for all three cases. Surface state effects are not included here and are expected to enhance hole densities in the Ge NW core at the Ge/Si interface and reduce the gate-coupling to the channel such that transconductances over-all will be reduced, and subthreshold slopes and off-currents will increase.[35]

Figure 6C shows the simulated transfer curves for the three situations discussed above. The i-Ge/p$^+$-Ge/i-Si core/multi-shell NW is predicted to result in higher transconductance and on-currents compared to the p-Ge/i-Si case. The i-Ge/i-Si core shell NWs with no doping is seen to result in the lowest transconductance. Such device architectures for multi-shell NWs with designed doping profiles can be grown with our core/shell growth method described here and the resulting on-current performance is found to give improvements over single shell Ge/Si NW HFETs reported previously.[32] Our simulations indicate that too high of Ge-shell doping levels can lead to high $I_{off}$ (Fig. 6D) and show the trade-off between high $I_{on}$ and high $I_{on}/I_{off}$ ratio for optimizing core/shell transistor performance.

5. Enhanced Heterostructure Transistor Performance

To demonstrate the benefits of our growth technique, we compare here the transport properties of i-Ge/p$^+$-Ge/i-Si core/multi-shell NW HFETs grown with and without Au diffusion. Figure 7A shows an oblique-angle scanning electron microscope (SEM) image of an HFET device based on a i-Ge/p$^+$-Ge/i-Si core/multi-shell NW heterostructure. The output curves from 500 nm channel length HFET devices are shown in Fig. 7B. The solid lines are measured from heterostructure NWs with no Au diffusion and the dashed lines are obtained from NWs with Au diffusion present on their surface during the core/shell growth. Transfer
curves for the same devices as well as for 400 nm channel length HFET devices are shown in Fig. 7C. The measured on-currents and transconductances from NW HFETs with no Au diffusion are ~ 2X higher than those measured on NW HFETs with persistent Au diffusion on their sidewalls.

The intrinsic transconductance, $g_m = \mu_h C_g V_{SD} / I_G^2$, where $\mu_h$ is the hole mobility, $C_g$ is the gate capacitance, $V_{SD}$ is the source-drain voltage bias, and $L_G$ is the physical gate length.[36] The mobility-capacitance product can therefore be expressed as

$$\mu_h C_g = I_G^2 \frac{\partial g_m}{\partial V_{SD}}. \quad (2)$$

Thus, the slope of the $g_m$ vs. $V_{SD}$ for the same gate length $L_G$ enables direct comparison of the mobility-capacitance product for the NW devices with and without Au diffusion. Fig. 7D shows a plot of $g_m$ vs. $V_{SD}$ for $L_G=400$ nm and $L_G=500$ nm where the $\mu_h C_g$ product for the case of no Au diffusion is ~ 2X greater than with Au diffusion. The ratio of the gate capacitances (oxide capacitance in series with the Si barrier capacitance), $C_g$ (no-Au)/$C_g$(with-Au), is ~ 1.14.[37] Since the NWs have similar radial dopant profiles, we can conclude that the significant enhancements in transconductances and on-currents for the case of Ge/Si core/multi-shell NW HFETs with no Au diffusion compared to those with Au diffusion are due to an ~ 1.75 X enhancement in the hole mobilities ($\mu_h$). We note that the contact resistances for both types of wires are much lower than the NW channel resistances (see Fig. S7) precluding contact resistance effects in the observed output and transfer characteristics in Fig. 7 and the analysis above. Further, core/shell NWs with Au diffusion have lower contact resistances than those grown without Au diffusion which in turn would lead to higher currents if the mobility for both types of wires were the same, contrary to our experimental observations. The maximum measured current for another device that utilized an $L_G= 400$ nm with a total Ge diameter of 61 nm, was even higher with 122 $\mu$A at $V_{SD} = 0.5$ V (output curves
given in Fig. S8). The normalized on-current corresponding to the physical dimensions of the device and the applied $V_{SD}$ bias can be expressed as $I_{\text{max}}=I_{SD}L_C/\pi d V_{SD}$. This results in a normalized $I_{\text{max}}=509 \ \mu\text{A/V}$, more than two times greater than the earlier best value of 211 \ \mu\text{A/V}.[38] The higher on-currents obtained in our NW multi-shell devices are enabled by the radial shell doping which are shown by simulations (see Fig. 6C) to shift the carrier concentrations closer to the gate compared to previous uniform i-Ge/i-Si core/shell NW approaches (Fig. 6B). To achieve high overall performance of these heterostructure FETs, future studies should use higher dielectric gate insulators, interfaces with lower surface state densities (than the Si/Si$_3$N$_4$ interfaces employed here) and conformal wrap-around gates to simultaneously achieve high $I_{\text{on}}$, low $I_{\text{off}}$ and steeper turn-on characteristics, however this work is beyond the scope of this report.

6. Conclusions

Our new growth procedure utilizes interface engineering to optimize control over the core/multi-shell Ge/Si heterostructure NW synthesis and sheds light on the relevant diffusion kinetics that enhance Au diffusion on NWs at small diameters. The resulting growth-by-design approach can further extend the superior electrostatic control in radial FET device architectures to engineer radial bandgaps and dopant profiles for enhanced transport performance by methods demonstrated here. The controlled epitaxial Si shell growth presented in this work paves the way for new experimental determination of coherent core and shell thicknesses and identification of the types of misfit dislocations that arise in Ge/Si core/shell NWs. It will also enable exploration of the influence of strain on charge transport properties without the introduction of additional variables into NW growth and device processing such as ex situ chemical or thermal treatments.
6. Experimental Section

Growth: Ge and Ge/Si core/multi-shell NW growth was carried out in a cold-wall chemical vapor deposition system using GeH$_4$ (30 % in H$_2$) and SiH$_4$ (50 % in H$_2$) as input precursors and various diameter Au colloids as growth seeds. P-type doping of the Ge shell was achieved with the introduction of B$_2$H$_6$ (100 ppm in H$_2$). The growth of Ge NWs was carried out in a two-temperature step process (366 °C nucleation and 276 °C elongation, 0.6 Torr GeH$_4$ partial pressure) whereas the growth of the Ge shell was performed at ~ 410 °C, 0.15 Torr GeH$_4$ partial pressure and of the Si shell at ~ 500 °C, 1Torr SiH$_4$ partial pressure.

Microscopy: For transmission electron microscope (TEM) analysis, the as-grown NWs were suspended in an isopropanol solution and deposited on Lacey Carbon TEM grids. A JEOL 3000F FEGTEM was used for all HRTEM images and a Tecnai F30 TEM was used for HAADF STEM imaging and EDX analysis. Both TEMs were operated at an accelerating voltage of 300 kV.

Device fabrication: The as-grown nanowires were suspended in an isopropanol solution and then drop-cast onto a SiO$_2$/Si surface prepared with a pre-patterned grid for position mapping. Subsequent e-beam lithography using a JEOL JBX-6300FS system operated at 100 keV, and e-beam evaporation were performed to deposit Ni contact electrodes. Low stress 10 nm SiN$_x$ gate dielectric was deposited by plasma enhanced chemical vapor deposition (PECVD). A second e-beam lithography step was performed to pattern the gate electrode and a Ti/Au metal gate was evaporated followed by lift-off. An Agilent B1500B parameter analyzer was used for transport measurements.
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References:

[37] The i-Ge/p+-Ge/i-Si has a radial thickness of ~ 19nm/3nm/2.5nm for the NW with no Au diffusion and ~ 16.5nm/3nm/6nm for the NW with Au diffusion. In each case the gate dielectric was a 10 nm thick Si$_3$N$_4$ PECVD layer with dielectric constant ~ 3-4. The ratio of the gate capacitance (oxide capacitance) of the NW HFET with no Au diffusion to that with Au diffusion is ~ 1.14.

Figure 1. TEM images and morphology of different diameter Ge NWs demonstrating inhibition of Au diffusion. (A) – (D) TEM images of Ge NWs grown at 276 °C from 10, 30, 50 and 100 nm Au nanoparticles, respectively. No Au diffusion is observed under such growth conditions. (E) – (H) TEM images of Ge NWs grown at 276 °C and subject to a temperature ramp-up to 410 °C; Au diffusion is evident throughout all diameters with total loss of Au nanoparticle for the smallest diameter in (E), and relocation of Au nanoparticle for the 30 nm diameter NW in (F). (I) – (L) same as in (E) – (H), however, with a Si blocking layer deposited at only 276 °C utilizing the Au catalytic effect for SiH4 decomposition. The Au nanoparticle is favored energetically to remain on top of the Si NW segment for the same temperatures used in (E) – (H), illustrating the effectiveness of Si in blocking Au diffusion. Note that the volumes of the Au nanoparticles in (I) – (L) are similar to those in (A) – (D), unlike (E) – (H) where Au diffusion reduces the total Au nanoparticle volume.
Figure 2. HAADF STEM images of 30 nm diameter Ge NWs and corresponding EDX spectra. (A) – (C) STEM micrographs of (A) as-grown Ge NWs at a temperature of 276 °C showing the Au nanoparticle only at the tip, (B) similar NWs heated to 410 °C after growth resulting in Au seed relocation and Au diffusion on the NW sidewalls (textured surface of bright dots), and (C) similar NWs after first depositing a Si interfacial layer at 276 °C after NW growth, then followed by temperature ramp-up to 410 °C in vacuum; no Au diffusion is observed. (D) Normalized EDX spectra at points marked in (A – C) showing in spectra 1 no
Au detected in the as-grown NW of (A), Au detected in spectra 2 with post growth temperature ramp of (B), no Au detection in spectra 3 of the Ge NW with the Si interfacial layer of (C), and Si and Au detection in spectra 4 in the segment directly under the Au seed of (C) illustrating that the Si-rich blocking layer prevents Au diffusion on the Ge NW sidewalls.

**Figure 3.** Comparison of Au-diffusion preference on Ge and on Si NW sidewalls according to equation (1). The predicted onset for Au diffusion (negative $\Delta\mu$) for Au-Ge on Ge occurs at a larger diameter than that for the onset of Au diffusion on Si.
Figure 4. TEM Characterization of Au diffusion on a 30 nm diameter Ge NW with a temperature ramp to 410 °C followed by Ge shell growth for 50 sec (A, B, C) and NW with a temperature ramp to 410 °C and 10 min anneal at 410 °C followed by Ge shell growth for 50 sec (D, E, F). (A) Low magnification TEM image of the NW. (B) TEM image near the tip of the Ge NW showing rough surface morphology indicating Au diffusion on this portion of the NW. (C) TEM image near the base of the NW segment showing a smooth Ge surface indicating the absence of Au on this portion of the NW. (D) Low magnification TEM image of the NW subject to a 10 min anneal before Ge shell growth. (E) TEM image near the tip segment of the NW and (F) near the base segment of the NW showing rough Ge surface indicating the extension of Au diffusion throughout the whole NW surface.
Figure 5. TEM images and morphology of different diameter Ge/Ge and Ge/Si core/shell NWs with and without the presence of Au. (A) – (D) TEM images of Ge NWs grown from Au colloids of the indicated diameters at 276 °C and subject to temperature ramp up to 410 °C followed by deposition of Ge shells at 410 °C for 2 min. Au diffusion during temperature ramp leads to enhanced local deposition of Ge on the NW sidewalls leading to faceting and rough shell morphology. (E) – (H), same as in (A) – (D) however with a low temperature Si blocking layer step between core and shell growth. The Ge shell growth demonstrates extremely smooth NW morphology for diameters ≥ 30 nm. (I) – (K) TEM images of Ge/Si
core/shell NWs grown at 276/500 ºC from 10, 30 and 50 nm Au colloids, respectively, \textit{without} a low temperature Si barrier layer where a SiH$_4$ partial pressure of 0.25 Torr was introduced only for the Si shell deposition (7 min at 500 ºC) leading to 5 – 7 nm thick Si shells and rough NW surface morphologies. (L) – (N), TEM images of Ge/Si core/shell NWs grown at 276/500 ºC from 10, 30 and 50 nm Au colloids, respectively, \textit{with} a low temperature Si barrier layer and a SiH$_4$ partial pressure of 0.25 Torr during temperature ramp (10 min) and Si shell deposition (7 min) leading to a 3 nm thick single crystal Si shell. Inset in (M) is a magnified image near the wire surface showing (111) lattice fringes extending from the Ge core to the Si shell; the white dotted line marks the Ge/Si interface. Inset in (L) is an EDX line scan across the diameter of a 16 nm diameter Ge/Si core/shell NW.
Figure 6. (A) Illustration of a Ge/Si core/multi-shell NW structure used as an input for Silvaco Atlas 3D simulations. (B) simulations: energy band-edge diagram and free hole density radial distribution for: i) 6nm/1nm/2nm i-Ge core/p⁺-Ge/i-Si with p⁺-Ge=10¹⁹ cm⁻³ (red line), and for ii) 7nm core/2nm radial p-Ge/i-Si with p-Ge=2.2x10¹⁸ cm⁻³ (black dashed line), with similar areal doping densities. Core/multi-shell NWs provide peaks in the charge carrier density near the Ge/Si interface (red line) leading to higher gate capacitances, transconductances, and currents. (C) Simulated transfer curves for the doping scenarios discussed above [i) corresponds to the solid red line, ii) corresponds to the dashed black line, and the dash-dot blue line corresponds to a i-Ge core/ i-Si shell] showing higher on-current, and therefore transconductance, for core/multi-shell approach. (D) \( I_{\text{off}} \) for the core/multi-shell approach as function of Ge-shell acceptor doping density \( (N_A) \) showing a steep increase in the off-current when the Ge-shell doping exceeds \( \sim 10^{19} \text{ cm}^{-3} \).
Figure 7. (A) Oblique-angle SEM image of a Ge/Si core/multi-shell NW HFET. (B) Measured output curves for two devices without (solid lines) and with (dashed lines) Au diffusion both for the same gate voltage steps and same $L_G=500$ nm. (C) Transfer curves of HFET devices with and without Au diffusion on devices with 2 different channel lengths showing higher on-currents and transconductances for the case of no Au diffusion. (D) plot of the transconductance as function of $V_{SD}$, the slope of which gives the mobility-capacitance product, which is $\sim 2X$ higher for the NWs with no Au diffusion.
Table of contents: With a new understanding of Au diffusion on nanowires, a novel growth procedure allowing in-situ synthesis of Ge/Ge and Ge/Si core/multi-shell nanowires in a single growth run without post-growth thermal or chemical treatment is enabled. The result is excellent surface morphology and crystalline core/multi-shell nanowires with advanced bandgap engineering and improved transport characteristics.

TOC Keyword: Heterostructure

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Elimination of Au Diffusion for Advanced Core/Multi-shell Germanium/Silicon Nanowire Heterostructure Transistors

ToC figure

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Supporting Information

1. **Figure S1.** HAADF STEM images and corresponding EDX line scans on a 30 nm diameter Ge NW.

2. **Figure S2.** Effect of incorporation of the diameter-dependent Au seed composition on the chemical potential difference between a monolayer of Au-Si from the NW tip to the NW surface, $\Delta\mu$.

3. **Figure S3 & S4.** High magnification TEM images of Au diffusion on a 30 nm diameter Ge NW with a temperature ramp to 410 °C (S3) and 10 min anneal at 410 °C (S4) followed by Ge shell growth for 50 sec.

4. **Figure S5.** Characterization of the stability of the Au seed on top of a 30 nm diameter Ge NW as a function of temperature.

5. **Figure S6.** SEM and TEM characterization of Ge/Ge core/shell NWs.

6. **Figure S7.** Contact resistance comparison for Ge/Si core/multi-shell NW HFETs with and without Au diffusion.

7. **Figure S8.** Measured output curves of a high current Ge/Si core/multi-shell NW HFET device.
Figure S1. HAADF STEM images and corresponding EDX line scans on a 30 nm diameter Ge NW. (a) STEM micrograph of NW under investigation. (b) STEM image and line scan at the NW tip showing a Si rich region. From bulk phase diagrams, we expect no Ge or Si directly in Au; we expect the Si and Ge signals to appear from a non-uniform hemispherical interface between the Au seed and the Ge NW. (c) STEM image and line scan directly at the Au seed/NW interface showing both Ge and Si signals. (d) STEM image and line scan at ~10 nm below the apparent Au seed/NW interface showing a reduced Si signal that becomes equal to the noise level in the line scan of (e) at ~80 nm below the Au seed/NW interface.
Figure S2. Effect of incorporation of the diameter-dependent Au seed composition on $\Delta \mu$. The chemical potential difference of a Au-Si monolayer between the Si NW sidewalls and the NW tip according to ref. [1] suggests Au diffusion for smaller diameter nanowires. The incorporation of the effect of suppression of the liquidus line for Au-Si nanoparticles increases the last term in equation (1) (main text) and thereby increases the chemical potential barrier to Au diffusion, consistent with experimental observations of ref. [16].
Figure S3. High magnification TEM images of the Ge NW shown in Fig. 3 A-C, (A) at its tip, (B) at the center of Fig. 3B, and (C) at the center of Fig. 3C (lower textured region is from underlying C support), showing close-up view of the roughness and Au dots on the Ge NW.
Figure S4. High magnification TEM images of the Ge NW shown in Fig. 3 D-F, (a) at its tip, (b) at the center of Fig. 3E, and (c) at the center of Fig. 3F, showing close-up view of total loss of Au from the NW tip as well as roughness and Au dots on the Ge NW.
**Figure S5.** Characterization of the stability of the Au seed on top of a 30 nm diameter Ge NW as a function of temperature. (a) Temperature profile of the growth of Ge NWs followed by a low temperature deposition of a Si barrier layer and ramp up to different peak temperatures. (b, c, d, e, f) TEM images near the Ge NW tip for these growths whose temperature profiles are shown in (a). Clear dark contrast (marked by a red arrow) on the NW surface was observed near 490 °C illustrating that the Si interfacial barrier layer withstands Au diffusion up to ~ 490 °C. The low contrast shell on the Ge NW surface is due to carbon deposition at high intensity electron beam irradiation.
Figure S6. SEM and TEM characterization of Ge/Ge core/shell NWs. a, b, c) Oblique-angle SEM images of Ge/Ge core/shell NWs when grown with a Si interfacial barrier layer from 30, 50, and 100 nm diameter Au colloids, respectively. A limited amount of axial elongation of a Ge segment during shell growth continues on top of the NW, however with no Au diffusion and smooth core/shell interface. d, e) TEM images at 200K and 400K magnifications, respectively, of a Ge/Ge core/shell NW grown from 100 nm Au colloid without a Si interfacial barrier layer showing the rough surface morphology and textured dots (Au). The HRTEM in (e) shows a continuum of the (111) lattice fringes to the surface of the Ge shell even in the presence of Au diffusion.
Figure S7. Measured resistances and line fits to infer contact resistances for Ge/Si core/shell NWs with and without Au diffusion. The y-intercept at zero channel length for NWs with Au diffusion occurs at a lower value compared to those grown without Au diffusion, indicating a lower contact resistance for the core/shell NWs with Au diffusion.

Figure S8. Measured output curves on a Ge/Si core/multi-shell HFET device corresponding to the device of Fig. 4 (main text) without Au diffusion. The channel length of this device is $L_G=400$ nm and its Ge diameter is $d=61$ nm.