

# Sharp-Switching CMOS-Compatible Devices with High Current Drive

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## 1. Introduction

During the last few decades, our lives have been changed dramatically by the unprecedented development of electronic devices, which become faster, more portable and less expensive, yet with more integrated functionalities. This progress was all driven by MOSFET downscaling, doubling the integration density of integrated circuits roughly every two years, as embodied in Moore's law.<sup>1</sup>

However, the scaling of the MOSFET is reaching a fundamental limit. The subthreshold swing (SS) of a MOSFET, which is a criterion characterizing the sharpness of the switching from  $I_{OFF}$  to  $I_{ON}$ , is limited by the thermal diffusion between source and drain to a value larger than 60 mV/decade of current at room temperature.<sup>2</sup> This physical limit impedes the scalability of the supply voltage  $V_{DD}$  of the MOSFET. In order to enable further scaling of the  $V_{DD}$ , sharp-switching devices with low SS < 60 mV/dec are of great interest.

Sharp-switching transistors using different operation mechanisms have recently been proposed, such as the tunneling FETs (TFETs)<sup>3</sup> and feedback FETs (FB-FETs).<sup>4</sup> The TFET current is carried by interband tunneling rather than source-drain diffusion, and thus can achieve SS < 60 mV/dec at room temperature.<sup>3,5,6</sup> However, due to the large bandgap  $E_G$  of Si, the  $I_{ON}$  of Si TFETs is typically 3–5 decades lower than that of a comparable MOSFET and the small SS is only obtained over a restricted current range.<sup>3,5-7</sup>

On the other hand, the FB-FET has been demonstrated to possess both extremely sharp switching and a high  $I_{ON}$ .<sup>4,8</sup> The operation of the FB-FET utilizes the positive feedback between carrier flow and injection barriers formed by both positive and negative surface charge densities  $Q_S$  generated in  $Si_3N_4$  spacers

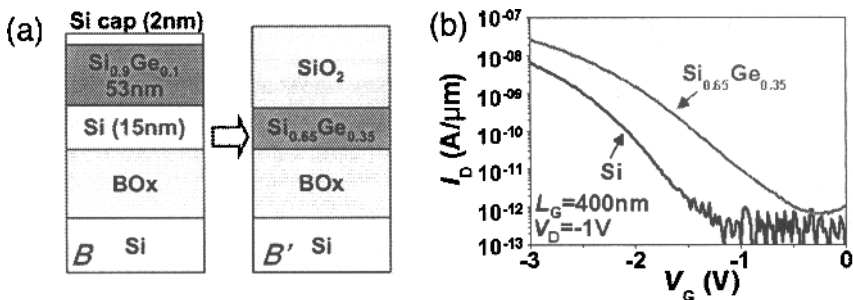
adjacent to the gate. The feedback mechanism makes the threshold voltage  $V_T$  of the FB-FET depend strongly on the surface charge density, which is difficult to control quantitatively. A variant of the FB-FET without surface charge is the field effect diode (FED).<sup>9</sup> The FED uses two adjacent front gates forming the carrier injection barriers to achieve better controllability. The fabrication of FED with two closely adjacent front gates separated by a narrow gap might be a challenge, especially at ultimate CMOS dimensions.

In this chapter, we survey the enhancement of the  $I_{ON}$  in TFETs using  $\text{Si}_{1-x}\text{Ge}_x$  and Ge channels with a lower  $E_G$  and a higher tunneling rate than all-Si devices. Next, a new device named the bipolar-enhanced tunneling FET (BET-FET) combining a TFET with a heterojunction bipolar transistor (HBT) is proposed. The BET-FET features extraordinary simulated performance, with the interband tunneling current serving as a base current that is amplified by the HBT to achieve both low SS and high  $I_{ON}$ . Alternatively, we present a novel, experimentally demonstrated feedback device that we have named the  $Z^2$ -FET (for *zero* subthreshold swing and *zero* impact ionization). The  $Z^2$ -FET offers both high  $I_{ON}$  and abrupt switching. It uses top and bottom gates for forming the carrier injection barriers without recourse to surface charge or the challenging fabrication of two front gates.

## 2. Enhancement of TFET $I_{ON}$ using $\text{Si}_{1-x}\text{Ge}_x$ and Ge channel materials

A TFET is a reverse-biased gated *p-i-n* diode. Interband tunneling occurs at the junction between  $n^+$  (or  $p^+$ ) terminal and the hole (or electron) channel. Thus far, Si TFETs built on SOI substrates have suffered from low  $I_{ON}$ , due to the wide  $E_G \sim 1.1$  eV of Si.<sup>3,5</sup> Materials with lower  $E_G$ , such as  $\text{Si}_{1-x}\text{Ge}_x$ ,<sup>6</sup> pure Ge,<sup>10,11</sup> and III-V semiconductors,<sup>12,13,14</sup> are of great interest to enhance the  $I_{ON}$  of TFETs. Among them,  $\text{Si}_{1-x}\text{Ge}_x$  and Ge are already compatible with Si CMOS.

Figure 1(a) schematically shows the fabrication of  $\text{Si}_{0.65}\text{Ge}_{0.35}$  by the SiGe enrichment process. A 53 nm  $\text{Si}_{0.9}\text{Ge}_{0.1}$  layer is epitaxially grown on the SOI



**Figure 1.** Schematic view of the SiGe enrichment process.<sup>15</sup> (b) Comparison of TFETs with either Si or  $\text{Si}_{0.65}\text{Ge}_{0.35}$  channel. For both of the devices, parameters are  $T_{ox} = 3$  nm  $\text{HfO}_2$ ,  $T_{BOx} = 145$  nm and  $L_G = 400$  nm under  $V_D = -1$  V.

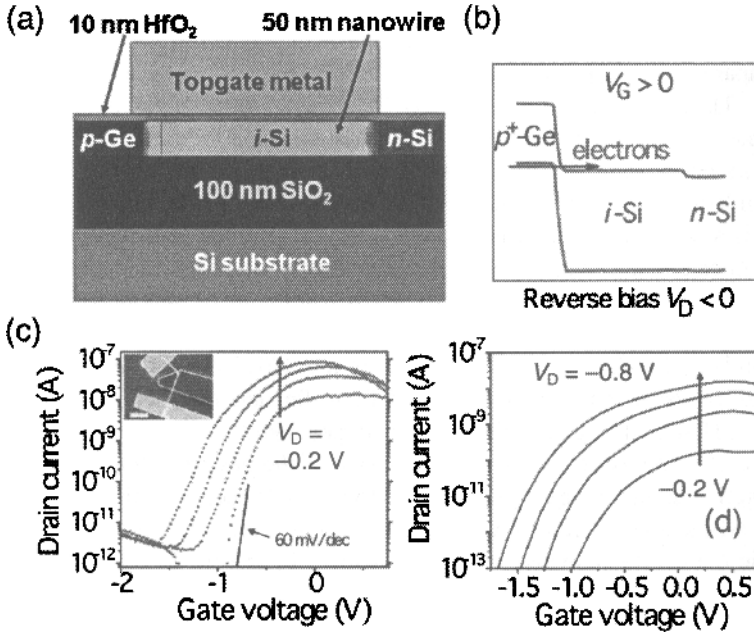
substrate, followed by thermal oxidation to increase the Ge content.<sup>15</sup> A 15 nm strained  $\text{Si}_{0.65}\text{Ge}_{0.35}$  layer is obtained and used as the TFET active layer. Figure 1(b) compares the  $I_D(V_G)$  measurements on TFETs with Si and  $\text{Si}_{0.65}\text{Ge}_{0.35}$  channels. The  $I_{ON}$  is enhanced by using  $\text{Si}_{0.65}\text{Ge}_{0.35}$ , albeit with higher leakage current and degraded SS due to trap-assisted tunneling and thermal generation.

To further increase the  $I_{ON}$ , it is desirable to enrich the Ge content in the channel and enhance the maximum electric field at tunneling junction. One of the solutions is a hetero-nanowire (hetero-NW) channel that can accommodate both a larger compositional change to pure Ge and the tri-gate device geometry with improved electrostatic control.<sup>16</sup> The schematic structure is shown in Fig. 2(a), where the axial  $p\text{-Ge}/i\text{-Si}/n\text{-Si}$  hetero-NW of  $\sim 50$  nm diameter, grown by the vapor-liquid-solid (VLS) method,<sup>17</sup> is used as the TFET channel material. The hetero-NW is placed on an oxide-covered Si wafer and then wrapped on three sides with a 10 nm  $\text{HfO}_2$  gate dielectric and Ni gate metal.

Figure 2(b) shows the energy band diagram of the device in the TFET mode, with a negative drain voltage  $V_D < 0$  applied to the  $p\text{-Ge}$  section with respect to the grounded  $n\text{-Si}$  source. The gate voltage  $V_G$  modulates the  $i\text{-Si}$  channel, as well as the electric field at the tunneling junction. Positive  $V_G$  lowers the conduction band of  $i\text{-Si}$  channel below the  $p\text{-Ge}$  valence band. The electric field at the drain-channel heterojunction, arising from the combination of  $V_G$  and  $V_D$ , promotes interband tunneling current from the Ge valence band in the drain to the  $i\text{-Si}$  conduction band. Tunneling is enhanced by the smaller Ge bandgap – see Fig. 2(b). The gate was positioned to extend over the  $i\text{-Si}$  channel into the  $p\text{-Ge}$  drain region beyond the heterojunction, see inset in Fig. 2(c). The gate overlap ensures that the maximum electric field at positive  $V_G$  lies within the Ge section, maximizing the  $I_{ON}$ .<sup>18</sup> Conversely, when  $V_G$  is negative, holes fill the channel and the tunneling junction shifts to the  $n\text{-Si}$  source, where the tunneling rate is much lower and reduces  $I_{OFF}$ .

Figure 2(c) shows the  $I_D(V_G)$  transfer characteristics of the device at constant  $V_D = -0.2$  to  $-0.8$  V in 0.2 V steps. The maximum  $I_{ON}$  achieved in our device at  $V_G = 0.1$  V and modest  $V_D = -0.8$  V is  $\sim 2$   $\mu\text{A}/\mu\text{m}$  (normalized to the wire diameter), comparable to or higher than that reported for Si NW,<sup>19,20</sup> Ge NW,<sup>21</sup> Ge/SiGe core-shell NW,<sup>22</sup> and the recently reported axial InP/GaAs hetero-NW TFETs.<sup>23</sup> At even higher positive  $V_G$ ,  $I_D$  begins to drop, as the gate voltage depletes carriers in the  $p\text{-Ge}$  section resulting in lower  $E_{MAX}$  at the tunneling heterojunction. Due to the axial heterostructure, ambipolar behavior is suppressed with a very low  $I_{OFF} \sim 10^{-12}$  A (corresponding to  $I_{OFF} \sim 20$  pA/ $\mu\text{m}$ ). The  $I_{ON}/I_{OFF}$  ratio of our devices is  $\sim 10^5$ , with an average subthreshold slope SS  $\sim 140$  mV/decade over 4 decades of current. The best SS, observed over two lowest decades of  $I_D$ , is  $\sim 50$  mV/decade.

Figure 2(d) represents the simulated  $I_D(V_G)$  curves for the structure of Fig. 2(a) using three-dimensional TCAD simulations. The simulations confirm that the current conduction is due to interband tunneling in the region around the Ge/Si heterojunction. Simulated values agree reasonably well with the experimentally measured  $I_{ON}$ , subthreshold slope, the  $I_{ON}/I_{OFF}$  ratio of  $\sim 10^5$ , and the saturation and turnover of  $I_D$  as  $V_G$  approaches 0.5 V.



**Figure 2.** (a) Schematic diagram of the complete top-gated axial SiGe hetero-NW TFET structure with  $p$ -doped Ge drain segment on the left and  $n$ -doped Si source segment on the right of the  $i$ -Si channel; dashed line indicates the  $p$ -Ge/ $i$ -Si junction. (b) Energy band diagram of the device in TFET mode, where  $V_D < 0$  and  $V_G > 0$  floods the channel with electrons, promoting interband tunneling in the Ge drain-channel junction. (c)  $I_D(V_G)$  transfer characteristics at  $V_D = -0.2$  to  $-0.8$  V in 0.2 V steps. At  $V_G = 0.1$  V,  $I_{ON}$  reaches  $\sim 100$  nA ( $\sim 2 \mu\text{A}/\mu\text{m}$  as normalized to NW diameter). Dashed line indicates  $SS = 60$  mV/decade. Inset shows a top-gated device. (d) Simulated  $I_D(V_G)$  characteristics at  $V_D = -0.2$  to  $-0.8$  V in 0.2 V steps, showing reasonable agreement with experimental data.

### 3. Bipolar-enhanced TFET: BET-FET

As discussed above, TFETs based on low  $E_G$  channel materials and multi-gate architectures have been demonstrated with improved  $I_{ON}$ , but still 2–3 decades lower than that of Si MOSFETs. Since the tunneling current is low, can an internal amplification mechanism come to the rescue?

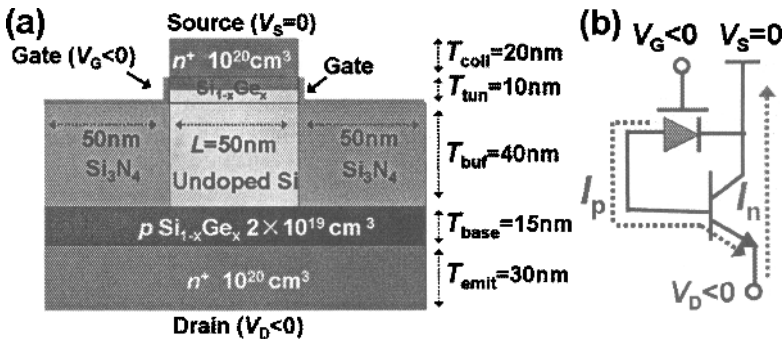
Here, we propose a high-performance device named the bipolar-enhanced tunneling FET (BET-FET), where the Si/Si<sub>1-x</sub>Ge<sub>x</sub> HBT is combined with a gate-controlled tunneling junction. Previously, a multi-emitter HBT with an Esaki tunnel diode supplying the base current had been demonstrated for enhanced logic functionality.<sup>24</sup> In the BET-FET, the tunnel diode base contact is replaced by a TFET region in the reverse-biased collector-base (CB) junction. The tunneling-generated holes flow to the base-emitter (BE) junction, forward-biasing it and leading to effective electron injection from the emitter. Due to the bipolar

amplification, our simulated device shows both high  $I_{ON}$  and low SS over a much wider range of current than a standard TFET.<sup>25</sup>

Figure 3(a) shows the simulated vertical BET-FET device structure, which is symmetrical and has a short sidewall gate close to the source.<sup>26</sup> Both source and drain are heavily  $n^+$ -doped Si ( $10^{20} \text{ cm}^{-3}$ ) and used as collector and emitter, respectively. A  $p^+$ -type  $\text{Si}_{1-x}\text{Ge}_x$  layer with doping concentration of  $2 \times 10^{19} \text{ cm}^{-3}$  is placed above the drain and used as the base, albeit without any direct base contact. The vertical  $n^+$ -Si source/ $p^+$ - $\text{Si}_{1-x}\text{Ge}_x$  base/ $n^+$ -Si drain structure forms an HBT, biased in the conventional way with the source grounded and the drain forward biased ( $V_D < 0$ ). The reverse-biased collector-base junction is used as tunneling junction controlled by the sidewall gates through a 1 nm thick equivalent oxide. The tunneling layer beneath the gate is 10 nm  $\text{Si}_{1-x}\text{Ge}_x$ , of which the upper 5 nm layer is heavily doped. It is separated from the base by an undoped Si buffer layer for reducing the ambipolar tunneling leakage as in optimized TFETs.<sup>27</sup>

The operating principle of the BET-FET is illustrated in Fig. 3(b). In the off-state, at low  $|V_G|$ , there is no tunneling current at the CB tunnel junction and hence no base current, leading to negligible emitter-collector current as in a floating-base HBT.<sup>24</sup> As  $|V_G|$  increases, the hole current ( $I_p$ ) generated in the tunneling CB junction flows to the BE junction and forward biases it, like a standard base current. A high electron current ( $I_n$ ) is then injected from the emitter into the base and subsequently drifts to the collector as in a normal HBT, see Fig. 3(b).

Figure 4(a) shows the  $I_D(V_G)$  characteristics of the BET-FET at  $V_D = -1.5 \text{ V}$  with Ge content  $x = 0.3$  in both base and tunneling layer. For comparison, a conventional vertical TFET with the same tunnel layer structure as in Fig. 3(a) but a  $p^+$ -Si doped drain was also simulated. The difference between the BET-FET and the TFET results from the bipolar amplification, which validates our concept.



**Figure 3.** (a) The simulated device structure has the following layer sequence:  $n^+$ -doped Si collector:  $T_{coll} = 20 \text{ nm}$ ;  $\text{Si}_{1-x}\text{Ge}_x$  tunneling layer:  $T_{tun} = 10 \text{ nm}$  of which 5 nm is  $n^+$ -doped; undoped Si buffer layer:  $T_{buf} = 40 \text{ nm}$ ;  $p$ -doped  $\text{Si}_{1-x}\text{Ge}_x$  base:  $T_{base} = 15 \text{ nm}$ ; and  $n^+$ -doped Si emitter:  $T_{emit} = 30 \text{ nm}$ . The source stripe width  $L = 50 \text{ nm}$ . (b) Equivalent circuit of the BET-FET in the on state, dashed arrows denote hole ( $I_p$ ) and electron ( $I_n$ ) current.

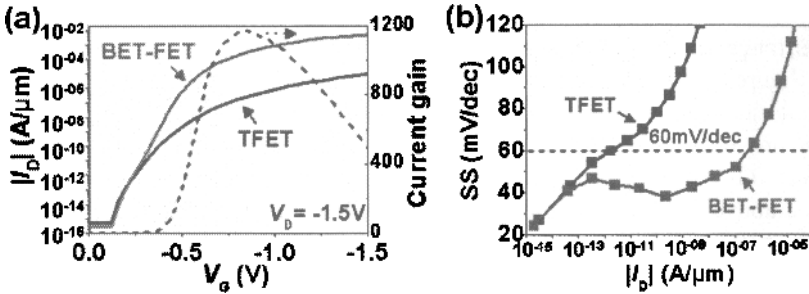


Figure 4. Comparisons of (a) current and (b) subthreshold swing (SS) between BET-FET and conventional TFET. Dashed line in (a) denotes the bipolar current gain that ensures the superior performance of the BET-FET.

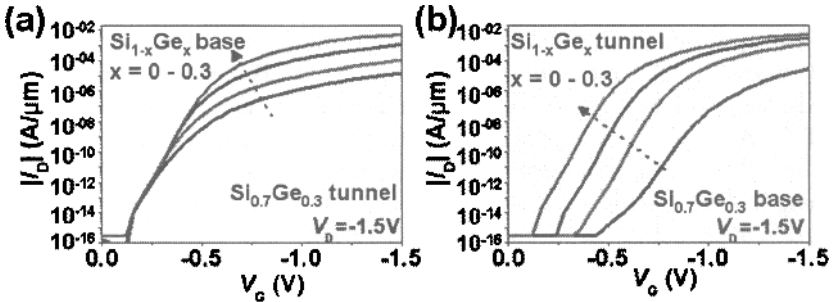
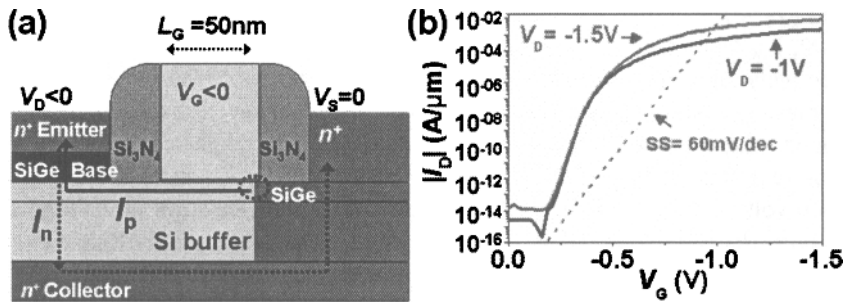


Figure 5. Transfer  $I_D(V_G)$  characteristics of BET-FET vs. Ge content  $x$  in (a) the base ( $x = 0.3$  in the tunneling layer) and (b) tunneling layer ( $x = 0.3$  in the base).

Compared to the standard TFET, the BET-FET has much higher  $I_{ON} > 4 \text{ mA}/\mu\text{m}$  at  $V_G = -1.5 \text{ V}$ . The bipolar current gain of BET-FET is modest under low  $I_D$  due to the carrier recombination in base-emitter junction, and ramps up rapidly as  $I_D$  increases. The highest current gain ( $> 10^3$ ) is achieved at  $I_D \sim 0.1 \text{ mA}/\mu\text{m}$  and then decreases due to high injection, as in a standard HBT. Figure 4(b) compares the SS values in BET-FET and TFET: the conventional TFET exhibits  $SS < 60 \text{ mV/dec}$  over a limited two-decade range of  $I_D$ , the BET-FET has low SS over 7 decades of current.

The superior performance of the BET-FET arises from both the bipolar current gain and the BTBT current, affected by the Ge content  $x$  in  $\text{Si}_{1-x}\text{Ge}_x$  base and tunneling layers, respectively. Figure 5(a) shows that the increase of  $x$  from 0 to 0.3 in the base enhances the current gain and  $I_{ON}$ . Higher Ge content  $x$  in the tunneling layer, on the other hand, increases the tunneling current and reduces the threshold voltage, thanks to the bandgap narrowing, see Fig. 5(b).

Figure 6(a) shows an asymmetric planar BET-FET variant, with a  $\text{Si}/\text{Si}_{0.7}\text{Ge}_{0.3}$  HBT at the drain ( $T_{\text{base}} = 15 \text{ nm}$ ,  $p$ -doped to  $2 \times 10^{19} \text{ cm}^{-3}$ ) and a gate-controlled tunneling junction at the source. The simulated gate length  $L_G$  was 50 nm, with 25 nm nitride spacers, and a 1 nm equivalent gate oxide thickness. The



**Figure 6.** (a) A variant of BET-FET with planar compact layout, showing the tunneling hole and injected electron currents. (b) Simulated  $I_D(V_G)$  curves for  $V_D = -1$  and  $-1.5$  V.

corresponding simulated  $I_D(V_G)$  curves for  $V_D = -1$  and  $-1.5$  V are shown in Fig. 6(b). Again, the device provides high  $I_{ON} > 1$  mA/ $\mu\text{m}$  and  $SS < 60$  mV/dec over a large current range. The same device concept can also be exploited in III-V heterojunctions that are often employed for high-performance HBTs.

#### 4. A feedback-based high-current sharp-switching device: $Z^2$ -FET

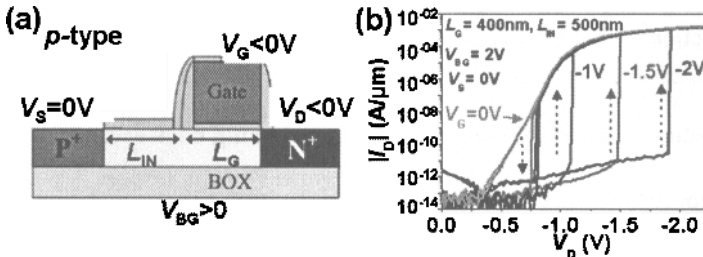
Another route towards CMOS-compatible high-current sharp-switching devices is the use of positive feedback devices, such as thyristors,<sup>2</sup> FB-FETs,<sup>4,8</sup> and multiple-gated FEDs.<sup>9,28</sup> A number of these devices have shown promising performance, with sharp switching and high  $I_{ON}$ , but compact CMOS-compatible versions still face various challenges. Thus, SOI-based compact thyristors using two coupled bipolar transistors triggered by impact ionization are quite temperature-sensitive and require precise doping control in the channel to obtain stable performance.<sup>29</sup> The FB-FET, utilizing the feedback between carrier flows and their injection barriers, does not use impact ionization or channel doping, but suffers from the poor controllability of the surface charge that forms the injection barriers. The FED, though using two front gates instead of surface charge for better controllability, faces challenges in fabricating two adjacent front gates.

Here, we discuss another feedback device with an intrinsic channel, which uses a single front gate and a back gate. The device is named the  $Z^2$ -FET<sup>30</sup> and exhibits ultra-sharp switching (near-zero subthreshold swing), high  $I_{ON}$  at operating voltages below 2 V, and gate-controlled hysteresis in the output characteristic that is potentially useful for compact refreshable capacitorless memories.<sup>31</sup>

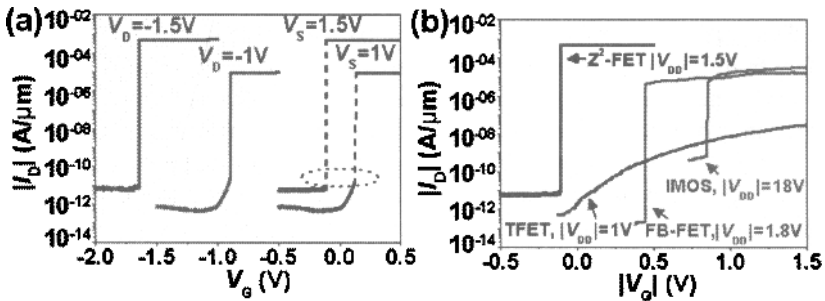
The  $Z^2$ -FET is a forward-biased  $p$ - $i$ - $n$  diode with the intrinsic channel partially covered by the front gate ( $L_G$ ) and the rest ungated ( $L_{IN}$ ), schematically shown in Fig. 7(a). The device has the same layout structure and fabrication process as the asymmetrical TFET used for reducing the ambipolar tunneling leakage current.<sup>27</sup> For the  $p$ -type  $Z^2$ -FET, the  $p^+$  source is grounded and the  $n^+$  drain is negatively

biased ( $V_S = 0$ ,  $V_D < 0$ ). The negatively and positively biased front and back gates ( $V_G < 0$ ,  $V_{BG} > 0$ ) form electron and hole injection barriers in the  $L_G$  and  $L_{IN}$  regions, respectively, blocking or enabling carrier flow in the forward-biased  $p$ - $i$ - $n$  structure. This biasing scheme emulates a virtual  $p/n/p/n$  thyristor even though the body is undoped. Experimental  $I_D(V_D)$  measurements show that the device is initially in a low-current state at low  $|V_D|$  and switches on sharply as  $|V_D|$  increases beyond a turn-on voltage  $|V_{ON}|$ . As  $|V_D|$  is swept back to 0, the device stays in the high  $I_{ON}$  state until  $|V_D|$  decreases below 0.8 V, at which point it turns off. Since  $V_{ON}$  is linearly dependent on  $V_G$ , a large hysteresis is obtained, see Fig. 7(b).

The transfer  $I_D(V_G)$  characteristic also shows sharp switching, where the current increases by 8 decades within a narrow  $\Delta V_G = 1$  mV range at  $V_D = -1.5$  V, see Fig. 8(a). The switching threshold can be tuned by biasing the  $V_D$  with grounded  $V_S$  (solid curves) or  $V_S$  with grounded  $V_D$  (dashed curves). Compared to other sharp-switching devices, such as the FB-FET, TFET, and impact ionization MOS (IMOS),<sup>32</sup> the  $Z^2$ -FET shows superior switching performance under reasonably low  $V_{DD} = 1.5$  V supply voltage, see Fig. 8(b).

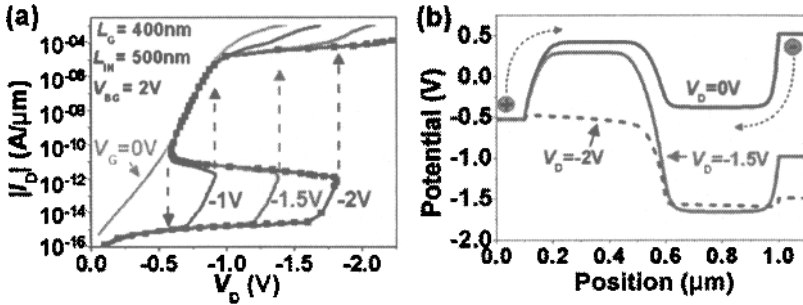


**Figure 7.** Schematic structure of the (a)  $p$ -type  $Z^2$ -FETs operating with backgate voltage  $V_{BG} > 0$ . (b) Its experimental  $I_D(V_D)$  curves show sharp switching and gate-controlled hysteresis. The device parameters are  $T_{ox} = 3$  nm  $\text{HfO}_2$ ,  $T_{Si} = 20$  nm,  $T_{BOX} = 145$  nm,  $L_G = 400$  nm and  $L_{IN} = 500$  nm.<sup>30</sup>



**Figure 8.** (a) Experimental  $I_D(V_G)$  curves of the  $p$ -type  $Z^2$ -FET show sharp switching with subthreshold swing below 1 mV/decade. The  $I_{ON}$  exceeds 500  $\mu\text{A}/\mu\text{m}$  at  $V_D = -1.5$  V. The threshold voltage is determined by the relative biasing of drain and source. (b) Comparison between  $Z^2$ -FET and other reported sharp-switching devices, including the FB-FET,<sup>4</sup> TFET,<sup>6</sup> and IMOS.<sup>32</sup>





**Figure 9.** (a) Simulated  $I_D(V_D)$  curves reproducing the experimental results in Fig. 7(b). (b) Simulated channel potential of device under three different  $V_D = 0, -1.5$ , and  $-2$  V, with constant  $V_G = -2$  V and  $V_{BG} = 2$  V. Arrows indicate the injection of electrons and holes over the relevant barriers.

The  $Z^2$ -FET device operation is most easily appreciated via TCAD simulations. Figure 9(a) shows the simulated  $I_D(V_D)$  curves under different  $V_G$  reproducing the  $p$ -type  $Z^2$ -FET experimental results in Fig. 7(b). Including impact ionization has no effect, as shown by the dots in the  $V_G = -2$  V curve, confirming that the operation of  $Z^2$ -FET does not involve impact ionization.

Figure 9(b) shows the potential in the channel of the device in Fig. 7(a) as a function of  $V_D$  for fixed  $V_G = -2$  V and  $V_{BG} = 2$  V. As  $|V_D|$  is increased, the electron injection barrier  $V_n$  is reduced, increasing injection, until at  $V_D = V_{ON}$  a sufficiently high electron current is injected to reduce the hole barrier  $V_p$ . This, in turn, permits hole injection and establishes the positive feedback, leading the device to switch sharply to the  $I_{ON}$  state. This feedback markedly reduces the electron and hole barriers, as shown in Fig. 9(b) for  $V_D = -2$  V. Once the barriers are collapsed, there is a high-density electron-hole carrier plasma in the channel, leading to high  $I_{ON}$ , as in regular forward-biased  $p$ - $i$ - $n$  diodes. The agreement with experimental data is quite good, see Fig. 7(b).

Our simulations show that, if built in an advanced SOI structure with ultrathin active layer and buried oxide, the  $Z^2$ -FET is scalable down to  $L_G = L_{IN} = 30$  nm.<sup>33</sup> Besides, thanks to the good reliability and gate-controlled hysteresis, the  $Z^2$ -FET has also been used as both single-transistor dynamic random-access-memory (DRAM) and static RAM (SRAM) with high access speed.<sup>31</sup>

## 5. Conclusions

This chapter has covered several CMOS-compatible sharp-switching devices with higher current drive than conventional Si TFETs, that can potentially supplement or replace CMOS FETs for future low-power applications. Thus, TFETs with  $\text{Si}_{0.65}\text{Ge}_{0.35}$  channels have been fabricated on SOI substrates and exhibit  $I_{ON} \sim 10$  times higher than a comparable all-Si TFET, due to the lower bandgap of  $\text{Si}_{0.65}\text{Ge}_{0.35}$ . A further enhancement of the  $I_{ON}$  in TFET has been achieved by

utilizing a tri-gate structure built on Si/Ge heteronanowires to enhance the tunneling electric field. In order to obtain an  $I_{ON}$  competitive with MOSFETs, the BET-FET has been proposed, combining a TFET with an HBT. Thanks to the sharp switching behavior of TFET and high current drive of HBT, the BET-FET exhibits  $SS < 60$  mV/dec over many decades of current and  $I_{ON} > 4$  mA/ $\mu$ m in TCAD simulation. Another new, compact sharp-switching device we have named the  $Z^2$ -FET has been demonstrated experimentally, using a fully CMOS-compatible SOI fabrication process. The  $Z^2$ -FET has simple structure with an intrinsic channel and a single front gate, and shows very high  $I_{ON}/I_{OFF} > 10^8$  ratio and a near-zero subthreshold swing  $SS < 1$  mV/dec. The operation of the  $Z^2$ -FET, as confirmed by TCAD simulations, involves positive feedback between carrier flow and gate-controlled injection barriers, with no need for impact ionization, enabling good temperature stability and reliability. As a result of its good reliability and gate-controlled hysteresis, the  $Z^2$ -FET may find applications in high-speed and compact memories.

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