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Sharp-Switching High-Current Tunneling Devices

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Tunneling FETs (TFETs) offer the possibility of overcoming the 60 mV/dec subthreshold slope limit of conventional transistors and thereby providing sharp-switching logic devices. We discuss two approaches to increasing the current drive of tunneling devices, both implemented in the silicon-germanium heterostructure system. First, the bipolar-enhanced TFET (BET-FET) multiplies the gate-controlled interband tunneling current by the Si/Ge heterojunction bipolar current gain. Both vertical and planar versions have been simulated, with high I_{ON} > 1000 μA/μm accompanying low subthreshold swing over many decades of current. Second, the trigate Si/Ge heteronanowire TFET is based on shifting the tunneling junction from Ge in the on-state to Si in the off-state. Fabricated with a vapor-liquid-solid epitaxial Si/Ge hetero-nanowire channel and high-κ dielectric trigate stack, the proof-of-concept prototype device exhibits reasonable I_{ON}, sub-60 mV/dec slope, as well as surprising backgating properties.

Introduction to Sharp-Switching Tunneling Transistors

For many decades, silicon technology has been driven by MOSFET downscaling, doubling the integration density of integrated circuits roughly every two years, as embodied in Moore's Law (1). In producing manufacturable FETs with gate length L_G < 50 nm, industry has overcome a number of hurdles, including the introduction of new materials, breaching the limits of optical lithography, and recently transitioning from bulk planar to silicon-on-insulator (SOI) or FinFET device architectures (2). However, the scaling of the MOSFET is reaching a fundamental limit. The subthreshold swing (*SS*) of a MOSFET, which is a criterion characterizing the sharpness of the switching from I_{OFF} to I_{ON}, is limited by the thermal diffusion between source and drain to a value larger than 60 mV/dec of current at room temperature (3). This physical limit impedes the scalability of the supply voltage V_{DD} of the MOSFET. In order to enable further scaling of the V_{DD}, sharp-switching devices with low *SS* < 60 mV/dec are of great interest.

Among the various sharp-switching transistors based on different operation mechanisms that have attracted considerable research interest over the past decade is the TFET. The TFET layout is quite similar to the MOSFET but with counter-doped source and drain electrodes. The source-drain current flows by interband tunneling, rather than

source-drain diffusion, with the gate voltage V_G controlling the size of the tunnel barrier, thereby modulating the current. Crucially, since there are no electronic states in the bandgap E_G, the tunneling carrier distribution has no high-energy tail (4) and hence the TFET can achieve $SS < 60$ mV/dec at room temperature. Furthermore, the TFET is well-suited to modern SOI channels (5), since the interband tunneling current is exponentially dependent on the maximum electric field F_{MAX} at the tunneling junction, which occurs near the dielectric/channel interface. Silicon-based TFETs with $SS < 60$ mV/dec have been reported (6, 7), but due to the large bandgap E_G of Si, the I_{ON} of these Si TFETs has typically been orders of magnitude lower than that of modern MOSFETs and insufficient for driving significant circuit loads. Further, the small SS has only obtained over a restricted current range, resulting in a modest I_{ON}/I_{OFF} ratio.

Efforts to enhance the I_{ON} by building TFETs in channel materials with smaller E_G, like $Si_{1-x}Ge_x$ and Ge (7, 8, 9), or III-V heterostructures (10, 11, 12) have met with limited success: it has proven difficult to simultaneously obtain $I_{ON} > 100$ μA/μm (ideally > 1000 μA/μm) and $SS < 60$ mV/dec over more than a couple of decades of current. Device concepts capable of reaching these metrics while retaining genuine compatibility with Si technology are urgently needed.

This paper will discuss two proposed high-current sharp-switching devices: the bipolar-enhanced TFET (BET-FET) and the Si/Ge trigate heteronanowire TFET. In the BET-FET, the V_G-controlled tunneling current is amplified via the current gain in a Si/SiGe heterojunction (13). This leads to a compact device with high simulated $I_{ON} > 10^3$ μA/μm, $SS < 60$ mV/decade over many orders of output current, and a low I_{OFF} as in a floating-base bipolar transistor. As we shall show, several SOI-compatible device variants are possible, including both vertical and lateral current layouts, and simulations show the device to be scalable down to sub-20 nm dimensions. The BET-FET outperforms both conventional MOSFETs and Si TFETs for $0.5\ V < V_{DD} < 1\ V$, but has not yet been demonstrated experimentally. In the Si/Ge trigate heteronanowire TFET (14,15) the I_{ON} is determined by F_{MAX} in the lower bandgap Ge section, while the I_{OFF} is due to the exponentially weaker tunneling in the Si section. Preliminary trigate high-κ insulated prototypes, grown by vapor-liquid-solid (VLS) epitaxy with an abrupt Si/Ge heterojunction, and fabricated via e-beam lithography on an oxide-covered Si substrate, show reasonably high $I_{ON} > 1$ μA/μm at $V_{DD} = 0.8$ V and good SS (< 60 mV/dec, albeit for only 2 decades of current). A fully CMOS-compatible process flow combining VLS epitaxy with vertical gate formation remains to be developed.

Bipolar-Enhanced TFET (BET-FET)

The BET-FET consists of gate-controlled TFET combined with a $Si/Si_{1-x}Ge_x$ HBT in a compact vertical or planar layout. When the TFET is turned on by V_G, the interband tunneling current supplies the base current to the HBT and is multiplied by the usual HBT current gain $\beta > 100$, leading to a high I_{ON}. When the TFET current is off, the HBT base is floating, leading to a negligibly small I_{OFF}. The basic idea is similar to the previously experimentally demonstrated multi-emitter $Si/Si_{1-x}Ge_x$ HBT with no base contact (16), shown in Fig. 1(a). In the multi-emitter HBT, with one of the emitters grounded and the other biased high, one of the heavily-doped emitter-base junctions would pass a small tunnel current in reverse bias, and this tunnel current would act as the

base current for the other, forward-biased emitter-base junctions. As a result, a large output collector current flows, with the tunneling current multiplied by the HBT current gain β. Conversely, with both emitters biased at the same voltage (grounded or high), there would be no base current, leading to a floating base configuration with a very small leakage current. As a result, the multi-emitter HBT provides enhanced logic functionality as a function of two (or more) inputs (16).

In the proposed BET-FET, the tunneling base current is provided by a gated TFET region in the reverse-biased collector-base junction of an *npn* Si/$Si_{1-x}Ge_x$ HBT, as shown in Fig 1(b). When $V_G < 0$ and the TFET is on, the tunneling-generated holes flow to the emitter-base Si/$Si_{1-x}Ge_x$ junction, forward-biasing it and leading to effective electron injection from the emitter. Due to the bipolar amplification, our simulated device shows both high I_{ON} (the TFET current multiplied by the HBT current gain β) and low SS over a much wider range of current than a standard TFET (12).

The parameters of the simulated (17) vertical BET-FET device structure, which is symmetrical and has a short sidewall gate close to the source, are shown in Fig. 1(b). The source and drain are n^+-Si doped 10^{20} cm^{-3} and used as collector and emitter, respectively. A p^+-$Si_{1-x}Ge_x$ layer of 15 nm thickness, doped 2×10^{19} cm^{-3}, is placed above the drain, but is not contacted separately. The vertical n^+-Si source/p^+-$Si_{1-x}Ge_x$ base/n^+-Si drain structure forms an HBT. The source is grounded, the drain is biased conventionally ($V_D < 0$), and there is no base contact as in the multi-emitter HBT. The reverse-biased collector-base junction is used as a TFET controlled by the sidewall gates through a 1 nm thick equivalent oxide. The tunneling layer beneath the gate is 10 nm $Si_{1-x}Ge_x$, of which the upper 5 nm layer is heavily doped. It is separated from the base by a 40 nm thick undoped Si buffer layer for reducing the ambipolar tunneling leakage as in optimized TFETs (18). The total thickness of the strained $Si_{1-x}Ge_x$ layers is 25 nm, below the critical thickness for dislocation formation for Ge content up to $x = 0.3$ (19).

The operating principle of the BET-FET is illustrated in Fig. 1(c). In the off-state, at $V_G = 0$, there is no TFET tunneling current and hence no base current, leading to a negli-

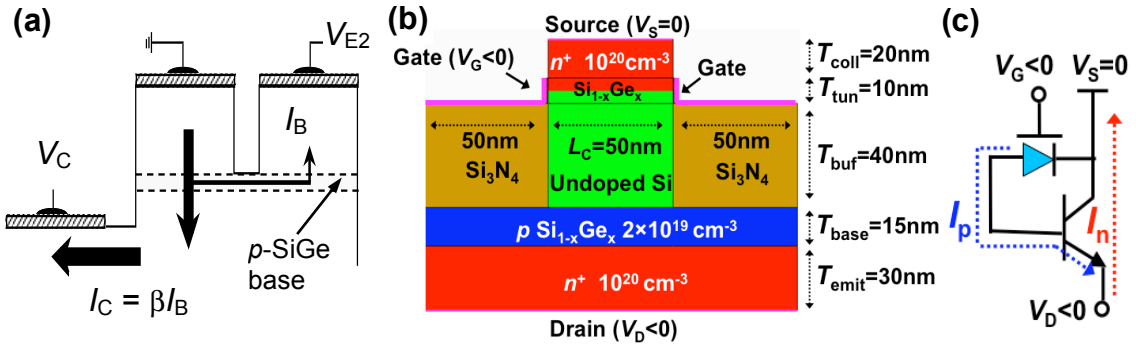

Figure 1. (a) Schematic view of the previously demonstrated multi-emitter Si/$Si_{1-x}Ge_x$ HBT with enhanced logic functionality, where the base current supplied by a reverse-biased emitter-base junction (16). (b) The BET-FET device layer sequence; the source (collector) stripe width $L_C = 50$ nm. (c) Equivalent circuit of the BET-FET in the $V_G < 0$ on-state; arrows denote current flow: the base current I_B is provided by the sidewall-gated TFET, leading to large $I_D = \beta I_B$ output current (12).

gible emitter-collector current as in a floating-base HBT. At $V_G < 0$, the TFET tunneling barrier is reduced and the tunneling hole current flows to emitter-base junction, providing the base current. A high electron current is then injected from the emitter into the base, diffuses across the base and goes to the collector as in a normal HBT. The current components are shown in Fig. 1(c): the difference between BET-FET and a standard HBT is the origin of I_B, whereas other HBT parameters like β are unaffected.

Figure 2(a) shows the $I_D(V_G)$ characteristics of the BET-FET at $V_D = -1.5$ V with Ge content $x = 0.3$ in both base and tunneling layer. For comparison, a conventional vertical TFET with the same tunnel layer structure as in Fig. 1(a) but with a p^+-Si doped drain replacing the p^+-$Si_{1-x}Ge_x$/n^+-Si emitter-base junction. The difference between the BET-FET and the TFET results from the bipolar current gain β, shown explicitly on the right of Fig. 2(a). As in a standard HBT, β is degraded both at low I_D due to nonideality of emitter-base injection and at high I_D due to high injection effects (20); for the parameters in Fig. 1(b), β peaks at ~1200 around I_D~100 μA/μm. At $V_G = V_D = -1.5$ V, the BET-FET provides a very high $I_{ON} > 4000$ μA/μm.

Figure 2(b) compares the *SS* values in BET-FET and TFET. As usual, the conventional TFET exhibits $SS < 60$ mV/dec over a limited two-decade range of I_D. The same is true for the TFET-provided base current of the BET-FET, but the bipolar gain ensures that the *SS* of the output current I_D remains < 60 mV/dec over 7 decades of current. The dependence of the BET-FET performance on the HBT design, such as the Ge content in the base or the base width T_{base} follows the usual dependence of current gain β on these parameters, as discussed in (12). Analogously, increasing the Ge content in the tunnel layer T_{tun} is important to maximize the interband tunneling current due to the smaller $Si_{1-x}Ge_x$ bandgap.

In the vertical BET-FET of Fig. 1(b), the hole base current is generated by interband tunneling at the sidewalls, whereas the injected electron current flows through the central section of the collector stripe L_C, as illustrated in Fig. 3. If the structure is symmetric, the downscaling of L_C is limited by the constriction of electron flow through the central region by the negatively biased sidewall TFET gates. The BET-FET performance can be restored by having independent biasing of the two sidewall gates: with one of the sidewall gates biased at $V_G < 0$ to activate the TFET current and the other sidewall gate biased at $V_G > 0$ to facilitate electron flow, a high I_{ON} can be created even with $L_C = 10$ nm (12). The fabrication of independent sidewall gate contacts on both sides of the collector stripe would complicate the process, but not impossibly so.

An alternative BET-FET variant that does not require a sidewall gate and is MOSFET-like in layout is shown in Fig. 4(a). Here the planar gate controls the interband tunneling at the edges of the n^+-$Si_{0.70}Ge_{0.30}$ source region junctions under the gate. The holes again flow to the p^+-$Si_{0.70}Ge_{0.30}$/n^+-Si emitter-base junction below, resulting in an amplified electron current I_D flowing from the emitter to the collector – the calculated $I_D(V_G)$ transfer curves for $V_D = -1$ and -1.5 V of an $L_G = 50$ nm device are shown in Fig. 4(b), whereas the corresponding hole and electron current densities are shown in Figs. 4(c) and 4(d), respectively. The I_{ON} is high and average *SS* remains below 60 mV/dec over many orders of magnitude in current.

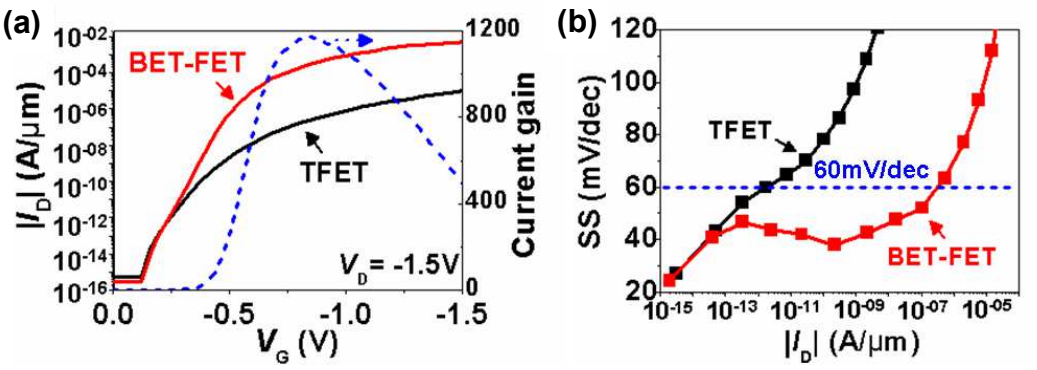

Figure 2. Comparisons of (a) current and (b) subthreshold swing (SS) between BET-FET and conventional TFET. Dashed line in (a) denotes the bipolar current gain that ensures the superior performance of the BET-FET.

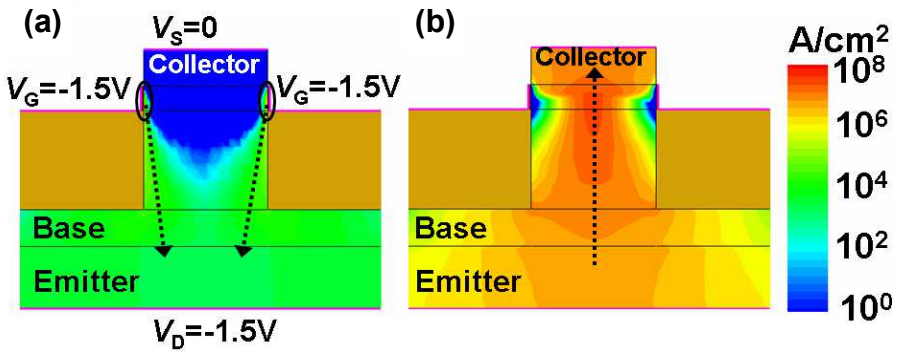

Figure 3. Hole (a) and electron (b) current densities in the BET-FET in the on-state, V_G = V_D = –1.5 V, for L_C = 50 nm. Arrows indicate the direction of hole and electron flow, which are spatially separated. Note the constriction of electron current to the center of the stripe.

It should be noted that as the gate length L_G is downscaled, the symmetric device of Fig. 4(a) would suffer from the same constriction of electron flow as the device in Fig. 3. Furthermore, both vertical current flow BET-FETs require the fabrication of an extended contact region for the buried drain. An alternative, fully planar BET-FET is illustrated in Fig. 5(a). This asymmetric BET-FET variant has a $Si/Si_{0.7}Ge_{0.3}$ HBT at the drain only (T_{base} = 15 nm, *p*-doped to 2×10^{19} cm^{-3}) and a gate-controlled tunneling junction at the source junction under the gate. The simulated gate length L_G = 50 nm, with 25 nm nitride spacers, and a 1 nm equivalent gate oxide thickness. The corresponding simulated $I_D(V_G)$ curves for V_D = –1 and –1.5 V are shown in Fig. 5(b). Again, the device provides high I_{ON} > 1 mA/um and SS < 60 mV/dec over a large current range. This variant of the device has the advantage of current separation: the tunneling hole base current flows laterally in the SiGe channel under the gate, whereas the electron current is injected vertically from the emitter through the base and then flows laterally in the n^+-Si collector under the Si buffer. As a result, the gate voltage V_G does not restrict the electron current and the device has potentially better scalability. However, the fabrication is much more challenging, as SiGe epitaxy of the HBT emitter-base heterojunction is required on the drain side selectively.

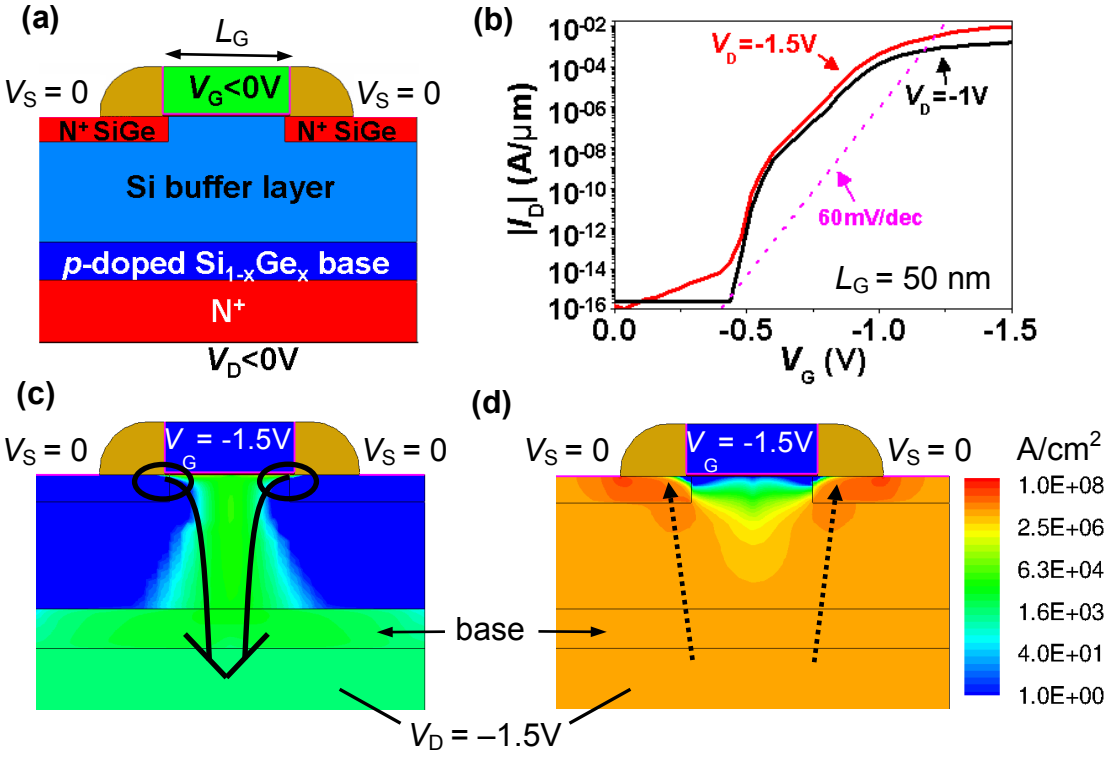

Figure 4. (a) Symmetrical BET-FET variant with a MOSFET-like layout. (b) $I_D(V_G)$ simulations for L_G = 50 nm and V_D = –1 and –1.5 V. (c) Hole and (d) electron current densities at $V_G = V_D$ = –1.5 V, with lines indicating the direction of current flow. Device parameters are: T_{coll} = 10 nm of n^+-$Si_{0.7}Ge_{0.3}$ with 10^{20} cm^{-3} doping; T_{buf} = 40 nm undoped Si; T_{base} = 15 nm of p-$Si_{0.7}Ge_{0.3}$ with 2×10^{19} cm^{-3} doping; T_{emit} = 30 nm of n^+-Si with 10^{20} cm^{-3} doping.

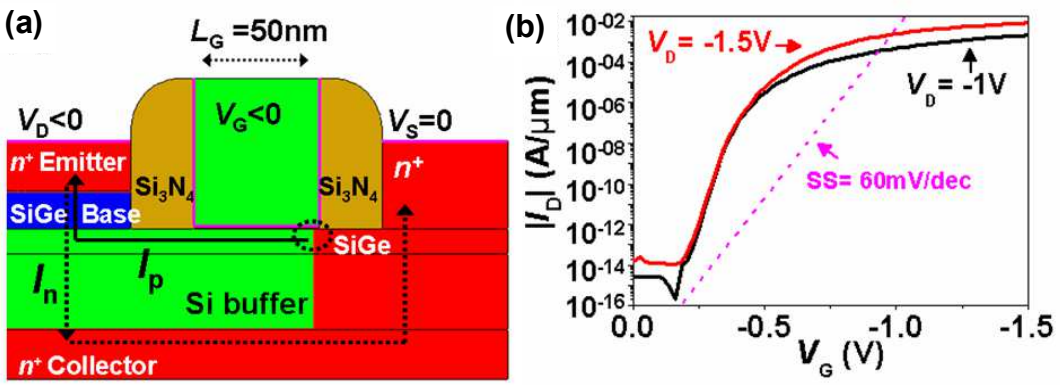

Figure 5. (a) A variant of BET-FET with planar compact layout, showing the tunneling hole and injected electron currents. (b) Simulated $I_D(V_G)$ curves for V_D = –1 and –1.5 V, with L_G = 50 nm and a $Si_{0.7}Ge_{0.3}$ base selectively deposited on the drain side only. The simulated *SS* is below 60 mV/decade over 10 orders of I_D.

As a final comment on the BET-FET concept, we note that while all of the simulations have been carried out for Si/SiGe HBT heterojunctions, the same device architecture can in principle be exploited in III-V heterojunction material systems that are often employed for high-performance HBTs. For example, III-V HBTs with InGaAs base and tunnel layers are well-suited to simultaneously increasing the HBT gain β and the TFET interband tunneling current density due to lower E_G and carrier effective mass (21). The required V_{DD} would also be lower due to faster turn-on of the emitter-base junction. The difficulty with the III-V implementation of the BET-FET lies in the inadequate dielectric surface passivation, which has prevented all reported III-V TFETs from achieving $SS < 60$ mV/decade (11, 21).

Heteronanowire trigate Si/Ge TFET

Another approach to increasing I_{ON} in a TFET while maintaining a low I_{OFF} is to use a heterostructure designed to have a tunneling junction in the lower bandgap material when the device is turned on by V_G, but in the higher bandgap material when the device is off, at $V_G = 0$. The most best-studied and most technologically mature Si-compatible heterostructure with a sufficiently small bandgap is $Si/Si_{1-x}Ge_x$. However, because of lattice mismatch and the fact that E_G of $Si_{1-x}Ge_x$ remains large until high Ge content (19), the usual $x < 0.4$ $Si/Si_{1-x}Ge_x$ heterostructures used to great advantage in HBTs are unlikely to provide sufficient performance. A possible solution is the use of a narrow diameter Si/Ge heteronanowire, where lattice mismatch can be accommodated by radial expansion and higher Ge content is attainable.

The concept of the Si/Ge heteronanowire TFET is illustrated in Fig. 6, where a diameter $D \sim 50$ nm Si/Ge heteronanowire is gated in the trigate geometry. The doping profile of the VLS-grown nanowire is shown in Fig. 6(a), with the p^+-Ge/p^--Si heterojunction followed by an axial doping *pn* junction in Si. The trigate, ideally using a high-κ gate insulator must be aligned with the Ge/Si heterojunction. At $V_G > 0$, the *p*-Si channel is inverted, creating a tunneling junction in the p^+-Ge section on the drain side of the gate, with a high F_{MAX} due to the high density of electrons in the channel, high doping in the Ge drain, and reverse drain biasing $V_D < 0$. Conversely, at $V_G = 0$, the junction is now on the source side of the gate and for the same V_D the F_{MAX} occurs in Si where one side of the channel-source junction is lightly doped. Figure 6(b) shows an SEM of the Ge/Si heteronanowire, on an oxide-covered Si substrate, prior to gate stack formation, with a kink at the heterojunction. While the kink can be avoided by optimizing the growth, it is helpful in the fabrication of the proof-of-concept TFET devices by facilitating gate alignment. The device was completed by depositing a 10 nm HfO_2 gate dielectric and Ni metal for both gate and source-drain metallization.

The room-temperature measured TFET $I_D(V_G)$ transfer characteristics at constant $V_D = -0.2$ to -0.8 V in 0.2 V steps are shown in Fig. 7(a). The maximum I_{ON} achieved in our device at $V_G = 0.1$ V and modest $V_D = -0.8$ V is ~ 2 μA/μm (normalized to the wire diameter), comparable to or higher than reported for Si-based NW (22, 23), Ge-based (24), Ge/SiGe core-shell NW (25), and recently reported axial InP-GaAs hetero-NW TFETs (26).

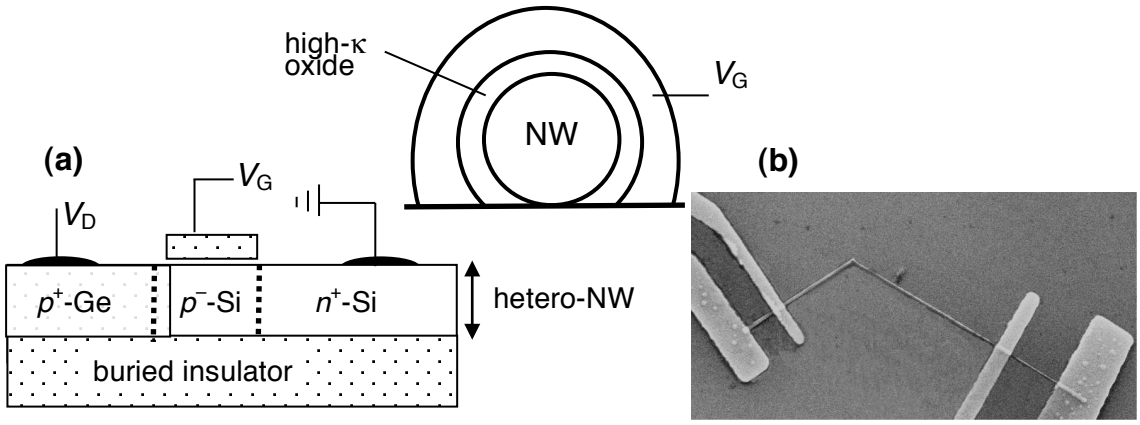

Figure 6. (a) Heteronanowire p^+-Si/Ge/n^+-Si NW TFET, gate overlaps source-drain depletion region, dashed lines indicate planes of F_{MAX} for V_G = high (in Ge, large I_{ON}) and V_G = low (in Si, low I_{OFF}). The gate wraps around the hetero-NW on three sides, as shown in the inset. (b) SEM of Ge/Si heteronanowire.

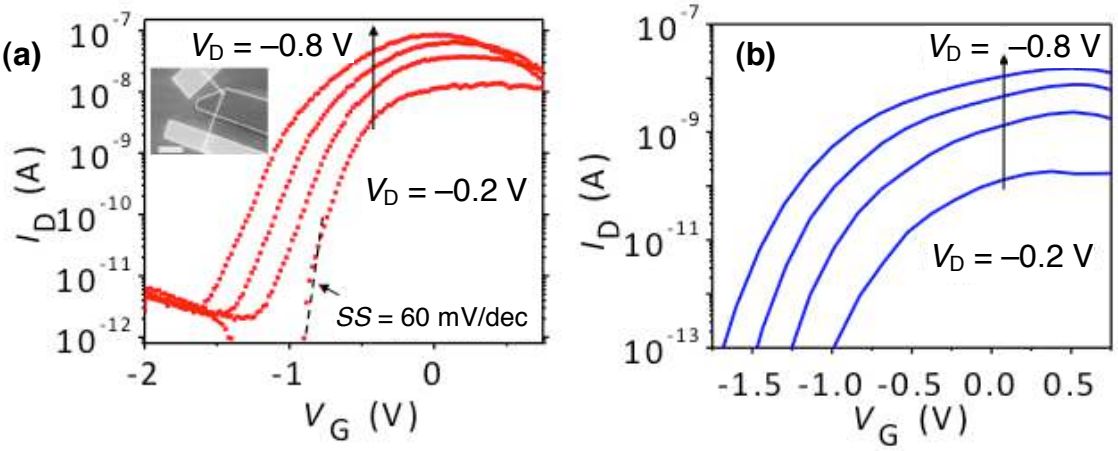

Figure 7. (a) $I_D(V_G)$ transfer characteristics at V_D = –0.2 to –0.8 V in 0.2 V steps, inset shows top-view SEM, with the metal gate overlapping the Ge/Si kinked heterojunction, dashed line shows *SS* = 60 mV/decade. (b) Simulation of the experimental data in the trigate geometry.

At even higher V_G, I_D begins to drop, as the gate voltage begins to deplete carriers in the *p*-Ge section resulting in lower F_{MAX} at the tunneling heterojunction. Due to our axial heterostructure, ambipolar behavior is suppressed with a very low $I_{OFF} \sim 10^{-12}$ A (corresponding to ~20 pA/μm). The I_{ON}/I_{OFF} ratio is 10^5, with an average subthreshold slope *SS* ~ 140 mV/decade over 4 orders. The best *SS*, observed over the two lowest decades of I_D, reaches 50 mV/decade. Better device performance, meaning higher I_{ON} and smaller *SS*, could be realized by improving the heterojunction abruptness (27) and surface passivation, better electrostatic gate control of a full gate-all-around geometry, and increased drain doping.

Figure 7(b) shows the TCAD simulation of the trigate structure, assuming a 50 nm linear Ge/Si drain-channel transition, a 6 nm per decade of doping decay in the p^+-Ge/p^--Si junction, a 10^{15} cm^{-3} doping in the p^--Si region (not intentionally doped), and a high fixed oxide charge at the HfO_2/Ge interface (15). The fixed oxide charge shifts the

threshold for inversion of the channel to negative V_G, resulting in good agreement with the data. The tunneling current was calculated using the nonlocal dynamical tunneling model with the reduced effective mass fitting parameter set to $m^* = 0.01m_0$ (28).

We also observed a surprising effect in our device: the back-gate V_{BG} response of the device depends strongly on the presence of the tri-gate metal. The transfer characteristic of our hetero-NW TFET as a function of V_{BG} applied to the *p*-Si substrate separated from the hetero-NW by 100 nm of SiO_2 is shown in Fig. 8(a). At this stage, the device had nickel source/drain contacts and a 10 nm HfO_2 top-gate oxide, but no gate metal. We observe that sweeping V_{BG} from zero down to –10 V exerts relatively weak control over the drain current I_D (at fixed V_D), as expected for the thick buried oxide. This agrees with our recent measurements on Ge nanowire TFETs in a similar geometry (29), where we modeled the back-gate control by estimating the fringing fields in SiO_2 and their effect on F_{MAX} at the tunneling junction. Figure 8 (b) shows the $I_D(V_{BG})$ measurement on the same device, with the tri-gate Ni metallization now in place but kept floating. We now observe excellent V_{BG} control with 4–5 orders of I_D modulation seen as V_{BG} is swept from 1 to –2 V. This strong V_{BG} control goes away if a fixed bias V_G is applied to the top gate.

As a final comment on the SiGe heteronanowire trigate TFET, it is clear that the Ge drain segment of the hetero-NW is a drawback due to the poor passivation of Ge surfaces. Given the freedom to design the composition of the hetero-NW channel, better performance could be expected if a short segment of Ge were inserted in the channel-drain junction of the otherwise Si-based device. Figure 9 shows a ~50 nm Ge section grown in a narrow, 20 nm diameter Si nanowire by the same VLS technique, together with the EDS analysis of the material composition. Such a short Ge inclusion, aligned with the gate in a vertical gate-all-around configuration demonstrated for all-Si devices (30, 31) would be promising for a Si-compatible high-current TFET.

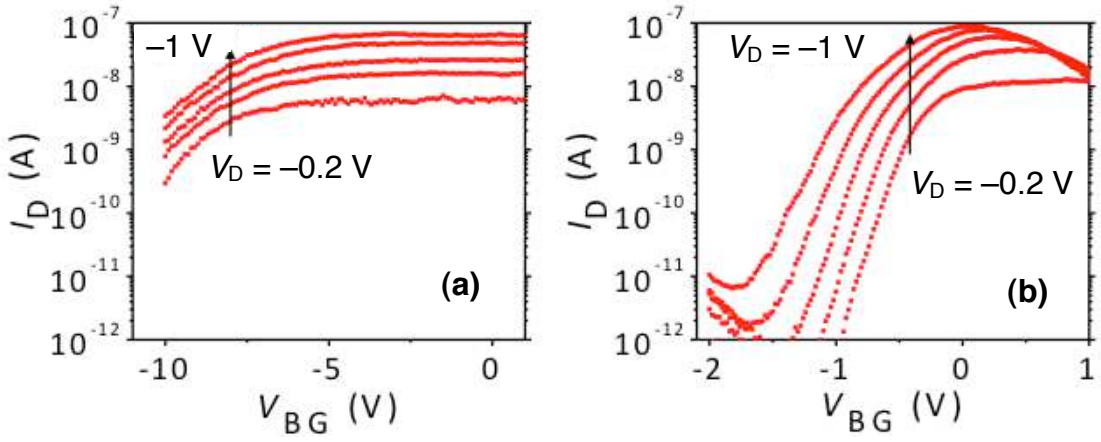

Figure 8. (a) $I_D(V_{BG})$ characteristics at V_D = –0.2 to –1 V in 0.2 V steps of the device with 10 nm HfO_2 oxide covered and no top-gate metal; (b) $I_D(V_{BG})$ characteristics of the same device with 10 nm HfO_2 covered and floating top-gate metal positioned on top of the Ge/Si heterojunction, same geometry as the inset in Fig. 7(a).

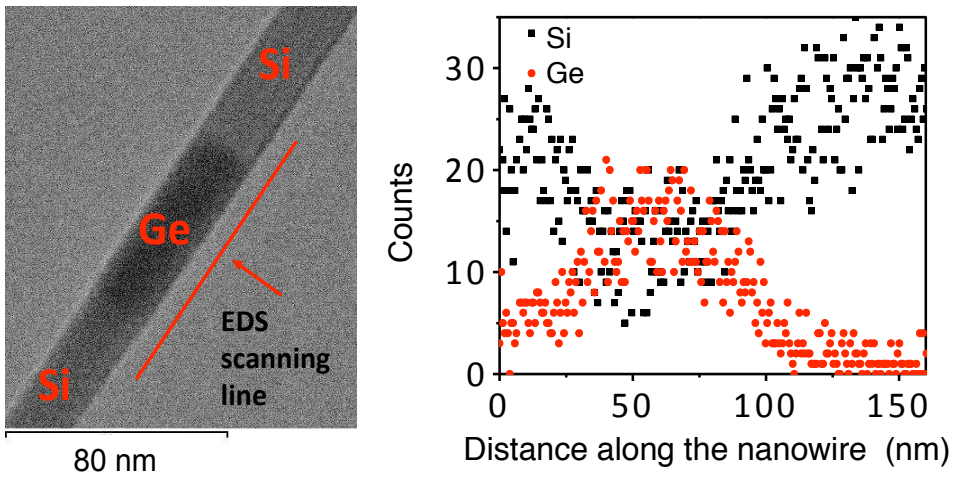

Figure 9. (a) TEM of a SiGe hetero-nanowire with the inserted Ge section of about ~50 nm; (b) EDS analysis confirming the composition along the hetero-nanowire.

Conclusions

In this paper, we have presented two distinct approaches to maximizing the current drive of TFET devices without compromising the I_{ON}/I_{OFF} current ratio or compatibility with silicon technology. The bipolar-enhanced TFET relies on the HBT-like amplification of the tunneling current and promises exceptionally high I_{ON} > 1000 μA/μm in simulation, with realistic $Si/Si_{1-x}Ge_x$ structural parameters. The device geometry can be either vertical or planar and the scaling is promising. However, the BET-FET is yet to be experimentally demonstrated.

The $Si/Si_{1-x}Ge_x$ heteronanowire trigate TFET has been experimentally demonstrated to provide I_{ON} > 1 μA/μm, competitive with the best reported nanowire devices in any material system. However, the I_{ON} is still inadequate and the proof-of-concept device was fabricated via e-beam lithography on an individual nanowire, rather than a truly CMOS-compatible process, which would require surrounding gate fabrication around a vertical VLS grown pillar.

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