Ultra-short channel field effect transistors based on Ge/Si core/shell nanowires

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Abstract

In recent years, transistor technology has scaled down to sub-20 nm channel length with many performance-boosting techniques at the material and device levels in order to meet the increasing demand for higher performance electronics. The nanowire (NW) device architecture has proven itself as a viable candidate for the sub-20 nm generation transistors. Compared to Si NWs, the Ge/Si core/shell NW alternative can supply larger on-current due to the increased confined hole mobility and ohmic behavior at the Ni-alloyed drain/source contacts. It is thus important to understand transport mechanisms in this core/shell structure, and develop pathway to realize ultra-short channel core/shell NW field effect transistors (FETs).

In this paper, we report the growth of Ge/Si concentric NWs with precise control of Si shell thickness. Performance of FETs fabricated from core/shell NWs exhibited a clear dependence on NWs' diameters, with steeper sub-threshold slopes for smaller NWs. An 18 nm diameter Ge/Si heterostructure FET exhibited sub-threshold swing of 102 mV/decade, with a maximum transconductance of 3.4 μS at V_{DS} =-100 mV. Finally, transmission electron microscopy was utilized to monitor and control the solid state reaction between Ni contacts and Ge/Si NWs, resulting in ultra-scaled channel lengths, as short as 5 nm.

Keywords: nanowires, Ge/Si core/shell, field effect transistor, ultra-short channel.

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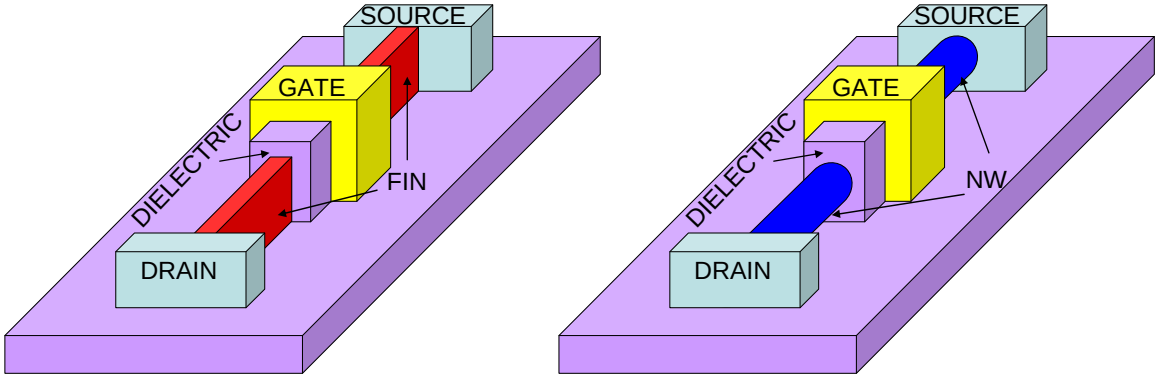
1. INTRODUCTION

In order to meet the increasing demand for high performance electronics, CMOS transistor technology has witnessed continuous scaling of their channel lengths down to sub-20 nm with many performance boosting techniques at the material and device levels. However, at these dimensions, conventional planar bulk field effect transistors (FETs) severely suffer from short channel length effects, as dictated by the threshold voltage roll-off, drain-induced barrier lowering and degradation of sub-threshold swing. In order to avoid such adverse performance effects, a novel transistor architecture utilized from the 22 nm technology node is the tri-gate FINFET (Fig 1a) where the conduction channel is raised above the planar platform for better electrostatic coupling between gate voltage and mobile carriers in the channel. This 3D configuration resembles to the geometry of a nanowire FET (NWFET), in which the gate can be formed in an Ω-shape, or completely wrap around the NW transistor. Moreover, for bottom-up synthesized NWs, the 3D geometry can be easily formed without sophisticated etching of nanoscale structures. Recently, ultrashort-channel length NW transistors have been demonstrated (40 nm channel length for Ge/Si core/shell NWs[1] and 17 nm for Si NWs[2]) with superior performance over conventional silicon planar devices for the former[1], thus, proving themselves as viable candidates for a new generation of sub-20 nm FETs.



a) b)

Figure 1- Schematic diagram of a) FINFET structure, b) NWFET structure.

Among the Si-based NW systems, the Ge/Si core/shell NW structure[3-4] possesses a number of advantages. First, utilizing Ge core as a hole conduction channel, this material system can enable higher on-current due to larger thermally generated mobile charge concentration with higher mobility tied to a lower hole effective mass in Ge than in Si. Second, with the higher band gap Si shell, the holes are thus confined in the Ge core, alleviating surface scattering that is detrimental to carrier mobility. Finally, the ohmic nature of Ge with Ni as a metal contact for PMOS source/drain reduces undesirable contact resistance that hampers transistor performance. In this paper, we present a systematic investigation on the diameter dependence of FET performance and experimentally confirm that the on-current enhancement of Ge/Si core/shell NWs compared to intrinsic Ge NWs is due to suppression of surface scattering. With the presence of the Si shell, the hole mobility remains insensitive to NW diameters while the sub-threshold swing monotonically decreases from ~ 400 mV/decade at 50 nm NW diameter to ~100 mV/decade as the diameter is reduced to 16nm. By using in-situ transmission electron microscopy, we demonstrate that sub-20 nm ultra-short channel length NWFETs with abrupt interfaces cannot be obtained using conventional solid-state reaction between a Ni lead and Ge/Si core/shell NW. A new process is devised to remedy this issue and control the nickelide/germanide-Ge interface to realize a 5 nm channel length.

2. MATERIAL GROWTH AND STRUCTURAL CHARACTERIZATION

Ge/Si core/shell NWs utilized in this work were grown in a low-pressure cold-wall CVD system[5]. The 1D growth of the core was mediated by liquid Au-Ge catalytic nanoparticles while the shell growth on sidewalls was governed by direct vapor-solid deposition on the NW's sidewalls. Gold colloids (Ted Pella, Inc. CA) with diameters ranging from 5 nm to 40 nm were dispersed randomly on a cleaned Ge (111) surface. The substrate was loaded into the CVD reactor and degassed at ~120^{o}C for 30 min under vacuum (low 10^{-6} Torr). The temperature was then ramped up to ~ 360^{o}C for 2 min to nucleate Ge NWs under 250 sccm GeH_4 (30% in H_2) at 2 Torr. Elongation of the Ge NWs proceeded under the same gas flow and pressure, but at ~280^{o}C to avoid lateral growth on the NW's sidewalls due to vapor-solid deposition. Prior to switching to Si shell growth, a thin interfacial layer of Si was introduced beneath Au seeds to avoid Au diffusion down to the Ge NW sidewalls at elevated temperatures[6]. The growth of the Si shell was performed at 410^{o}C under 450 sccm SiH_4 (50% in H_2) at 0.5 Torr. Shell deposition thicknesses were calibrated ex-situ with TEM measurement to result in 1-4 nm shell thickness with a 1 nm step as shown in **Figure 2**. Further details on growth procedure and structural analysis can be found in Ref[7] [8].

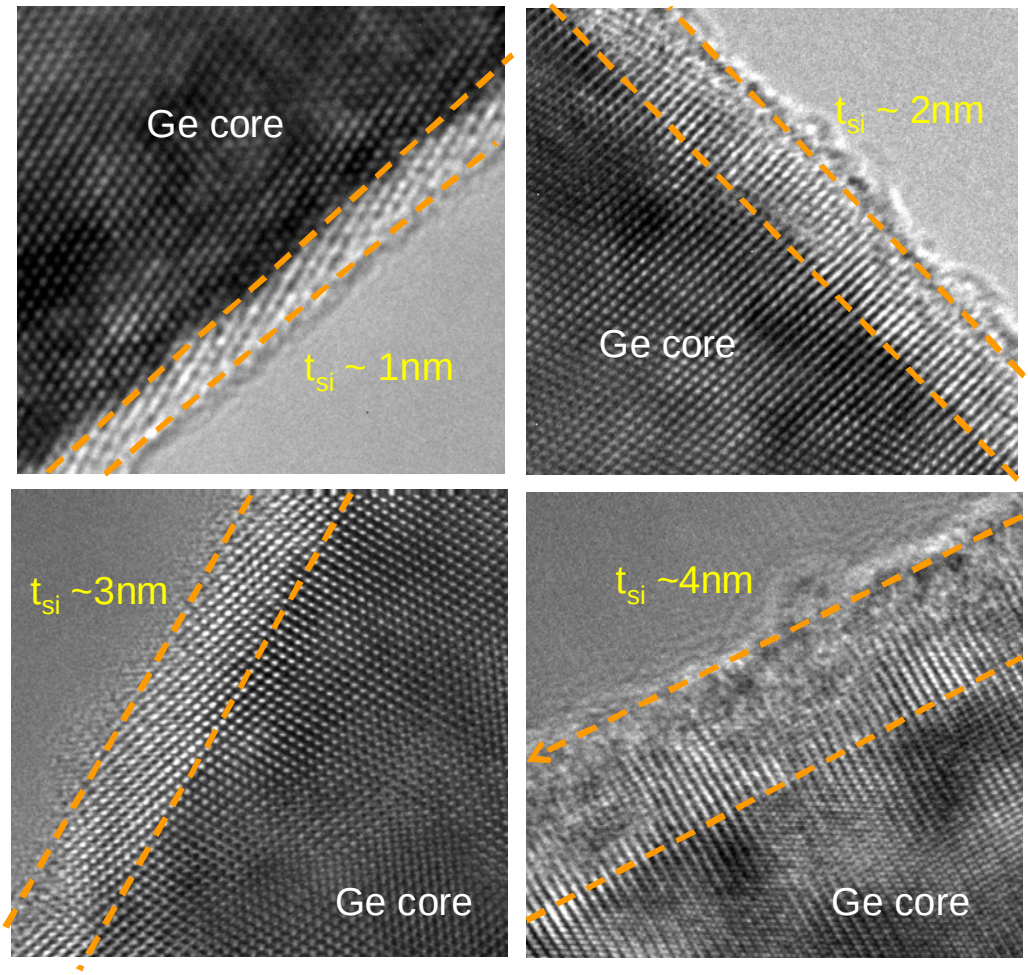


Figure 2- High resolution TEM images of Ge/Si core/shell structures with different Si shell thicknesses. Deposition duration was 27, 32, 37 and 42 minutes for 1, 2, 3 and 4 nm thick Si shell, respectively.

3. DEVICE FABRICATION

In this study, 5, 10, 20, 30 and 40 nm diameter Au colloids were utilized in order to assess NWFET performance as a function of NW diameters. The shell thickness was chosen to be 3 nm in order to maximize carrier confinement in Ge cores, while still ensuring shell crystallinity to avoid potential dislocation-induced surface leakage [8]. In addition to the samples listed above, a control reference of Ge NWs without any Si shell, grown from 30 nm Au colloids was added for comparison between core and core/shell structures. While for the same growth run, the shell diameter stays relatively constant, there is a distribution of NW diameters despite using Au colloids with the same nominal sizes (**Figure 3**). It is thus important to understand how the NW diameter affects transistor performance, and establish a figure of merit to compare NWs at different diameters.

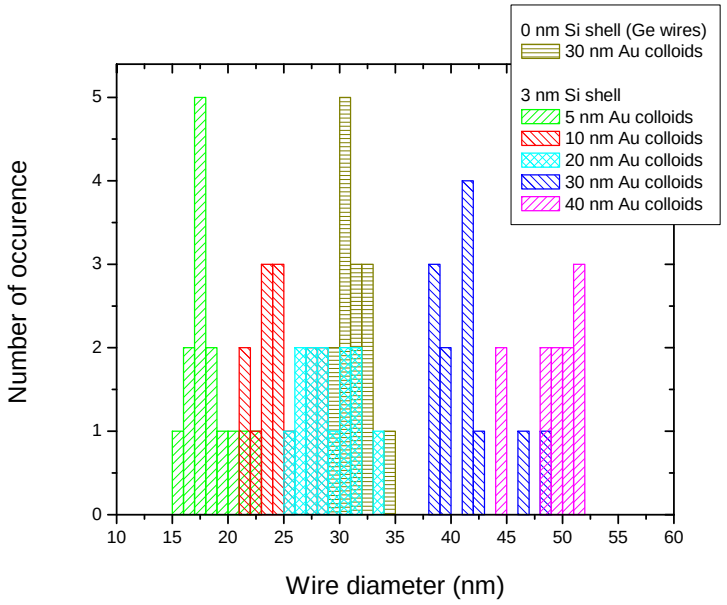


Figure 3- Diameter distribution of NWs utilized in this study.

For FET fabrication, NWs were transferred onto a Si_3N_4-coated Si substrate with pre-deposited marks for electron-beam (e-beam) lithography alignment, and for recording NW coordinates. Six groups of NWs with different nominal diameters were transferred to six separated dies on the same Si_3N_4/Si handle substrate, and were processed together in order to minimize discrepancy that might arise during the device fabrication. A scanning electron microscope (SEM) was utilized to identify NW location while a combination of Matlab and L-edit scripts were run to draw NWs and contact pads on a CAD file. E-beam lithography was used to define openings for electrical contacts to the NWs, followed by 130 nm thick Ni contact deposition by e-beam evaporation. After metallization and lift-off, the sample was annealed at 300^{o}C for 30 seconds using Rapid Thermal Annealing (RTA) under vacuum with forming gas. This anneal step is introduced to create solid-state reaction between Ni and Si/Ge, and from a metallic low contact resistance $NiSi_x$/$NiGe_y$ interface with the NWs. The formation of $NiSi_x$ into Si NWs was shown to exhibit layer-by-layer epitaxy with atomically sharp interfaces[2], hence, can be utilized to precisely control the length of an un-reacted semiconductor channel. This process will be detailed in section 5 for the realization of ultra-short channel length Ge/Si core/shell NWs. After RTA, SEM was performed to record the NW diameters and lengths of

un-reacted segments (**Figure 4**). A 10 nm thick high-k HfO_2 dielectric was then deposited using atomic layer deposition (ALD) and finally 130 nm thick Ti/Au top gate contacts were formed with e-beam lithography and metal evaporation. The metal gate is designed to fully overlap with the source and drain in order to minimize series resistances caused by un-gated segments. Prior to electrical measurements, the sample was annealed with RTA at 300°C for 30 seconds to saturate dangling bonds within the HfO_2 layer and at the HfO_2/Si interface for better FET performance.

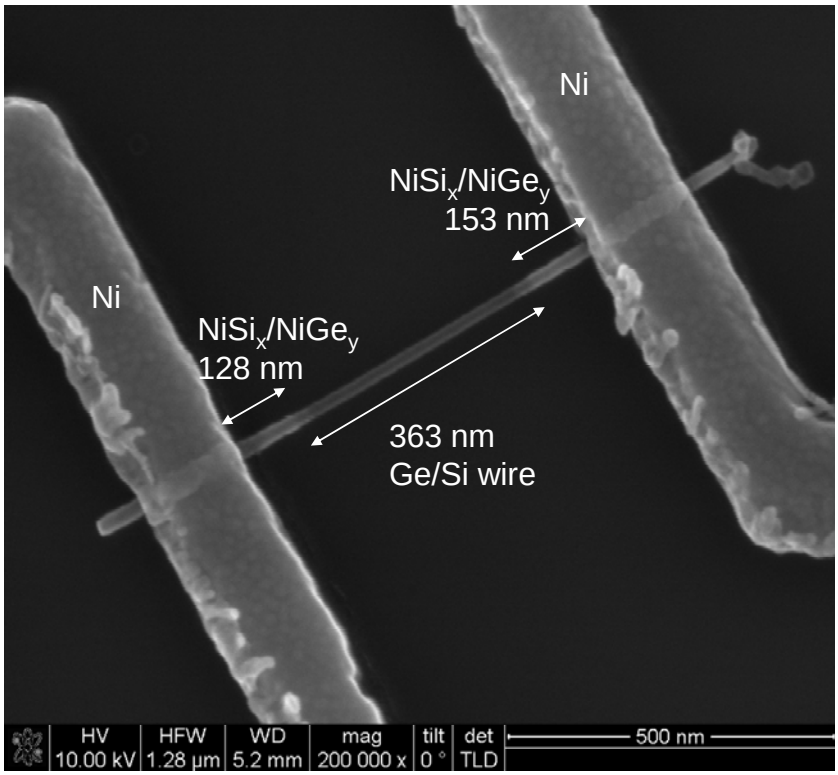


Figure 4-SEM image of a NWFET (prior to Gate formation). Channel length is determined by the marked un-reacted segment with darker contrast.

4. RESULTS AND ANALYSIS

Figure 5 shows the transfer curves (abs(I_{DS}) vs. V_G) at V_{DS}=-100 mV for representative devices from each group of diameters. As it can be clearly seen, the Ge NW (without Si shell- black line) has significantly lower current than core/shell NWs. This result is an experimental evidence for the advantages of core/shell structures in comparison with bare Ge NWs, which have been discussed in the introduction. The improvement in transconductance in core/shell structures can be explained by either an increase of hole concentration due to charge transfer from the outer shell to the confined Ge core, or an enhancement of hole mobility due to minimized surface scattering in the core/shell NWs, or both. Further evaluation of these two possibilities will be discussed later in this manuscript with more statistics of all transistor devices. When comparing the core/shell NWs, it is clear that NWs with larger diameter have larger on-current and are more difficult to turn off. This is because larger NWs have more cross-section to contribute to the on current, thus are also more difficult to deplete across the entire diameter. While it is straightforward to qualitatively understand the trend with diameter, it is important to draw out a more quantitative description of the relationship between NW diameter and FET performance.

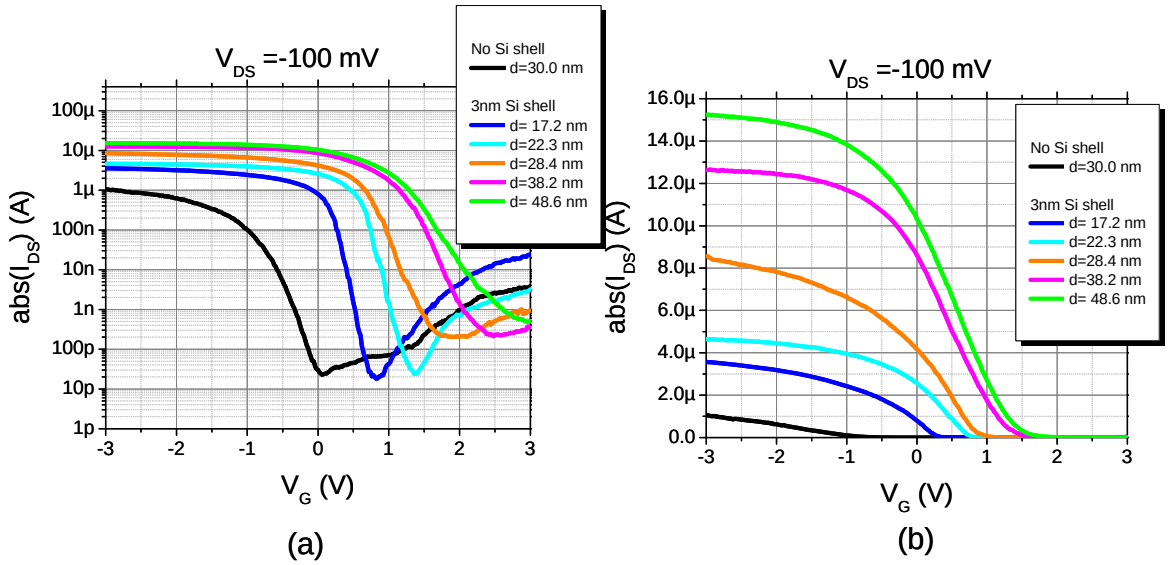


Figure 5- abs(I_{DS}) vs. V_G transfer curves of representative devices for each die: a) log scale, b) linear scale.

In order to better quantify the trend for diameter dependence, we extract the sub-threshold swing $SS_{\max} = \max(\frac{d\ln(abs(I_{DS}))}{dV_G})$ and the maximum gate transconductance $g_{m-\max} = \max\frac{d(abs(I_{DS}))}{dV_G}$ for all NWs.

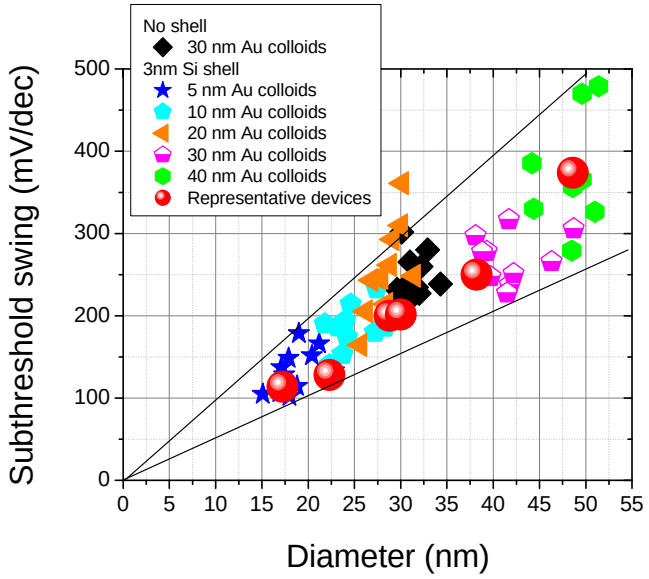


Figure 6- Sub-threshold swing of all devices as a function of NW diameter

Shown in **Figure 6** is the sub-threshold slope as a function of NW diameters. The two straight lines are for guiding the eyes to illustrate the distribution of SS_{max} for all the measured NWFETs, but do not have any physical meaning. Not only do smaller NWs have smaller sub-threshold swings, but they also appear to be more uniform. Unlike the general intuition that smaller nano-systems are prone to be more sensitive than larger ones due to bigger surface contribution, in this case of NWFETs, smaller diameter NWs are easier to be depleted, thus can be controlled more uniformly with gate bias. The trends for SS_{max} in NWFETs is similar to what have been shown theoretically with a thin body silicon-on-insulator Schottky barrier transistor [9].

While there is no difference in SS_{max} between core/shell and core structures, the maximum transconductance ($g_{m\text{-}max}$) of the NWs without shell lies significantly below the trend for core/shell NWs (**Figure 7**). In an FET, the transconductance is governed by the device geometry, drain/source voltage and carrier mobility, as shown in equation (1):

$$g_m = \frac{d(abs(I_{DS}))}{dV_G} = \frac{\mu C_g V_{DS}}{L^2} \quad \text{Equation 1}$$

where μ is the hole mobility, C_g is the gate capacitance, V_{DS} is the drain/source voltage, L is the channel length. As there is no difference in V_{DS} and L between core/shell and core structures, the difference in $g_{m\text{-}max}$ is clearly due to the change in the product of carrier mobility and gate capacitance

The linear relationship between $g_{m\text{-}max}$ and diameter in **Figure 7** validates the use of the normalized transconductance[1] as a figure of merit to compare between NWFETs, and with other transistor technologies. In this work, the maximum normalized transconductance $g_{m\text{-}max}/d$ attains 190 μS/μm. It is important to note that this value is associated with V_{DS}= -100 mV, and the gate dielectric thickness is 10 nm. With a thinner dielectric and a larger V_{DS}, the normalized transconductance is expected to surpass 1mS/μm.

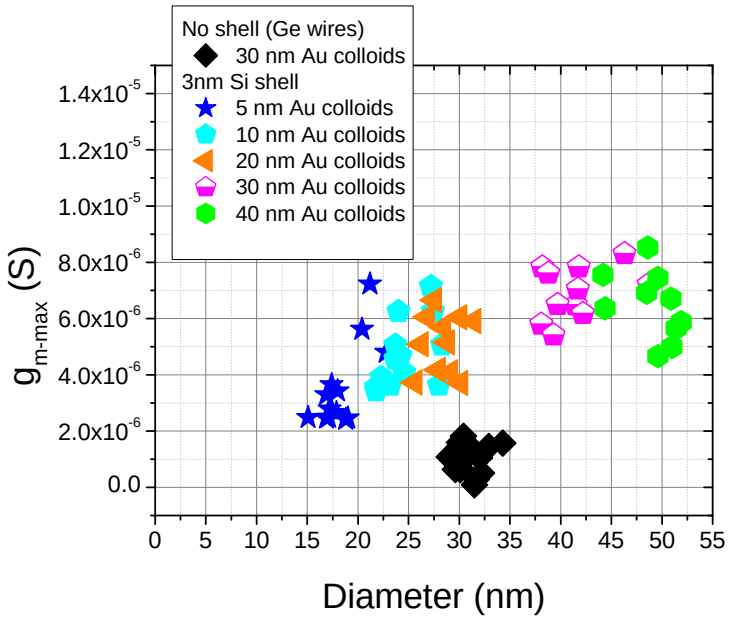


Figure 7-Maximum transconductance of all devices as a function of NW diameter

5. TOWARD ULTRA-SHORT CHANNEL FETS

While Ge/Si core/shell devices enable higher current than the Si counter part, so far, no core/shell devices have been able to attain a channel length less than 20 nm. In order to uncover critical details for achieving such ultra-short channels, we utilized a transmission electron microscope (TEM) as a tool for the

in-situ study and control of channel length formation.

Devices for this study were processed using the same procedure as presented in section 3, however, the substrate has 250 μmx250 μm window of 50 nm thick Si_3N_4 membrane that is transparent to the electron beam inside the TEM. NWs were transferred on the membrane so that they can be observed under TEM during silicide/germanide contact growth (**Figure 8**).

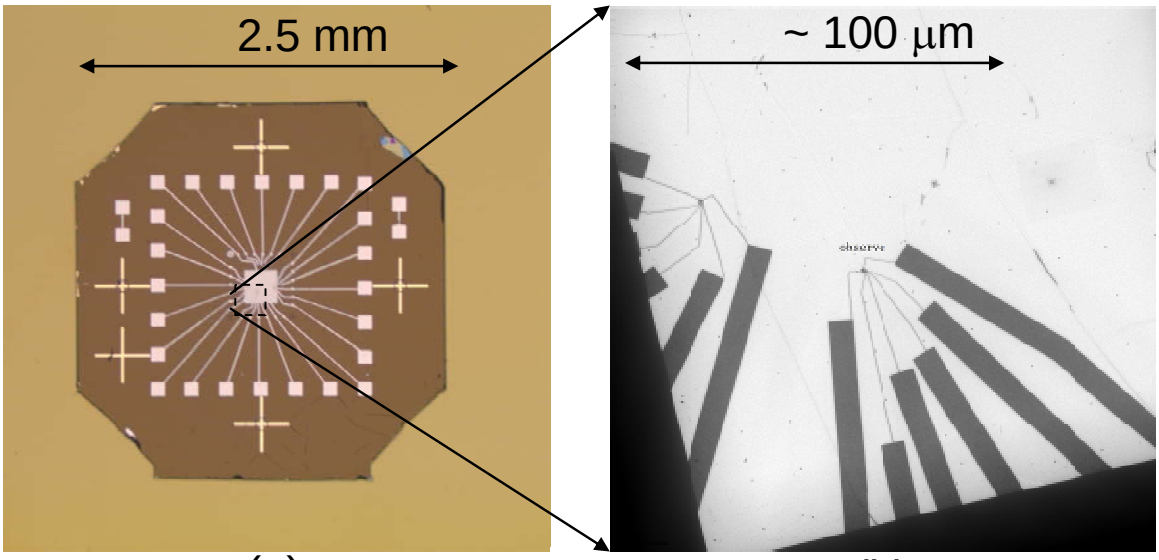


Figure 8-Substrate with 250 μmx250 μm window of 50 nm thick Si_3N_4 membrane for TEM measurement

After processing, the sample was loaded onto a single tilt Gatan heated-stage in a Tecnai F30 TEM. The stage was slowly heated up to 265 ^oC, at which temperature Ni contacts began to react with the NWs. The process started with nickel silicide formation at the shell and extended a few tens of nanometers before the germanide nucleation took place at the core. Despite a faster reaction rate of Ni with bulk Ge than with bulk Si, the two reaction fronts at the core and the shell propagated with the same growth velocity, making it impossible to create ultra-short Ge channel without having a conductive nickel silicide shell (**Figure 9**a). In order to eliminate earlier nucleation in the Si shell, we have revised the process flow and removed the Si shell in the drain/source opening prior to depositing Ni contacts. As a result, Ni was in direct contact with the Ge NW core, facilitating the germanide reaction at even lower temperature (240 ^oC). As shown in **Figure 9**b, a channel length of 5 nm was formed while the Si around the Ge segment remains un-reacted with Ni. Transport characterization of ultra-short channel Ge/Si core/shell NWFETs is currently in progress.

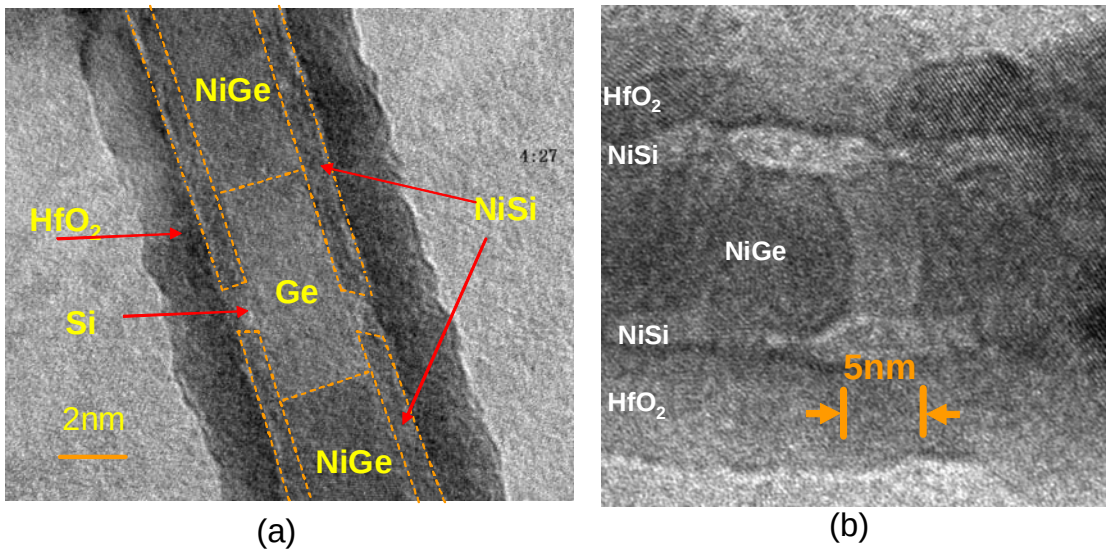


Figure 9-In-situ observation of ultra-short channel length formation a) with Si shell, b) Si shell removed underneath Ni contacts

6. CONCLUSIONS

In conclusion, we have experimentally confirmed the advantages of Ge/Si core/shell NWs, with enhanced mobility due to suppression of surface scattering. Diameter dependence of transport study confirms that it is easier to deplete smaller NWs, thus having steeper inverse sub-threshold slopes. An ~18 nm diameter Ge/Si heterostructure FET exhibited a sub-threshold swing of 102 mV/decade with a maximum transconductance of 3.4 μS at V_{DS}=-100 mV. In-situ TEM heating experiment enabled the realization of ultra-short channel length (5 nm) Ge/Si core/shell structures, which is the first stepping stone to demonstrate high performance, ultra-short channel Ge/Si heterostructured NWFETs.

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7. REFERENCES

[1] Y. Hu, J. Xiang, G. Liang, H. Yan, and C. M. Lieber, “Sub-100 Nanometer Channel Length Ge/Si Nanowire Transistors with Potential for 2 THz Switching Speed,” Nano Letters, 8(3), 925-930 (2008).

[2] W. Tang, S. A. Dayeh, S. T. Picraux, J. Y. Huang, and K.-N. Tu, “Ultrashort Channel Silicon Nanowire Transistors with Nickel Silicide Source/Drain Contacts,” Nano Letters, (2012).

[3] L. J. Lauhon, M. S. Gudiksen, D. Wang, and C. M. Lieber, “Epitaxial core-shell and core-multishell nanowire heterostructures,” Nature, 420(6911), 57-61 (2002).

[4] W. Lu, J. Xiang, B. P. Timko, Y. Wu, and C. M. Lieber, “One-dimensional hole gas in germanium/silicon nanowire heterostructures,” Proceedings of the National Academy of Sciences of the United States of America, 102(29), 10046-10051 (2005).

[5] S. T. Picraux, S. Dayeh, P. Manandhar, D. Perea, and S. Choi, “Silicon and germanium nanowires: Growth, properties, and integration,” JOM, 62(4), 35-43 (2010).
[6] S. A. Dayeh, N. H. Mack, J. Y. Huang, and S. T. Picraux, “Advanced core/multishell germanium/silicon nanowire heterostructures: The Au-diffusion bottleneck,” Applied Physics Letters, 99(2), 023102 (2011).
[7] S. A. Dayeh, A. V. Gin, and S. T. Picraux, “Advanced core/multishell germanium/silicon nanowire heterostructures: Morphology and transport,” Applied Physics Letters, 98(16), 163112-3 (2011).
[8] S. A. Dayeh, W. Tang, F. Boioli, K. L. Kavanagh, H. Zheng, J. Wang, N. H. Mack, G. Swadener, J. Y. Huang, L. Miglio, K.-N. Tu, and S. T. Picraux, “Direct Measurement of Coherency Limits for Strain Relaxation in Heteroepitaxial Core/Shell Nanowires,” Nano Letters, (2012).
[9] J. Knoch, M. Zhang, J. Appenzeller, and S. Mantl, “Physics of ultrathin-body silicon-on-insulator Schottky-barrier field-effect transistors,” Applied Physics A, 87(3), 351-357 (2007).