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Nanoscale Heterogeneous Reactions and Interfaces in Ge/Si and for III-V on Si Integrated Devices

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In the pursuit of realizing sub-10 nm transistor channel lengths in homogenous and heterostructured materials, nanoscale defects and hetero-interfaces can significantly impact the formation of alloyed metal contacts conventionally used in CMOS devices. We utilize in-situ transmission electron microscopy to unveil new observations on the detailed formation of such alloys and interfaces at an atomic scale by capturing single nucleation events during the reaction of Ni with Si, Ge and Ge/Si core/shell nanowires and assess their resultant transistor performance. We then utilized the NiSi reaction to develop a novel heterogeneous integration process for III-V semiconductors on planar and patterned Ni electrodes in a fab-compatible process. We demonstrate the operation of the first InGaAs FinFETs on Si.

Introduction

The in-situ transmission electron microscopy (TEM) observation of solid-state reactions and direct correlation with transport behavior in semiconductors is a unique tool to correlate the fundamental material structure information to final device transport characteristics (1). In ultra-scaled device dimensions, a single stacking fault, twin or grain can dominate the physical properties of the material and can exclusively take over the material's solid state reactions. Nickel silicide remains to be the standard low electrical resistance alloy contact to Si transistors in the sub-30 nm technology nodes whose processing and formation is prone to the formation of intentional and un-intentional defects. It is therefore important to assess the silicide/germanide alloy formation in such nanostructures with and without defects to better predict their physical dimensions post the silicide formation and its consequences on the overall device performance (2). Accurate control over such reaction allowed the formation of 2 nm gap in $Ni_2Ge/NiSi_x$-Ge/Si-$Ni_2Ge/NiSi_x$ metal-semiconductor-metal core/shell nanowires (3). We overview here our results on Ni alloy formation in Si, Ge, and Ge/Si core/shell nanowires and

present performance of ultra-scaled nanowire transistors with channel lengths as short as 17 nm.

We developed a heterogenous integration scheme using the NiSi reaction to integrate III-V materials on Si. Our process (i) is CMOS compatible, (ii) has a wide thermal budget, (iii) can be applied to patterned substrates, and (iv) overcomes the shortcomings of eutectic bonding and limitations of smart-cut technique. The Ni alloy reaction is used here to bond dielectric capped III-V layers to Si, and to directly react with III-V layers to form self-aligned III-V transistors on Si. This work demonstrates the first InGaAs FinFETs fabricated on insulator on Si.

Heterogeneous Reactions and FETs in Si Nanowires

Our platform consists of a 50 nm silicon nitride membrane suspended over a window in a TEM-compatible Si carrier. Vapor-Liquid-Solid (VLS) grown Si NWs were transferred to the nitride membranes from solution and photolithography was used to define Ni electrodes to the Si NWs. The metal-Si reaction formed inward into the channel with a phase sequence of Ni-rich $NiSi_x$ alloys and an abrupt termination with θ-$NiSi_2$-Si interface as shown in Figure 1. The process is precisely controlled with accuracy of 1nm on an in-situ TEM hot stage. The reactions are generally formed at 400 °C resulting in theta-Ni_2Si silicide as the leading phase in contact with silicon. The silicidation path is preferred over (111) planes and [211] oriented NWs exhibit a reaction front plane normal that is 19° inclined with respect to the growth direction, and the interface is atomically abrupt as shown in Fig. 1c with $NiSi_2$ (111)//Si (111) and $NiSi_2$ [-110]//Si [-110].

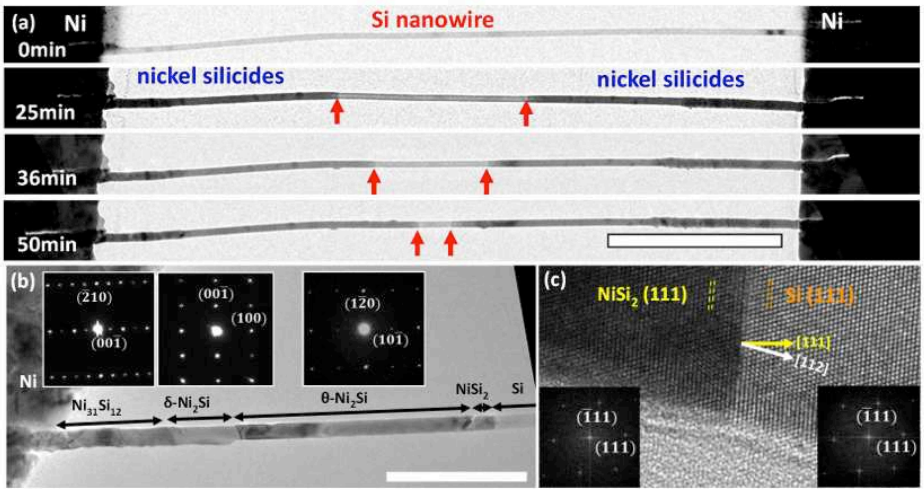

Figure 1. (a) A time stamped sequence of in-situ TEM formation of $NiSi_2$-Si-$NiSi_2$ metal-semiconductor-metal heterostructured nanowire. Scale bar is 1 μm. (b) $NiSi_x$ phase sequence starting with the Ni reservoir on the left toward the Si channel on the right with inset selective area diffraction patterns near each correspondent phase. Scale bar is 400 nm. (c) Abrupt $NiSi_2$-Si interface with the Si nanowire.

Heterogeneous Reactions in the presence of Defects

The latest source/drain (S/D) engineering technology strategically incorporates stacking faults to exert tensile strain in n-MOSFET devices (4), and elevates the Ge content (which ultimately leads to strain relaxation via stacking faults and dislocations) in

the S/D regions for p-MOSFETs (5), to boost electron and hole mobility, respectively. It is important to understand the role of structural alteration, or defects, in the NiSi reaction. We find by lattice-resolved TEM observations that the presence of defects in Si fundamentally changes the silicide nucleation mechanism and growth behavior. Figure 2 shows the silicide reaction in Si nanowire with a coherent ∑3 (111) twin boundary and with a nanowire axis along the <112> orientation (6). A leading and a lagging $NiSi_2$ interfaces are formed in the bi-crystal with a corner at their stepped edge. Fig. 2c-f shows a series of in-situ TEM snapshots providing direct evidence that a new $NiSi_2$ (111) plane nucleates at the TB, propagates on Si (111) plane at the leading interface and towards the edge surface of the NW (Fig. 1c-f), in a layer-by-layer manner. The new layer cannot directly propagate across the TB but rather remains in the same half of the twinned-bicrystal at which a nucleus was initially formed, and the new silicide nucleus does not form across the TB either. Nucleation at the corner edge, which is less energetically favorable than at the TB, then follows (Fig. 2g-j). The presence of surface grains and near surface stacking faults also accelerate the reaction and are the lowest energetically favorable nucleation sites (2).

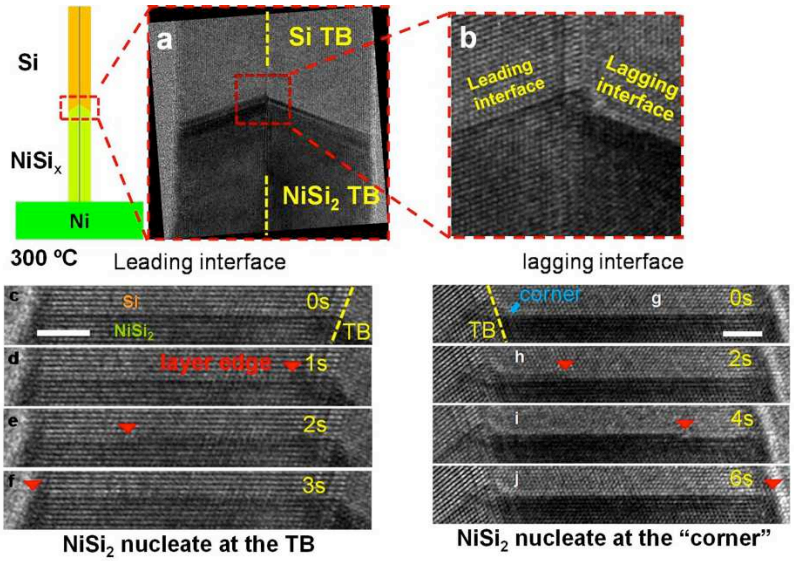

Figure 2. Reaction between Ni and a Si nanowire with a TB, marked by the dashed yellow line in (a). (b) Zoom-in image of the red dashed box in panel (a) showing asynchronous growth of a leading interface and a lagging interface. (c-f) Nucleation and propagation of a (111) $NiSi_2$ plane at the leading interface from the TB. Scale bar is 3 nm. (g-j) Asynchronous nucleation from the 'corner' interface between the silicided twin and unsilicided twin segment, and propagation of a (111) $NiSi_2$ plane at the lagging interface. Scale bar is 3 nm.

Ultra-short Channel Si Nanowire FETs

The reaction described above was utilized to form an ultra-short channel FET in a Si nanowire with a Si gap of 17 nm as shown in Figure 3. The undoped Si is characterized with a hole barrier height of ~ 0.4 eV with $NiSi_2$, and this translated to a threshold voltage shift in the transfer characteristics of the device (Fig. 3c). The SS^{-1} of this device is 350 mV/decade and is expected to be improved, together with a lower off-current, when a thinner nanowire diameter is used.

We have studied the channel length scaling in such Schottky barrier FETs for a set of 64 devices. To correlate the geometrical factors of the gate capacitance, we developed an empirical formula for Ω-gate capacitance, C_G^{Ω}, by curve fitting to capacitance values obtained from finite element simulations (1),

$$C_G^{\Omega}(h,r) = L_G\left[2\pi - 2\,\mathrm{acos}\left(\frac{1-h/r}{1+h/r}\right) + a\cdot\left(h/r\right) + b\cdot\left(h/r\right)^2\right]\varepsilon_0\varepsilon_r / \ln\left[1+h/r\right] \quad [1]$$

Here, r is the radius of the NW, h is the dielectric layer thickness, ε_r is the relative dielectric constant, a=2.086 and b=0.852 for the case of thin dielectrics in a Ω-gate configuration ($h/r<1$), and account for fringing fields, were fitted from the simulations.

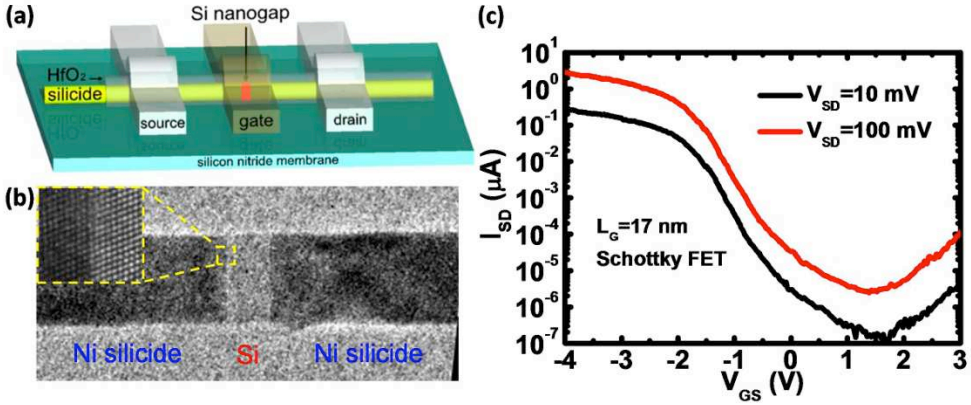

Figure 3. (a) Schematic of the fabricated ultra-short channel device. (b) A 17 nm gap (bright undoped Si segment in between the $NiSi_2$ dark segments) is formed. (c) Transfer curve from a FET fabricated on the nanowire in panel (b) showing good conductance modulation and expected threshold voltage shift as function of V_{DS} for this Schottky barrier FET device.

To compare different devices whose diameters vary in the range of 30 – 50 nm, we normalize our experimental transconductances with respect to the gate capacitance of a virtual reference device (40nm in diameter, top gate device with 10 nm HfO_2 gate dielectric) using the formula:

$$g_m^{normalized} = g_m \frac{C_G^{ref}}{C_G} \quad [2]$$

Both of the experimental and simulated devices (using Silvaco, ref. (1)) show deviation from the predicted enhancement of $g_m^{normalized}$ according to $g_m = \frac{\mu_h V_d C_G}{L_G^2}$, with shorter channel lengths, which is due to a dominant potential drop across the Schottky barrier region in the short channel device and consequently a thinner barrier that is less prone to gate modulation. In other words, the effective potential drop in the channel becomes very small, and the drive current and g_m are consequently degraded.

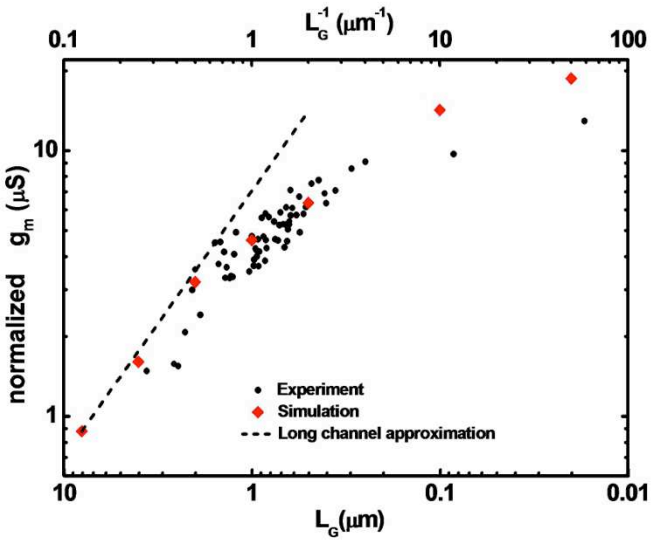

Figure 4. Double log plot of normalized maximum transconductance as a function of channel length. Each black small circle represents measured transconductance from an individual experimental device, and red diamonds represent extracted transconductance from simulated devices with different channel lengths. The dashed line describes the trend predicted by the long channel approximation.

Heterogeneous Reactions and FETs in Ge/Si Core/Shell Nanowires

Higher performance is expected from heterostructured nanowires with conformal shells that can provide carrier confinement and surface passivation (7). We have fabricated $Ni_2Ge/NiSi_x$-Ge/Si-$Ni_2Ge/NiSi_x$ metal-semiconductor-metal core/shell nanowire heterostructures with channel lengths down to 2 nm, and with different diameters. Figure 5 shows the precise control over the shell thickness as described elsewhere (3,8-10) and the transfer curves from a set of Ge/Si core/shell nanowires with different diameters. We observed that the on-current increases when a Si shell is deposited on the surface of the Ge core, and that the thinner the nanowire diameter is, the sharper is its turn-on characteristics with the lowest off-state current. We also observed electron conduction at positive gate voltages in these devices, termed as ambipolar behavior.

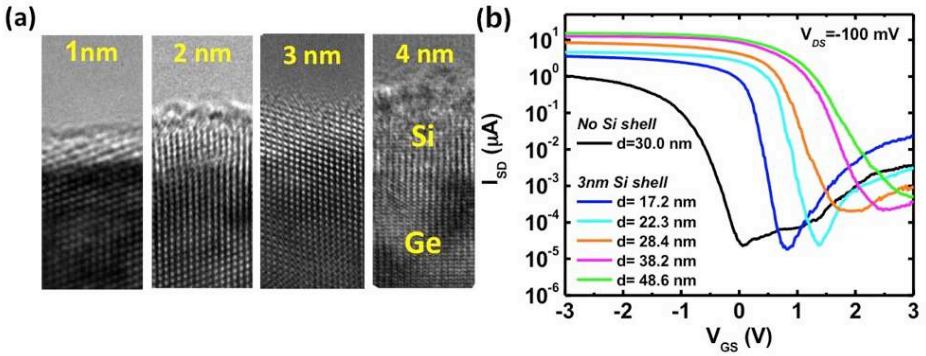

Figure 5. (a) Sections of Ge/Si core/shell nanowires with shell thicknesses of 1, 2, 3, and 4 nm. (b) Transfer curves of devices fabricated on different Ge core diameters and 3 nm Si shell thickness. Shown is also a transfer curve from a 30 nm Ge core diameter and without a Si shell for reference.

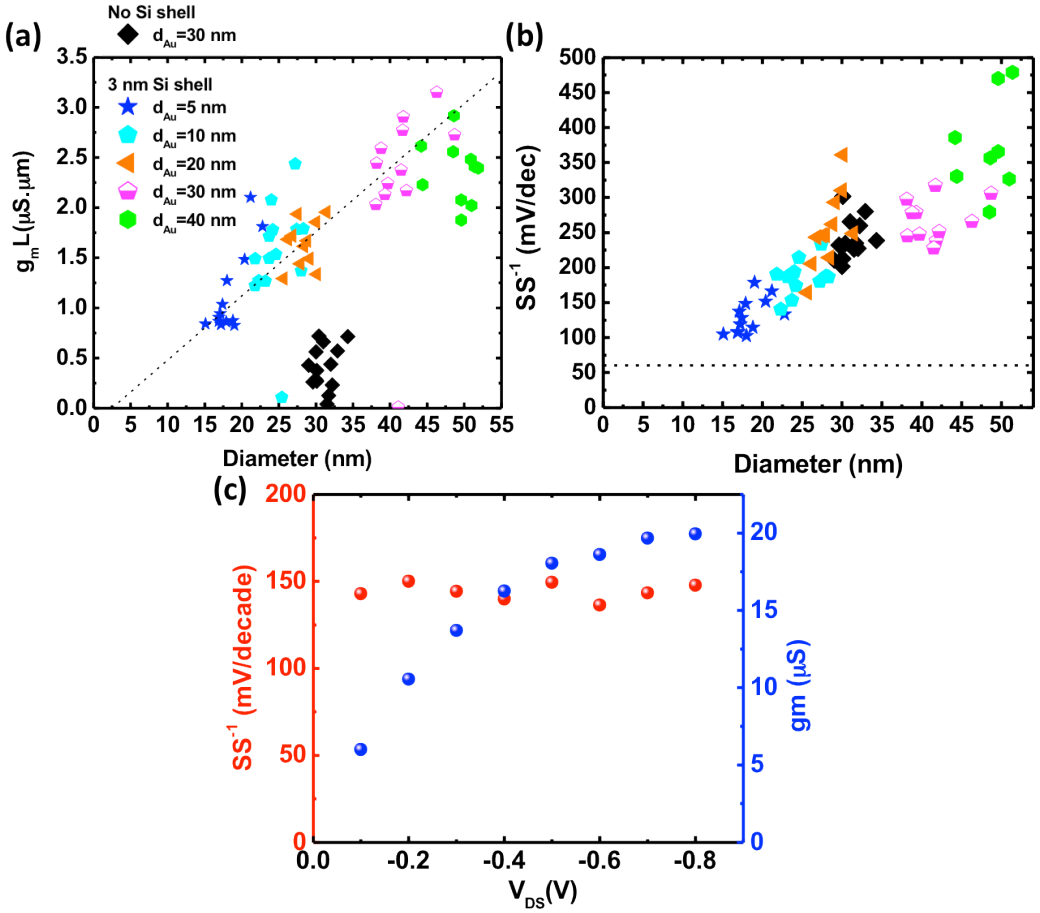

Figure 6. Performance assessment of $Ni_2Ge/NiSi_x$-Ge/Si-$Ni_2Ge/NiSi_x$ core/shell nanowires for different diameters: (a) Normalized transconductance, (b) inverse subthreshold slope, and (c) field-effect mobility. (d) SS^{-1} and g_m as a function of V_{DS}.

The unreacted channel length is ~ 250 nm on average. To account for small variations on performance of the measured devices, the channel-length corrected transconductance g_mL is plotted in Fig. 6 as a function of diameter, exhibiting linear increase with diameter as a consequence of increased circumference and increased gate capacitance. The Ge nanowires without any Si shell exhibited the lowest transconductances. The SS^{-1} increases nearly linearly with diameter where the sharpest turn-on characteristics are observed for smallest diameters. An SS^{-1}=102 mV/decade was measured for an 18 nm core diameter in a Ge/Si heterostructure FET with a maximum transconductance of 3.4 μS at V_{DS}=-100 mV. A lower bound of the hole field-effect mobility, μ, was calculated using the oxide/Si gate capacitance and without accounting for surface and interface states and was found to be insensitive to diameter, in the diameter range studied here. This is in contrast to our earlier studies on InAs nanowires which exhibited a reduced electron field-effect mobility with diameter due to surface scattering (11). Further, the field-effect mobility of Ge core only wires is much smaller than that of Ge/Si core/shell nanowires, which together with the insensitivity of μ for core/shell nanowires suggest the effectiveness of the surface passivation effects of our Si shells. For a constant Ge core diameter of 18 nm, the transconductance increases linearly and starts to saturate at relatively low V_{DS} presumably due to series resistance effects whereas the inverse subthreshold slope remains flat with V_{DS}.

Heterogeneous Reactions in Ge/Si Core/Shell Nanowires

The reaction between Ni and Ge/Si core/shell nanowires is characterized with a single dominant Ni_2Ge phase, in contrast to the profile seen in Fig. 1b for Si, and a Ni_2Ge (111) //Ge (111) interface. The phase of the thin $NiSi_x$ could not be determined. Despite NiGe has a lower nucleation energy barrier than $NiSi_x$, we observe that the $NiSi_x$ nucleates first and leads the reaction along the axis of the nanowire compared to Ni_2Ge (see Figure 8a). Without appropriate management of this problem, it establishes a limit over which ultra-short channel devices in Ge/Si core/shell nanowires could be realized. By removing the Si shell locally under the Ni contact to promote Ni_2Ge formation, simultaneous propagation of the Ni_2Ge and the $NiSi_x$ was accomplished as demonstrated in Fig. 8b. Abrupt $Ni_2Ge/NiSi_x$-Ge/Si-$Ni_2Ge/NiSi_x$ metal-semiconductor-metal heterostructured nanowires are achieved here with ~ 14 nm unreacted Ge/Si core/shell gap, and the technique has been successfully utilized to demonstrate 2 nm Ge/Si gap in the heterostructured nanowire.

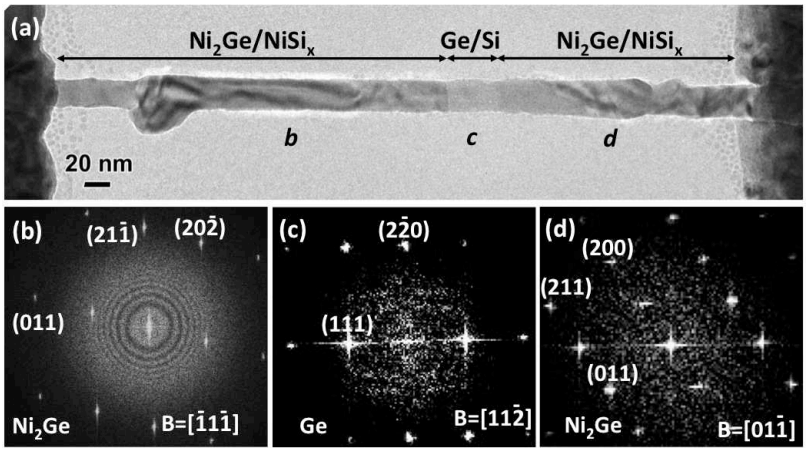

Figure 7. Phase sequence and FFT analysis demonstrating Ni_2Ge phase in the extension regions and a Ni_2Ge (111) //Ge (111) interface.

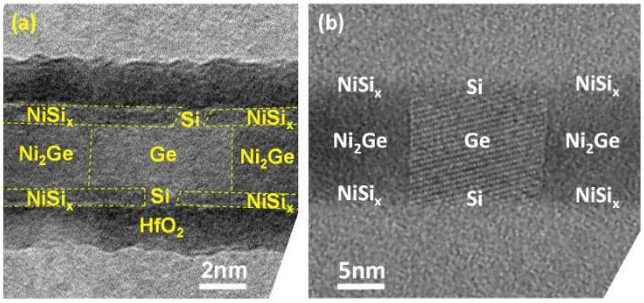

Figure 8. (a) Leading $NiSi_x$ interface in conventional and (b) simultaneous $Ni_2Ge/NiSi_x$ interface propagation in our approach.

Gate All Around Ge/Si Core/Shell Nanowire FETs

We developed a process for the conformal atomic layer deposition in a short pulse duration and a small number of pulses using trimethyl(methylcyclopentadienyl) Platinum(IV) precursor. This is accomplished by cycling tri-methyl aluminum for an optimal number of cycles to facilitate nucleation of Pt on pre-deposited HfO_2 dielectric. Figure 9 shows resultant gate all around Ge/Si/HfO_2/Pt core/multi-shell nanowire with $Ni_2Ge/NiSi_x$ source/drain regions extending underneath the Pt gate. The transfer curves

with V_{SD}=100 mV is shown in Fig. 9c showing modest performance. Reliability of these devices remains to be an issue, likely due the aqua-regia etch used to open the source/drain regions in Pt in order to provide access to the Ge/Si core/shell nanowire.

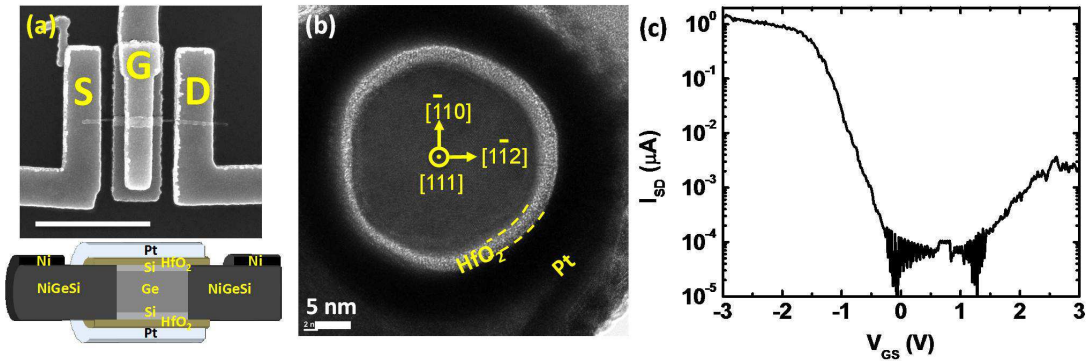

Figure 9. (a) SEM image of a gate all around Ge/Si core/shell nanowire FET with $Ni_2Ge/NiSi_x$ source/drain regions, and cross-section schematic along the length of the nanowire device. (b) Cross-sectional TEM image across the Pt gate region. (c) Transfer curve of a gate all around device at V_{SD}=100 mV.

Heterogeneous Integration with NiSi and Ni/III-V Reactions

The interest in integrating III-V materials to Si for alternative channel materials is well documented in the literature (13), and there are currently a variety of approaches to integrate the largely lattice mismatched materials together. Hybrid integration and wafer recycling remains a viable approach for both the integrated circuit and photovoltaic industries (14). We developed a fab-compatible process that allows the integration of III-V materials to Si using a NiSi all solid-phase reaction (15). Unlike eutectic bonding, this approach allows integration on surfaces with patterned Ni electrodes due to its solid phase character. Figure 10 demonstrates this integration for the case of Si on arbitrary substrates. An SiO_2/Si surface is chosen for ease of cleaving for cross-sectional SEM imaging.

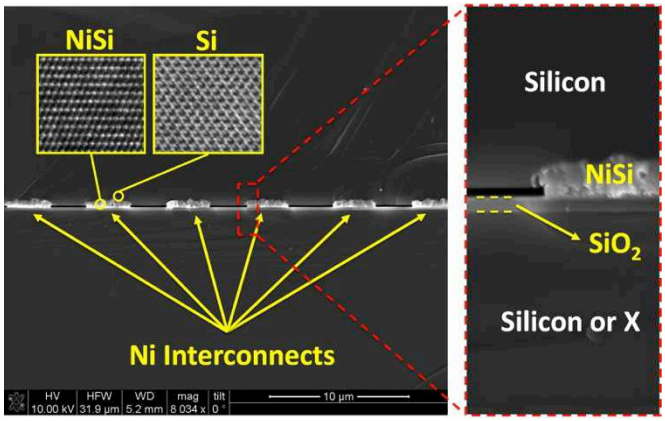

Figure 10. NiSi bonding on patterned Ni electrodes. A NiSi reaction through the diffusion of Ni into Si allows fusing Si substrates to any surface with patterned Ni atop.

Figure 11 demonstrates the successful bonding of InAs capped with a dielectric stack to a Si wafer using the NiSi reaction. The dielectric/InAs interface can be optimized/passivated prior to the bonding procedure and defect-free InAs on insulator on

Si can be realized using this wafer bonding approach. A Ni reaction between Ni layers deposited atop SiO_2/Si and an InAs layer has also been accomplished through the formation of NiInAs alloyed interface.

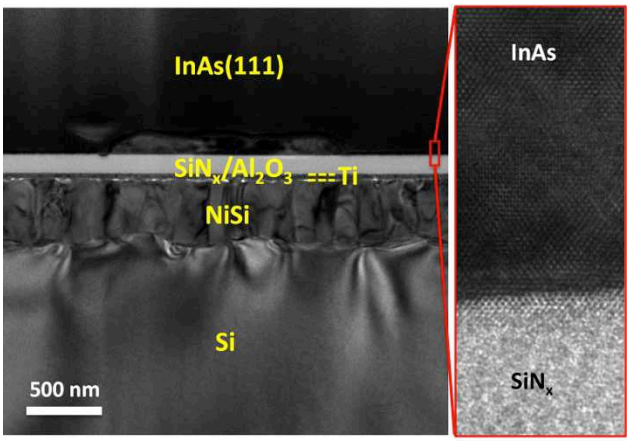

Figure 11. NiSi bonding of InAs layer to a Si substrate by a NiSi reaction.

InGaAs FinFETs on Insulator on Si

Using our wafer bonding scheme, we were able to integrate $In_{0.53}Ga_{0.47}As$ layers on insulator on Si, which was then subject to dry etching to pattern InGaAs Fins as demonstrated in Figure 12a. We further fabricated InGaAs FinFET devices on Si using this integration scheme. A cross-sectional TEM image of the fabricated structure is shown in Fig. 12b exhibiting the whole material stack from the Si substrate to the Ni metal tri-gate. Fig. 12c shows a HRTEM image at the InGaAs Fin showing a smooth etched interface (which was further processed after dry etching) with the HfO_2 gate dielectric. While demonstrated here for InGaAs channels, our process is compatible for integration of any III-V material with Si using a simple NiSi solid-phase reaction. The transfer curves of a fabricated device with L_G=450 nm at different V_{DS} biases is shown in Figure 13. For this device, I_{on}=5.3 μA/μm at V_{DS}=0.5V and V_{GS}-V_T=0.5 V and a DIBL of 50 mV/V were measured. The on-current for this device is limited by the series contact resistance due to a narrow contact pad (~ 100 nm) and the undoped InGaAs layer, with potential for improved performance with further structure and material optimization. The InGaAs FinFETs presented in Figs. 12-13 are the first of their kind that are fabricated on a Si substrate.

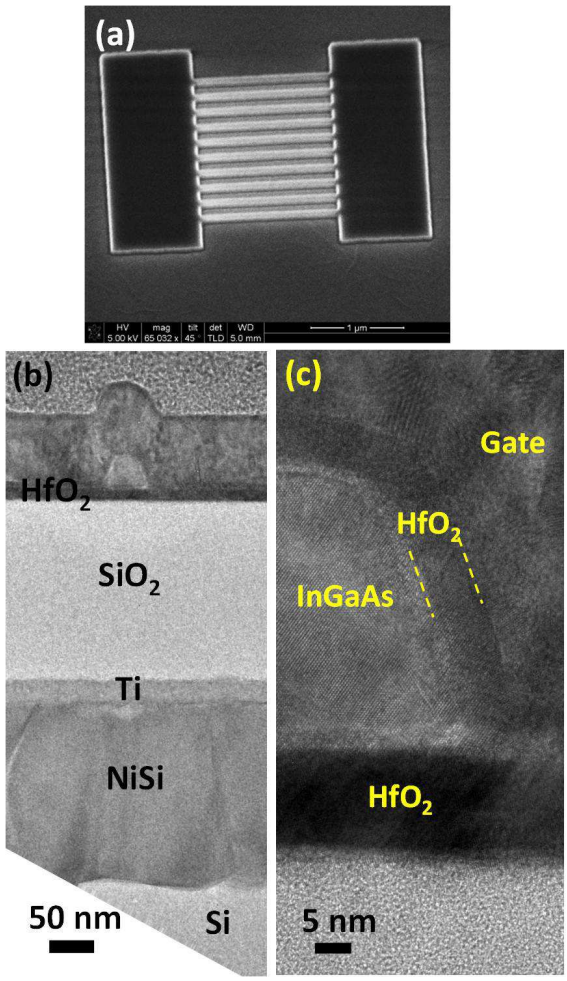

Figure 12. (a) SEM image of InGaAs Fins on insulator on Si. (b) Cross-sectional TEM across the gate of the fabricated InGaAs FinFET on Si. (c) HRTEM image showing single crystal InGaAs Fin with smooth interface with the HfO_2 gate dielectric.

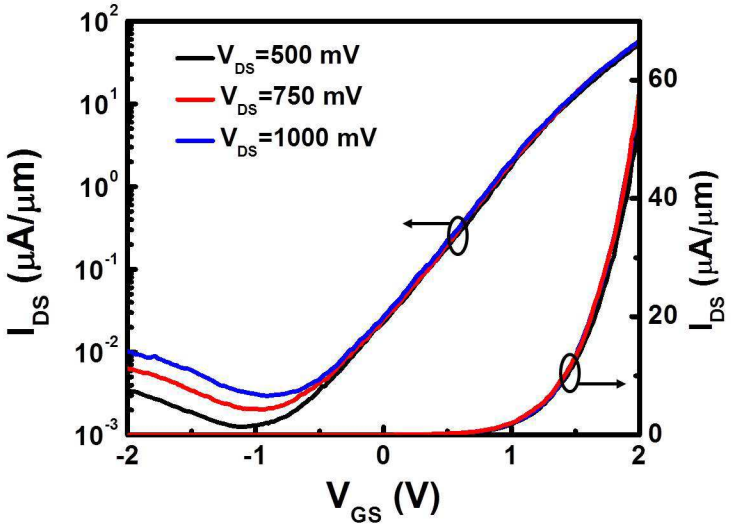

Figure 13. Measured transfer curves on log and linear scales for preliminary InGaAs FinFETs fabricated on insulator on Si.

Acknowledgments

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