Optimal Control over the InAs Nanowire Growth for System Integration and their Structural and Transport Properties

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Abstract – **We present new fundamental insights into the nucleation and evolution of InAs nanowires (NWs) grown using organo-metallic vapor-phase epitaxy (OMVPE), the correlation of their room temperature transport behavior with their structural properties, and a novel scheme for their integration to Si substrates. We experimentally distinguish, for the first time, two NW growth regimes defined by the direction of In adatom exchange between the NW (InAs) and the substrate (InAs (111)B). This understanding leads to optimal control over the NW morphology over length scales of the order of the In adatom surface diffusion length on the NW sidewalls. Transmission Electron Microscopy (TEM) analysis of the NW crystal structure of wurtzite (WZ) and zincblende (ZB) NWs is used to explain striking differences in their transport behavior. We find that the presence of small ZB sections in the WZ NWs can create spontaneous polarization sheet charges at each section interface along the NW channel, leading to improved subthreshold characteristics over those of pure ZB NWs, as observed in our electrical device measurements. Finally, we successfully demonstrate the vertical integration of electrically isolated InAs NWs on SiO_2 on Si suitable for implementing 3D NW circuits using the bottom-up synthesis approach for practical integration of III-V functional devices to Si technology.**

Keywords – InAs Nanowire, Microstructure, Wurtzite, Zincblende, Transport, Integration, III-V on Silicon.

I. Introduction

Quasi 1-dimensional semiconductor nanowires have been intensively studied in the past decade due to their potential for nanoscale electronics and photonics [1,2]. InAs NWs in particular have displayed high electron mobilities (10^3-10^4 $cm^2/V{\cdot}s$) [3,4,5], which together with the possibility of implementing wrap-gate FETs [5] places them at the forefront of material research for future high performance FETs. Systematic studies of the InAs NW nucleation and evolution [6], together with correlated microscopy and transport studies allows enhanced understanding as well as better control over their morphology and transport properties, and provides necessary background for integrating NWs into functional systems. In this work, we report new insights into the NW-substrate adatom exchange that enabled us to demonstrate optimal control over the InAs NW morphology. Furthermore, through transmission electron microscopy (TEM) and back-gate field effect transistors (FETs) transport analysis, we report direct correlation between the InAs NWs microstructure and their individual electronic transport behavior for wurtzite (WZ) and zincblende (ZB) NWs. Finally, we utilize this understanding and combine it with the ion-cut or (or Smart Cut®) layer transfer technique [7] to successfully demonstrate practical integration of vertical and electrically isolated III-V NWs to the standard Si mainstream.

II. Nanowire Synthesis and Morpholgy Control

We have grown InAs NWs in a home-built OMVPE reactor on InAs (111)B substrates from 40 nm-diameter Au nanoparticles (NPs). Tri-methyl-indium (TMIn) and arsine precursors in H_2 carrier gas were used to grow the InAs NWs at 100 Torr chamber pressure and 500 ˚C. We have studied the effect of TMIn flow rate on the NW morphology and rate of growth. Figs. 1 and 2 show *ex-situ* field-emission scanning electron microscopy (FE-SEM) images of InAs NWs grown at TMIn flow rates of 1 and 6 µmol/min, respectively, as function of time. Uniform NW diameter of 40 nm, dictated by the Au NP diameter, is obtained in the former case, whereas tapered NWs with large base diameters are obtained in the latter case.

For a TMIn flow rate of 1 µmol/min the NW length as function of time, shown in Fig. 3 (a), varies exponentially initially and becomes linear after 3 min. Fig. 3 (b) compares the NW lengths as a function of time for both TMIn flow rates. The higher TMIn flow rate results in a faster NW growth rate initially, but this decays to a rate comparable to that of the lower TMIn flow rate by 1.5 min. If we assume that the In adatom diffusivity from the substrate to the NW is negligible for the lower TMIn flow rate, then for short growth times, the collection area of In adatoms on the NW sidewalls increases as the NW length increases. This would result in the exponential NW elongation with time that was observed. In this case, pure Vapor-Liquid-Solid (VLS) NW growth occurs at the Au interface. Longer growth times result in NW lengths that exceed the In adatom diffusion length on the NW side walls. However, the collection area of In adatoms that can make it to the NW tip to contribute in NW elongation remains the same, resulting in linear increase of the NW length with time. In adatoms that are more than one diffusion length away from the NW tip either desorb from or adsorb to the NW sidewalls (Inset of Fig. 3 (a)). Thus, Vapor-Solid growth in addition to the VLS growth persists for longer growth times. The transition point from exponential to linear growth as a function of time allows us to determine the In adatom diffusion length on the NW surface, which we find to be ~ 1.5 µm at 500 ˚C. This is consistent with the length of the uniform NW segment near the tip for long growth times (Inset of Fig. 3 (a)).

Thus, we identify two distinct NW growth regimes: (i) Regime-I, negligible substrate to NW diffusion and uniform

NWs (within one In adatom diffusion length) can be grown. (ii) Regime-II, substrate to NW diffusion and lateral growth occur resulting in tapered NWs. In this latter regime, the collection area of In adatoms includes a portion of the substrate at the NW base, and the initial growth rate is non-exponential as was seen in Fig. 3 (b). The growth rates and the distinction between the two growth regimes is in excellent agreement with theoretical predictions made for whisker growth rates based on whisker-substrate adatom exchange [8]. Fig. 4 shows SEM images of different diameter NWs grown on the same substrate and at specified locations using e-beam lithography-patterned Au NPs. This illustrates the ability to specify location, diameter, and length of uniform morphology NWs based on insights gained from this growth study.

III. Correlation of Nanowire microstructure and transport behavior

In order to exploit the full potential of NWs, developing an understanding that correlates their crystal structure to their transport behavior is essential. We demonstrate such a correlation for ZB and WZ InAs NWs. OMVPE InAs NW growth was performed on SiO_2 substrates resulting in ZB NWs [9] and on InAs (111)B substrates resulting in WZ NWs [6]. Fig. 5 (a) shows a high resolution TEM (HR-TEM) image of a ZB InAs NW with its correspondent fast Fourier transform (FFT). In general, this type of NW consists of two twin segments separated by a grain boundary running along the <110> growth axis. Fig. 5 (b) shows a TEM image of a WZ InAs NW with its correspondent selective area diffraction pattern (SAD). This type of NW has numerous stacking faults perpendicular to its <0001> growth direction as well as small ZB sections.

Back-gate FETs fabricated from both types of wires have shown significant differences in their output (Fig. 6) and transfer (Fig. 7) curves. Specifically, the ZB NWs showed poor subthreshold characteristics with $I_{on}/I_{off} \sim 2$ and a lower contact resistance R_c=1480 Ω when compared to WZ NWs (I_{on}/I_{off} ~10^4, R_c=11280 Ω). Detailed device analysis [10] to extract the transport coefficients from 17 devices of both types of NWs have resulted in similar average values (μ_{FE}=2200 $cm^2/V{\cdot}s$, n=6.4x10^{17} cm^{-3} for ZB NWs, and μ_{FE}=1715 $cm^2/V{\cdot}s$, n=8.5x10^{17} cm^{-3} for WZ NWs). Energy band offsets for ZB/WZ heterostructure [11] has been used recently to explain differences in optical properties of rotationally twinned InP NWs [12]. Using Silvaco-Atlas two-dimensional (2D) device simulations, band offsets for the InAs ZB/WZ heterostructure ($|\Delta E_c|$=86 meV, $|\Delta E_v|$=46 meV, Fig. 8) cannot reproduce the trends observed in the subthreshold characteristics for both types of NWs.

It is known that hexagonal crystals have non-zero spontaneous polarization that will lead to polarization fields and charges at the opposite faces of the crystal [13]. The presence of such charges at the ZB/WZ hetero-interface lead to a saw-tooth type electric field along the axis of the WZ NW channel (Fig. 8) that compensates surface accumulation charges and leads to full depletion of the channel at negative V_{GS}. Using 2D Atlas simulations with a surface state density of 10^{12} cm^{-2} [14], the extracted transport coefficients from above for the 2 types of NWs, and a spontaneous polarization charge density of 10^{13} cm^{-2} for the WZ NW, we were able to reproduce the trends observed in the transfer curves. This value is within the lower limit of spontaneous polarization charges for other hexagonal materials such as nitrides and zinc oxide [15]. Fig. 9 shows the simulated transfer characteristics of both device structures showing larger I_{on}/I_{off} ratios for the WZ NWs. The I_{on}/I_{off} ratios in Fig. 10 are lower than those of Fig. 7 due to short channel effects in the 400 nm channel (back-gate device t_{ox}=100 nm) , and the current values are lower than the experimental ones due to the underestimated field-effect mobility in the presence of surface states [1,14]. Nonetheless, the observed trends in the subthreshold characteristics are in agreement with the experimental ones and imply that spontaneous polarization charges in WZ III-V NWs have direct impact on the electronic and optical properties of such hexagonal NWs.

IV. Practical Integration of III-V Nanowires to Silicon substrates

Several approaches have emerged to integrate NWs into functional systems including micro-fluidic [16] and dielectrophretic [17] manipulation, dry [18] and bubble blow transfer [19]. While these approaches may be suitable for heterogeneous integration that requires low temperature processing, such as integration to flexible substrates, none of these integration techniques is suitable for practical fabrication of dense and high performance devices that may compete with current planar devices. Vertical wrap-around gate transistors are promising candidates for future technology nodes [20]. However, such vertical integration utilizes conducting substrates (InAs NWs on InAs substrates [5, 20] and III-V NWs on Si [21]) that prohibit single NW device addressing and isolation as well as the feasibility of multi-functions per chip. It has been argued that future technology nodes should make use of advancement of Si technology mainstream and thus, promising high performance devices should be integrated to Si substrates.

Here, we develop and implement a novel integration scheme for III-V NWs to Si substrates that allows vertical integration, electrical isolation, and individually addressable III-V NWs on Si for 3D circuit applications. This integration scheme utilizes the smart-cut® technique [7] – typically used for producing Silicon-on-Insulator (SOI) wafers – to transfer InAs (111)B layers onto SiO_2/Si. In brief, InAs (111)B wafers are implanted with Hydrogen ions to a projected range of 170 nm below the surface and bonded via Van der Waals forces to a 70 nm SiO_2 layer on Si at T ~ 70 ˚C. Further temperature annealing to T ~ 110 ˚C leads to H-platelets nucleation, growth, and eventual exfoliation of the donor InAs (111)B substrate around the projected range of hydrogen. Thus a thin film of InAs with a thickness of ~170 nm is transferred onto SiO_2/Si. Fig. 10 shows a cross-sectional FE-SEM image of the final bonded structure. Consequent wet etching and InAs thin film re-growth are utilized to planarize and activate the surface for NW growth. We then have performed OMVPE growth of InAs NW

arrays at specified locations utilizing e-beam patterned Au dots. Another e-beam lithography and alignment followed to mask the NWs and etch InAs islands at the NW base as shown in Fig. 11. This results in vertical and electrically isolated InAs NWs on SiO_2/Si suitable for high performance 3D III-V circuits on Si with simple device architecture and physics of operation.

V. Conclusions

In conclusion, we have demonstrated optimal control over the InAs NW morphology through surface kinetics and experimentally distinguished, for the first time, between two NW growth regimes depending on the substrate-NW adatom exchange. Uniform InAs NW morphology is feasible for NW lengths ≤ 1.5 μm, the surface diffusion length of In adatoms on the NW sidewalls. In addition, we have correlated the microstructure for ZB and WZ InAs NWs with their transport properties and have shown that spontaneous polarization induced charges in the WZ twinned NWs lead to improved subthreshold characteristics over those of pure ZB NWs. To bring this understanding together for functional systems, we have developed and demonstrated a novel integration scheme that allows vertical, yet individually addressed high performance III-V NWs on Si substrates. These results aid in the understanding and controlling the growth and transport properties of III-V NWs and illustrate a practical scheme for their integration.

Acknowledgments

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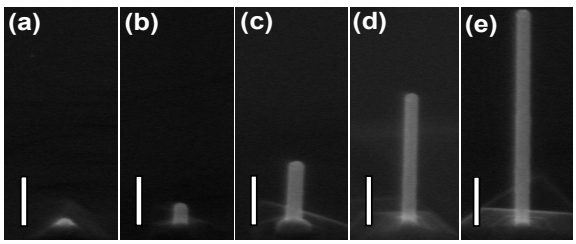

Figure 1: 45˚ angle view SEM images of InAs NWs grown at a 1 μmol/min TMIn flow rate at 500 ˚C for (a) 30 s, (b) 60 s, (c) 90 s, (d) 120 s, and (e) 150 s. Scale bars are 280 nm.

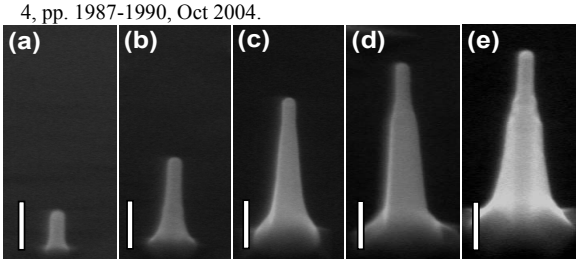

Figure 2: 45˚ angle view SEM images of InAs NWs grown at a 6 μmol/min TMIn flow rate and 500 ˚C for (a) 10 s, (b) 20 s, (c) 30 s, (d) 40 s, and (e) 50 s. Scale bars are 280 nm.

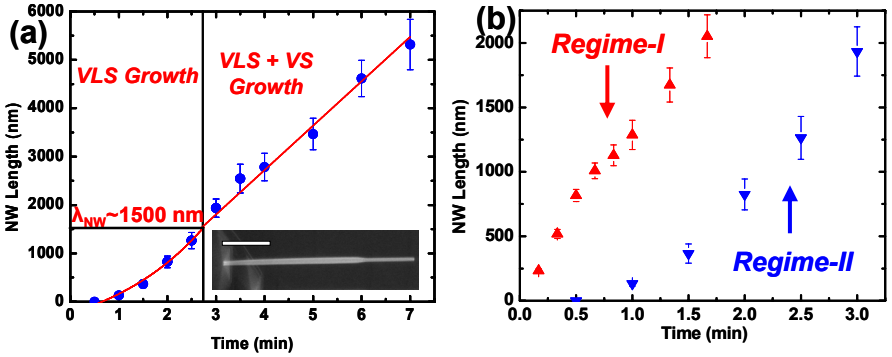

Figure 3: (a) Plot of the NW length as function of time and correspondent growth mode at TMIn flow rate. (b) Plot of the NW length as function of time showing the 2-growth regimes at 2 different TMIn flow rates. Inset in (a) is a FE-SEM of an InAs NW grown for 7 minutes. Scale bar is 1.41 µm.

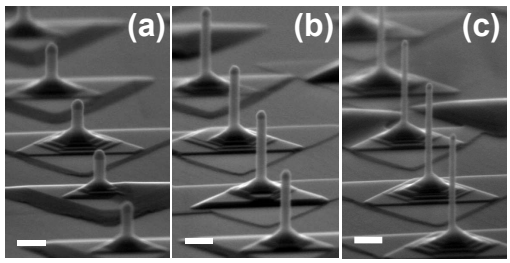

Figure 4: 45˚ angle view FE-SEM images of InAs NWs grown at predefined locations on the same substrate with different diameters (a) 90 nm, (b) 70 nm, and (c) 45 nm. Scale bars are 280 nm.

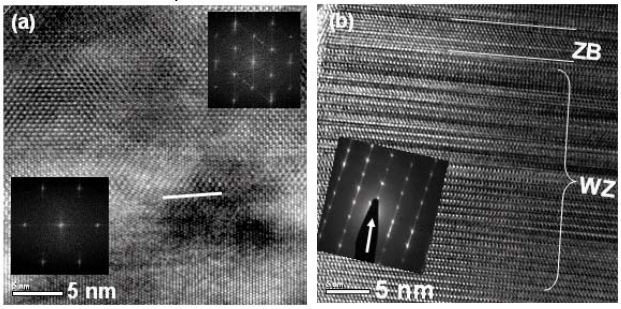

Figure 5: HR-TEM images of InAs NWs (a) ZB NW with a grain boundary along its axis and (b) WZ NW with stacking faults and a small ZB segment perpendicular to its axis. Insets are correspondent FFTs in (a) and SAD pattern in (b).

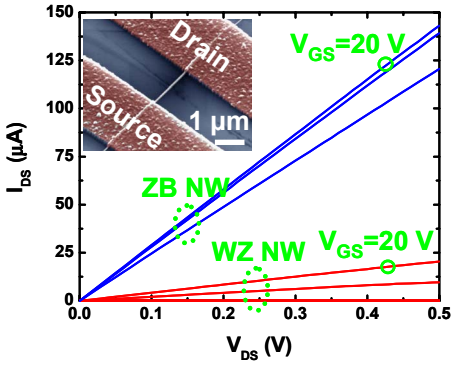

Figure 6: Output curves of back-gate ZB and WZ InAs NWFETs with L_{SD}= 3.6 µm (V_{GS}=20, 0 and -20 V). Inset is a representative FE-SEM image of a back-gate InAs NWFET.

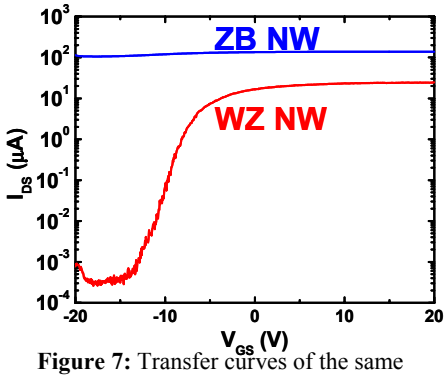

Figure 7: Transfer curves of the same devices in Figure 6 at V_{DS}=0.5V.

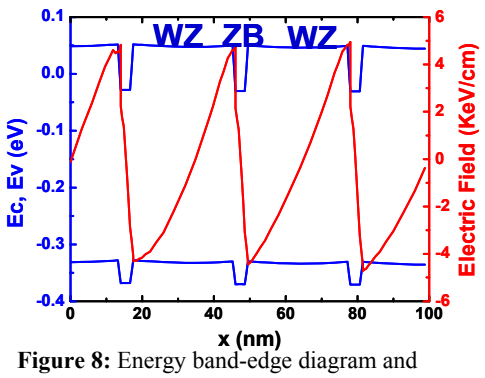

Figure 8: Energy band-edge diagram and spontaneous polarization field across the WZ NW channel.

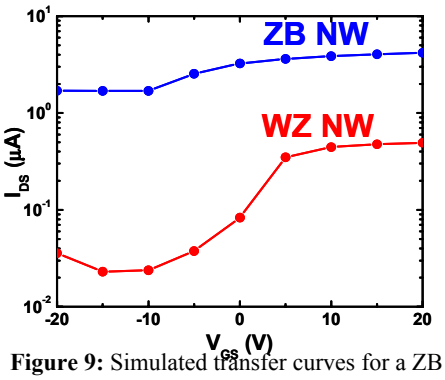

Figure 9: Simulated transfer curves for a ZB and a WZ (with ZB segments) NWFETs with 400 nm channel length at V_{DS}=0.1V.

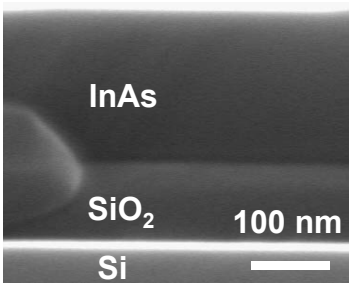

Figure 10: Cross-sectional view of a bonded InAs layer through the smart-cut technique.

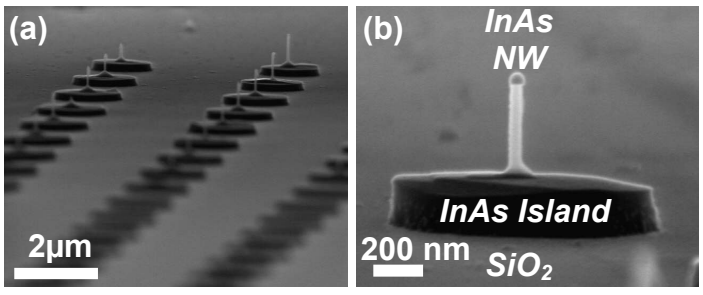

Figure 11: (a) 45˚ angle view FE-SEM image of an array of vertically aligned InAs NWs atop of InAs islands on SiO_2/Si substrate. (b) Zoom in FE-SEM image of a single NW in the array shown in (a).