Proceedings of 10th IEEE International Conference
on Nanotechnology Joint Symposium with Nano Korea 2010
August 17~20, KINTEX, Korea

Synthesis, Fabrication, and Characterization of Ge/Si Axial Nanowire Heterostructure Tunnel FETs

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***Abstract*- Axial Ge/Si heterostructure nanowires allow energy band-edge engineering along the axis of the nanowire, which is the charge transport direction, and allows the realization of novel asymmetric device architectures. This work reports on two advances in the area of heterostructure nanowires and tunnel FETs: (i) the realization of 100 % compositionally modulated Si/Ge axial heterostructure nanowires with lengths suitable for device fabrication and (ii) the design and implementation of Schottky barrier tunnel FETs on these nanowires for high-on currents and suppressed ambipolar behavior. Initial prototype devices resulted in a current drive in excess of 100 µA/µm ($I/\pi D$) and 10^5 I_{on}/I_{off} ratios. These results demonstrate the potential of such asymmetric heterostructures (both in the semiconductor channel and at the metal-semiconductor interfaces) for low-power and high performance electronics.**

I. Introduction

While new materials and device concepts are being developed to extend CMOS device scaling beyond the 22 nm node, the potential of combining Si/Ge heterostructure materials with the dimensionality of semiconductor nanowires (NWs) remains to be explored. The vapor-liquid-solid (VLS) synthesis allows modulation of doping and alloy composition in the axial NW direction which is the transport direction for NW FETs [1]. This provides an additional degree of freedom for band-gap engineering in the axial direction, which when added to Ge compatibility for integration with Si technology [2], gives Ge/Si axial NW heterostructures advantages over other existing NW material systems and suggests superior device performance, in particular for tunnel FETs.

Prior work on the synthesis of Ge/Si NW axial heterostructures through the VLS mechanism have resulted in axial $Si/Si_{1-x}Ge_x$ NW heterostructures with x_{max} ~ 0.3 [3,4]. Synthesis of such NW materials is limited due to the difference in the decomposition temperatures of SiH_4 and GeH_4, which are ~ 650 ºC [5] and ~ 280 ºC [6], respectively. Due to the difficulty in their synthesis and control over their composition, no useful devices have been demonstrated from such heterostructure NWs. Recently, 100 % composition modulation of Ge/Si axial NW heterostructures was demonstrated using a solid growth catalyst [7]. In this case, the thickness of the heterostructure cannot exceed few atomic layers due to the slow axial growth rate and concurrent radial deposition on the NW sidewalls leading to a mixture of axial and radial heterostructures.

Here, we report the VLS growth of 100 % doping and composition modulated axial Ge/Si heterostructure NWs with lengths appropriate for device fabrication. We devised a growth procedure that eliminates Au diffusion on the NW sidewalls and minimizes random kinking in the heterostructure NWs as deduced from detailed microscopy analysis. Tunnel FETs made from these axial NW heterostructures have shown promising performance and current drives well beyond what has been accomplished before with semiconductor NWs [8] and carbon nanotubes [9].

II. Heterostructure Nanowire growth

Growth of the Ge/Si axial NW heterostructures was carried out in a cold-wall chemical vapor deposition system using GeH_4 (30 % in H_2) and SiH_4 (50 % in H_2) as input precursors and variable size Au colloids as growth seeds. Doping was achieved with the introduction of B_2H_6 (100 ppm in H_2) and PH_3 (100 ppm in H_2) as p- and n-type dopants for the Ge and Si segments, respectively. The growth of Ge NWs was carried out in a two-temperature step process (366 °C nucleation and 276 °C elongation) whereas the growth of the Si segment was carried out at 430 °C – catalyzed at such a low temperature by the Au growth seed with ~ 300 nm intrinsic segment length followed by an n-type Si segment growth of ~ 1 µm length.

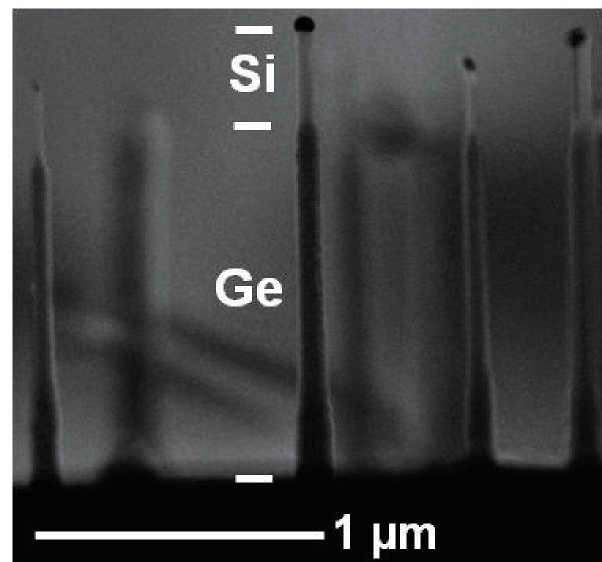

Fig. 1. a) SEM image of epitaxially grown Ge/Si axial NW heterostructures on a Ge(111) substrate.

This work was performed, in part, at the Center for Integrated Nanotechnologies, a U.S. Department of Energy, Office of Basic Energy Sciences user facility at Los Alamos National Laboratory (Contract DE-AC52-06NA25396) and Sandia National Laboratories (Contract DE-AC04-94AL85000). SAD and STP are with Los Alamos National Laboratory, Los Alamos, NM, and JH and AG are with Sandia National Laboratories, Albuquerque, NM. (*corresponding –author, phone: +15056659030; E-mail: shadi@lanl.gov).

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To nucleate the Si segment, an intermediate precursor switching step was necessary. This is depicted in Fig. 1 which shows an SEM image illustrating the successful growth of epitaxial 100 % Ge/Si axial heterostructures (confirmed by EDS line scans) on a Ge(111) substrate. While the growth of such heterostructures is viable by inserting a precursor switching step that maintains a liquid nucleating growth seed, the growth seed remains unstable atop the NW, leading to Au diffusion that tend to decorate the NW surface (Fig. 2a). By adjusting the duration of this intermediate step, the total temperature ramp time and precursor pressure, Au diffusion on the NW sidewalls was eliminated as demonstrated in the TEM and STEM images of Fig. 2b-e. In general, the NWs grown using this growth procedure are straight up to lengths of ~ 300 nm after which the NWs kink by ~ 20 ° from their axis, which is typically a transition from the [111] orientation into the [211] orientation. Detailed TEM microscopy on these NWs have shown that there is a single fault that can be generated at a time in the Si segment (typically a stacking fault) and that the NW kinks when a [111]/[211] twin boundrary, which has ~ 20 ° between both directions, nucleates at the edge of the NW. This has also been verified by selective area diffraction patterns on different regions across the NW length (not shown here).

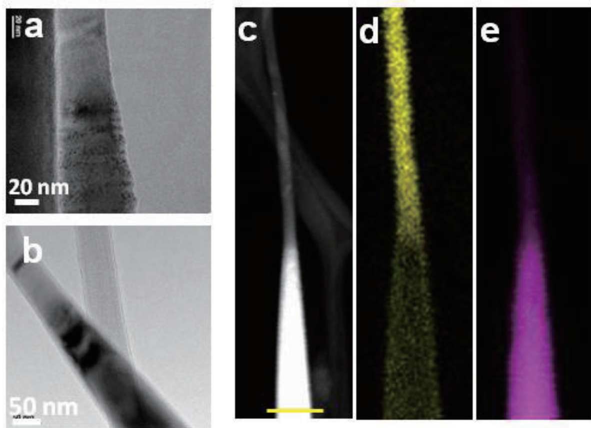

Fig. 2. a,b) TEM images at the interface of a 40 nm diameter Ge/Si axial NW heterostructure with (a) and without (b) Au clusters at the interface with new growth sequence. c) STEM image of a Ge/Si NW showing distinct contrast between Ge (bright) and Si (dark) with false color maps of Si (d) and Ge (e).

The Abruptness of the Ge/Si p-n junction can be tuned by the NW diameter. Indeed, we have observed that the transition length in our Ge/Si axial NW heterostructures is characterized by a logarithmic decrease of the Ge content that is also diameter dependent. Since the growth of these NWs is mediated by a liquid particle that acts as a reservoir for growth reactants, theoretical modeling of the incorporation rates when the material precursors are switched have predicted such a dependence [10]. This sets the minimum transition width for VLS grown heterostructure NWs which depends on NW diameter. There is also a thermodynamic limit below which VLS growth of NWs doesn't occur [11]. Growth from a solid seed does not rely on the dissolution of the input reactant into the particle itself but rather upon diffusion of reactants at the seed/NW interface, leading therefore to an abrupt interface [7]. However, the length scales at which these interfaces can be formed by the VLS mechanism is sufficiently abrupt to be very useful for developing band-gap engineered tunnel devices beyond those typically populated in the literature as we demonstrate below.

III. Asymmetric Band-gap engineered Tunnel FETs

Band-to-Band tunnel FETs (TFETs) have been recently proposed to overcome the minimum inverse subthreshold slope (SS^{-1}) of 60 mV/decade with experimental demonstrations of ~ 53 mV/decade and ~ 216 mV/decade in Si [12] and $In_{0.53}Ga_{0.47}As$ [13], respectively. These devices however suffer from ambipolar tunnel transport in the nearly symmetric tunnel barriers at the source and drain regions. Heterostructure TFETs (HTFETs) have been proposed for improved performance with Si/Ge [14] and in III-V [15] material systems. In the context of semiconductor NW VLS growth, obtaining an abrupt doping profile is as challenging as achieving the abrupt composition profile discussed in section II. Thus, to attain the benefit of the of the 3D geometry of the semiconductor NW, which allows the formation of wrap-around gates, we propose Schottky-barrier HTFETs for which an abrupt junction could be formed at the metal/semiconductor interface allowing additional benefits for band-gap engineering. The band-edge profile at thermal equilibrium of an optimal asymmetric device (validated by 3D Silvaco Atlas simulations) is shown in Fig. 3a. Design considerations for establishing this device architecture take into account not only the graded band-edge profile across the transition region between a Ge source and a Si drain but also the presence of band-offsets at the Schottky contacts that have to be accommodated for I_{on}/I_{off} currents and lowest possible ambipolar behavior. In brief, a small electron barrier at the source side results in dominance of thermally emitted electrons into the channel, reduced overall channel field (determined by band offsets at the two Schottky contacts) and therefore non-steep subthreshold characteristics. A large hole barrier at the drain side leads to accommodation of the band-offsets mainly at the valence band on the drain side, which will result in a high electric field and hole tunneling that raises the hole ambipolar transport branch at negative gate voltages. Fig. 3b shows the simulated transfer characteristics of a nanowire channel with a band-edge profile similar to that in Fig. 3a as well as for a pure Ge channel. It can be seen from Fig. 3b that the asymmetric HTFET leads to a higher I_{on}/I_{off} ratio and reduced ambipolar behavior. A small underlap (drain-to-gate separation) near the drain side can result in further reduction of the ambipolar behavior at negative gate biases.

IV. Device Fabrication and Transport Results

The as-grown nanowires were suspended in an isopropanol solution and then drop-cast onto a SiO_2/Si surface prepared with a pre-patterned grid for position mapping. Subsequent e-beam lithography and evaporation were performed to deposit Ni contact electrodes. NiGe and NiSi contacts were formed

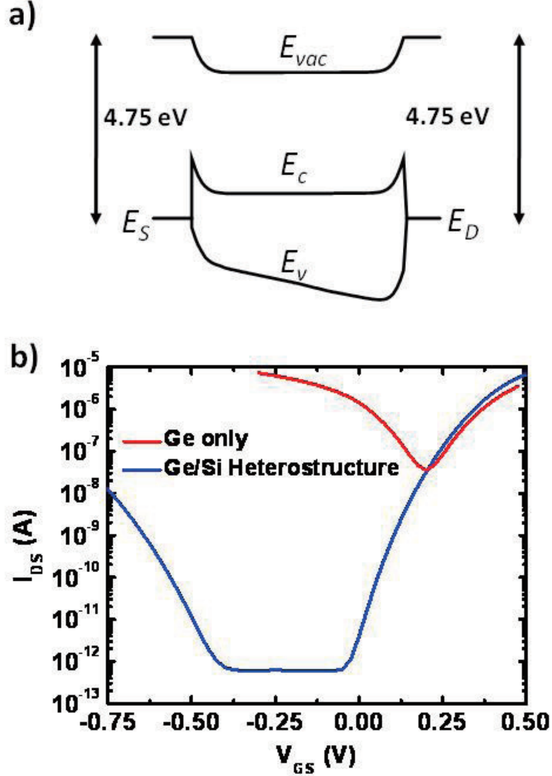

Fig. 3. a) Band-edge profile of an asymmetric Ge/Si HTFET allowing band-gap engineering at the source/drain electrodes. b) Simulated transfer curves for a 30 nm diameter Ge/Si heterostructure with 300 nm channel length together with a similar structure made of pure Ge.

afterwards by rapid thermal annealing (RTA) for 30 s at 300 °C followed by PECVD deposition of 10 nm SiN_x gate dielectric. Another e-beam lithography step was performed to pattern a gate electrode and Ti/Au metal gate was evaporated followed by lift-off. Fig. 4 shows SEM images of a single Ge/Si axial NW heterostructure prior to and after metal contact fabrication.

Fig. 5 shows typical transfer curves measured on these axial Ge/Si HTFETs. Current modulation over five orders of magnitude and a high on-current of ~ 7 µA were measured and a subthreshold slope of ~ 170 mV/decade was estimated. We note that both forward and reverse biased devices resulted in such transfer curves with higher current drives for the forward-bias case. NiSi is known to form a ~ 0.74 eV electron Schottky barrier height on Si [16] whereas NiGe has ~ 0.52 eV electron Schottky barrier height on Ge [17]. We expect that the high p-doping at the Ge side prevent the gate field from effective

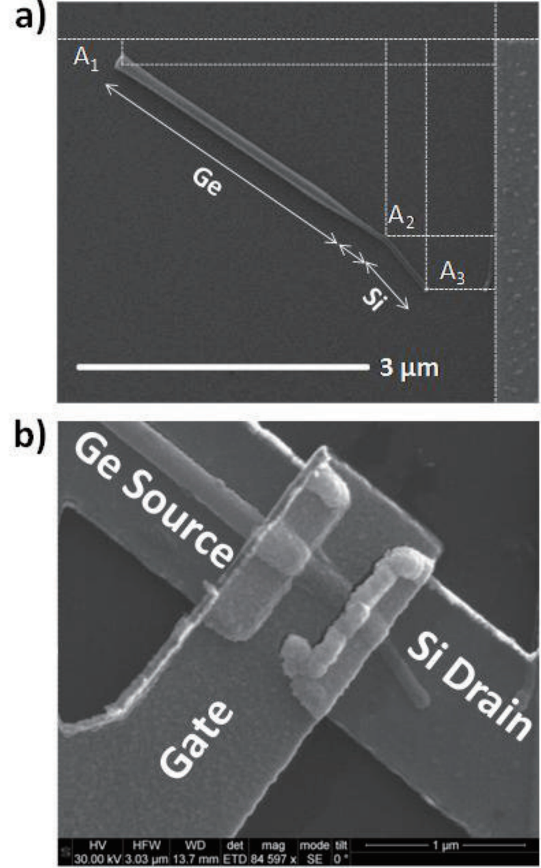

Fig. 4. a,b) SEM images of a Ge/Si axial NW heterostructure before (a) and after (b) HTFET fabrication.

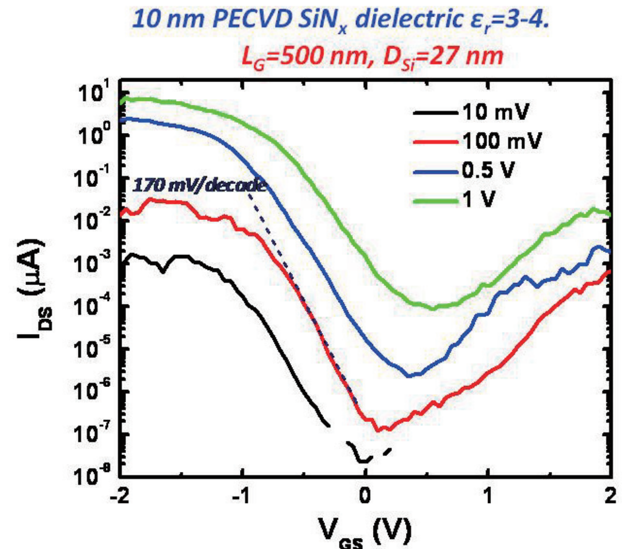

Fig. 5. Room temperature transfer curves of a Ge/Si axial HTFET.

modulation of the barrier heights at the Schottky contacts on the Ge side for both gate polarities, or the charge carrier

density in the Ge NW itself. In contrast, modulation of the current in the Si segment is effective with on-currents extending to ~ 10 nA and ~ 3 orders of magnitude I_{on}/I_{off} ratios. With such gate response in both segments, and with the barrier heights as indicated above, we expect that the band-offsets created by the Ge/Si axial heterojunction and the Schottky contacts lead to the observed enhancement in the HTFET transfer curves. Thus, the high doping of the Ge side confines most of the gate action and band-edge modulation to the Si segment of the wire. As such, a negative gate voltage will result in electron tunneling from the NiSi contact into the Si segment of the wire and subsequent drift toward the NiGe contact. A positive gate voltage leads to mild carrier modulation and drift of holes from the Ge segment of the device toward the NiSi contact. Additional studies are being carried out to confirm this interpretation. While further optimization is anticipated to enhance the performance of the fabricated devices and shed further light on their transport mechanism, we demonstrate HTFET devices with high on currents and exhibit 5 orders of magnitude I_{on}/I_{off} ratios for different V_{DS} biases. This behavior reinforces the hypothesized band-edge profiles of the Ge/Si NW heterostructure used in this study.

V. Conclusion

We have grown 100 % composition modulated Ge/Si axial NW heterostructures, and designed and fabricated asymmetric tunnel FETs from these NWs. Improved performance over their bulk counterpart and over homogenous NW TFETs is demonstrated here by utilizing band-gap engineering in the transport direction, only possible through the VLS growth mechanism. High on currents of the order of 10 μA (100 μA/μm), and 5 orders of magnitude I_{on}/I_{off} ratios have been measured with inverse subthreshold slopes of 170 mV/decade. These promising results not only highlight the potential of Ge/Si axial NWs in novel device designs but also prove competitive in the area of tunnel FETs. We anticipate that further use of high-k dielectrics and finer control over the device architecture will further enhance the subthreshold characteristics of these devices.

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