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Axial Ge/Si Nanowire Heterostructure Tunnel FETs

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The vapor-liquid-solid (VLS) growth of semiconductor nanowires allows doping and composition modulation along their axis and the realization of axial 1D heterostructures. This provides additional flexibility in energy band-edge engineering along the transport direction which is difficult to attain by planar materials growth and processing techniques. We report here on the design, growth, fabrication, and characterization of asymmetric heterostructure tunnel field-effect transistors (HTFETs) based on 100 % compositionally modulated Si/Ge axial NWs for high on-current operation and low ambipolar transport behavior. We discuss the optimization of band-offsets and Schottky barrier heights for high performance HTFETs and issues surrounding their experimental realization. Our HTFET devices with 10 nm PECVD SiN_x gate dielectric resulted in a measured current drive exceeding 100 μA/μm ($I/\pi D$) and 10^5 I_{on}/I_{off} ratios.

Introduction

The bottom-up synthesis (1) and top-down processing (2) of semiconductor nanowires (NWs) provide 1D nanostructures with unusual characteristics and significant potential for new device performance due to quantum confinement in 2D, novel 3D device architectures, and material hetero-epitaxy with coherency limits exceeding those of identical planar counterparts (3,4). With top-down processing to define lateral 1D channels, one is limited by the starting material composition, which is typically grown by chemical vapor deposition (CVD) techniques. On the other hand, vapor-liquid-solid NW growth allows modulation of composition and realization of band-edge engineered structures along the axis of the NW which is the transport direction. This attribute together with the small dimensionality of NWs and the compatibility of Ge/Si with Si technology, make Ge/Si axial NW heterostructures an attractive platform for exploring basic device physics in nanoscale heterostructures and the resulting performance gains, as illustrated in this work.

Growth of Ge/Si heterostructure NWs by CVD can be challenging due to the different decomposition temperatures of GeH_4 and SiH_4 sources, thereby creating instabilities in the growth during switching of the precursors and limiting the yield. These effects have limited successful axial SiGe heterostructures to a maximum compositional modulation of ~30 % in earlier work (5,6). By carefully controlling the growth conditions and precursor switching sequence (7), we are able to grow 100 % composition modulated Ge/Si axial heterostructure NWs with high yield. Fig. 1 shows representative scanning electron microscope (SEM) images and compositional maps of Ge/Si axial heterostructured NWs. In general, the Si segment exhibits a crystallographic kink and change of growth direction from <111> to <211> growth orientations through the nucleation of a <111>/<211> twin boundary (6). This crystallographic kink allows us to

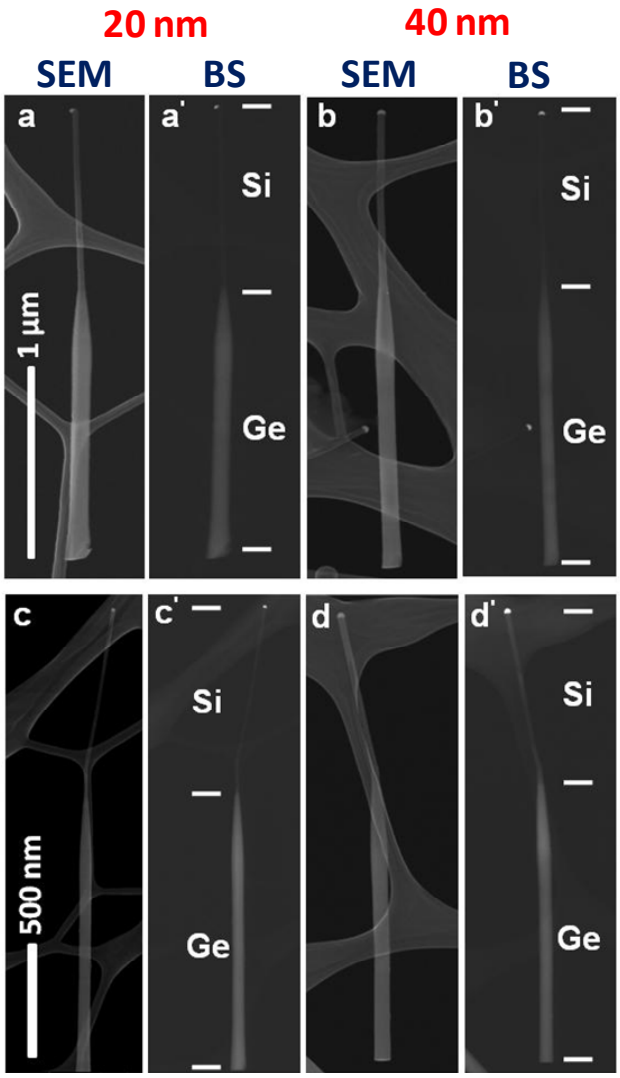

Figure 1: Axial Si/Ge heterostructured nanowires; a, b), secondary electron microscope (SEM) and a', b') back scattering (BS) compositional map images of straight Ge-Si axial NW heterostructures grown from 20 nm (a, a') and 40 nm (b, b') Au colloids. c, d) SEM and c', d') BS compositional map images of mostly observed kinked Ge-Si axial NW heterostructures grown from 20 nm (c, c') and 40 nm (d, d') Au colloids.

determine the location of the pure Ge, pure Si, and the graded SiGe transition segment in between both and therefore aids us in placing contacts to the heterostructure NW as required by device design. The graded SiGe transition region, whose length scales with the NW diameter, is a direct consequence of using a liquid metal catalyst which acts as a reservoir that expels material "A" gradually as material "B" is introduced for the growth of an "A/B" heterostructure. As a result a transition region is formed in the axial direction, with the extent of the transition increasing with increased solubility of species A and B in the liquid catalyst at the growth temperature. A similar effect is found for changing the doping along the axis, such that doped interfaces were shown to be diffuse in VLS grown NWs (8). Since the performance of tunnel FETs, that are capable of sub-60mV/decade inverse subthreshold slopes, is determined by abruptness of doping profiles, it is hard to achieve such ultimate performance in these structures. Therefore we turn our focus in this work to the "ideal" abrupt interfaces that can be formed at the metal/semiconductor

contacts. In this scenario, the Ge segment can be utilized as the high efficiency tunneling source and the Si segment as the ambipolar transport suppressor drain (9). The barrier heights at either side can also be adjusted to create/compensate built-in fields in the channel to assist in obtaining high I_{on}/I_{off} ratios as we describe below.

HTFET Design

To gain insight into the physics of operation of the asymmetric Ge/Si NW HTFET, we used 3D Silvaco Atlas simulations with device dimensions similar to those used in our experiments. These simulations are utilized to obtain the optimal energy band-edge design and understand their effects on the on-currents and ambipolar behavior. They are not intended to extract exact solutions of the expected current values in these devices. Figure 2a shows a simulated band-edge profile along the length of an undoped Ge/Si axial NW heterostructure with a 300 nm channel length. The graded SiGe region from the Si source to the Si drain is shown here to vary linearly as a function of length for simplicity. In the actual NWs shown in Fig. 1, the Ge fraction drops exponentially over a distance comparable to the NW diameter and a logarithmic Ge fraction tail extends into Si. The gate extends over both the Ge source and Si drain in the simulated structure. The band-edge situation in (a) resembles that of a Ni metal contact on Ge and Si which is known to produce an electron barrier height of ~ 0.7 eV on both (10). With a positive gate bias (Figure 2b), a thin tunnel barrier is created at the Ge source and electrons can tunnel into the channel and are drifted toward the Si drain. Upon application of a negative gate bias (Figure 2c), a wider tunnel barrier is created at the Si side leading to less efficient hole tunneling into the channel and drifting toward the Ge source. The resultant transfer characteristics for this situation are shown in Figure 2f (solid blue line). The exact location of band-offsets or magnitude of barrier heights at the Ge source and Si drain determine the efficiency of tunneling of the carriers.

The band-offsets also determine the magnitude of the drift-field which can improve or degrade carrier velocity in the channel. Figure 2d illustrates the situation of a smaller electron barrier height at the Ge source and similar barrier height to that in Figure 2a at the Si drain. In this case, one can see that most of the band-offsets are accommodated in the conduction band-edge at the source side, which will in turn create an opposing electric field for current transport from the Ge source to the Si drain and reduce the on-current value (dash-dot black line in Figure 2f). In addition, the small electron barrier height at the Ge source results in mostly thermionic emission current with less steep subthreshold characteristics than that corresponding to Figure 2a (see solid blue line in Figure 2f). One concludes here that a large electron barrier height at the Ge source is necessary for: (i) high field assisted Zenner tunneling into the channel for sub-60 mV/decade subthreshold slopes, and (ii) maintaining a large drift field in the channel for high on-currents.

The hole barrier height on the Si drain side not only plays a role in determining the strength of the electric field in the channel for sweeping in electrons injected from the Ge source, but also in determining the magnitude of ambipolar hole transport in the device. A large hole barrier height at the Si drain will result in accommodation of the band-offsets mainly at the valence band-edge near the Si drain (Figure 2e). This will in turn result in a spatially thin hole tunnel-barrier at the Si drain side as well as residual electric field in the channel that accelerate hole transport toward the Ge source. Strong ambipolar behavior is expected to result in this case, as shown in Figure 2f (dashed red line).

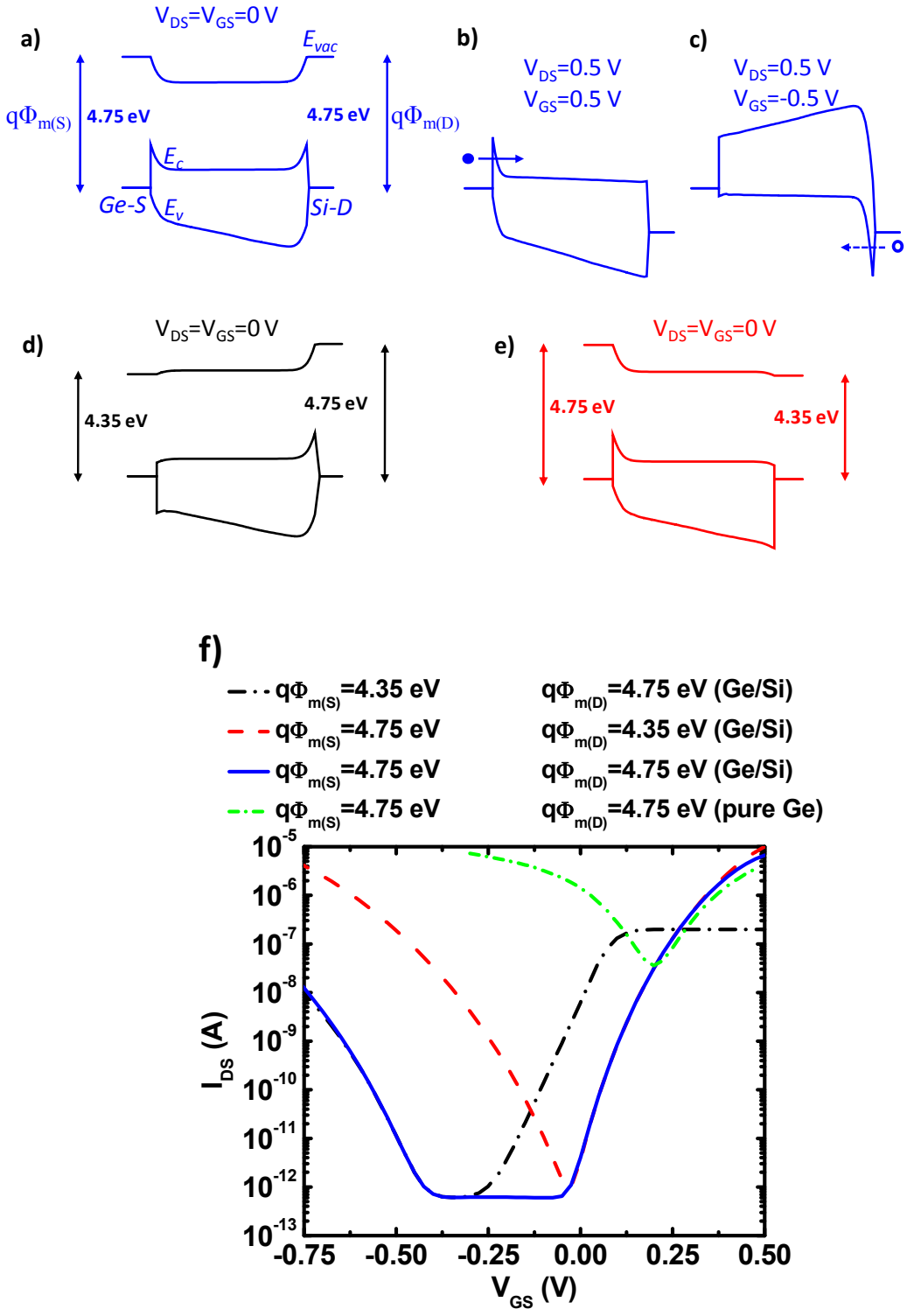

Figure 2: HTFET modeling results; a) Energy band-edge diagram along the axis of a Ge/Si axial NW heterostructure at thermal equilibrium. b) Same as in (a) for a V_{DS}=V_{GS}=0.5 V corresponding to a turned-on device. c) Same as in (a) for V_{DS}=0.5 V and V_{GS}=-0.5 V corresponding to a turned-off device. d) and e) Thermal equilibrium energy band-edge diagrams for different metal work functions. f) Simulated transfer curves for the band-alignments in (a, d, e) and in a pure Ge NW channel to aid in selecting appropriate barrier heights for reduced ambipolar behavior (see text).

The optimal structure for asymmetric Ge/Si Schottky barrier HTFETs is thus predicted to be attained by a large electron barrier height at the Ge source for steep subthreshold characteristics and high on-currents, and a near mid-gap hole barrier height at the Si drain for reduced ambipolar behavior. To compare these results with a homogenous Ge channel, we show in Figure 2f (short dash-dot green line) transfer curves obtained with $q\Phi_m$=4.75 eV at both the source and drain sides for a pure Ge NW. In the uniform Ge NW case strong ambipolar behavior and small I_{on}/I_{off} ratios is clearly seen in Figure 2f.

Device Fabrication and Transport Measurements

Ge/Si heterostructured NWs grown from 30 nm Au colloids (equal to the Si segment diameter) were suspended in isopropanol and transferred to a SiO_2/Si substrate carrier where NW coordinates were mapped with respect to a pre-defined grid. E-beam lithography was utilized to pattern source and drain electrodes as well as top gate contacts. E-beam evaporation of Ni was used for both the source and drain electrodes and Ti/Au for the top gate. Figure 3a shows a representative SEM image of the fabricated devices.

Figure 3b shows the room-temperature transfer curves of a Ge/Si HTFET for different V_{DS} values (forward bias case where positive voltage was applied to the Ge side) showing a maximum on-current of ~ 7 μA, ~ 170 mV/decade inverse subthreshold slope and 5 orders of magnitude I_{on}/I_{off} ratios for all V_{DS} biases considered here. It is worth to mention that reference devices in a separate processed batch with only their Ge segment gated showed no gate response (Ge was heavily p-doped in both cases). Reference devices with only their Si segments gated showed ambipolar behavior with maximum on-current ~ 10 nA, which is 10^2 – 10^3 times smaller than typical observed currents in the HTFETs (~ 1-10 μA). Changing the polarity of V_{DS} didn't change the trends observed in Figure 3b, however a slightly lower current (~ 10X) was obtained at negative gate voltages. This suggests more efficient hole tunneling at the Si side of the channel is responsible for the p-type behavior in the fabricated HFETs. Future work will utilize undoped Ge segments for better efficacy in modulating the electron barrier at the Ge side.

The high on-current value obtained from this device of Figure 3b is ~ 1750 X higher than that obtained with Si p-i-n^+ NW TFETs (11) and ~ 35 X higher than that obtained with CNT TFET (12). The I_{on}/I_{off} ratio and inverse subthreshold slope compare favorably to that of Si (~ 10^3 I_{on}/I_{off} and ~ 800 mV/decade SS^{-1}) but lags behind those of CNT TFET due to poor PECVD nitride gate dielectric quality (ε_r ~ 3-4). The asymmetry in the Schottky barrier heights used here eliminates the stringent requirements of abrupt doped interfaces as discussed above. These initial promising results are expected to be further improved by using a high-k gate dielectric.

Conclusions

We have discussed the design, growth, fabrication, and measurement of transport properties of Ge/Si axial NW HTFETs. We introduce the concept of built-in electric fields in the context of asymmetric Schottky barrier HTFETs. Our initial experimental results suggest that this novel approach to device architecture (Ge/Si heterostructure) is superior to what could be obtained from either Ge or Si NWs and exceeds what has previously been achieved in the area of homogenous p-i-n junction TFETs.

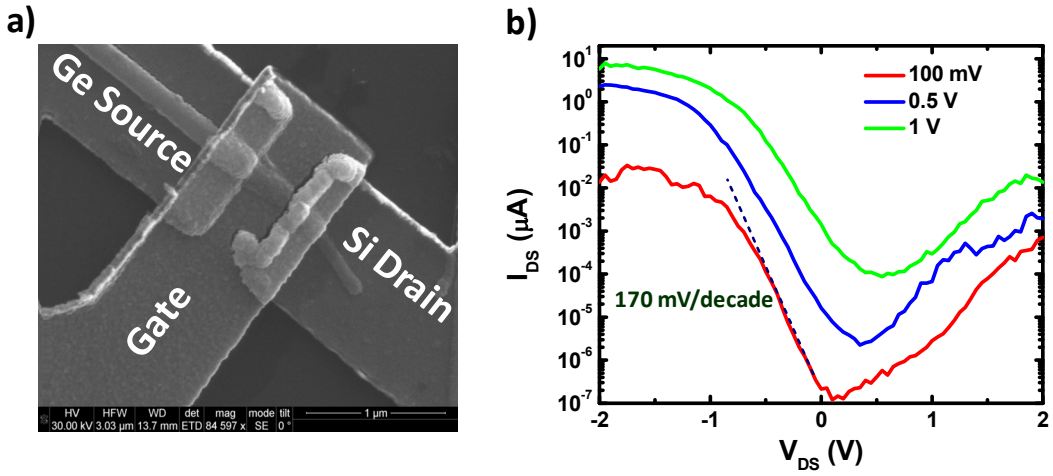

Figure 3: a) Representative SEM image of fabricated Ge/Si HTFET device. b) Transfer curves of a Ge/Si HTFET device with L_G=500 nm, D_{Si}=27 nm, 10 nm PECVD SiN_x (ε_r=3-4) for different V_{DS} values.

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