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Ge/Si Core/Multi-shell Heterostructure FETs

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Concentric heterostructured materials provide numerous design opportunities for engineering strain and interfaces, as well as tailoring energy band-edge combinations for optimal device performance. Key to the realization of such novel device concepts is the complete understanding and full control over their growth, crystal structure, and hetero-epitaxy. We report here on a new route for synthesizing Ge/Si core/multi-shell heterostructure nanowires that eliminate Au seed diffusion on the nanowire sidewalls by engineering the interface energy density difference. We show that such control over core/shell synthesis enable experimental realization of heterostructure FET devices beyond those available in the literature with enhanced transport characteristics. We provide a side-by-side comparison on the transport properties of Ge/Si core/multi-shell nanowires grown with and without Au diffusion and demonstrate heterostructure FETs with drive currents that are ~ 2X higher than record results for p-type FETs.

Introduction

Radial semiconductor nanowire (NW) devices not only provide superior electrostatic control over other possible channel geometries but also allow more flexibility in heterostructure core/shell materials designs for controlled interfaces and energy band-edge engineering in the confined radial direction (1). For example, in the SiGe materials system, it is possible to grow Ge/Si core/shell NWs which allows simultaneous passivation of the Ge surface and confinement of holes in the central small band-gap Ge region. While 1D Ge NW growth is mediated by a liquid AuGe alloy at a relative low temperature (~ 280 °C), 2D Si shell growth requires much higher temperatures (~ 500 °C) in order to achieve efficient SiH_4 precursor decomposition and Si crystallization on the NW sidewalls. These high temperatures lead to instabilities in the AuGe alloy and Au diffusion on the Ge NW sidewalls that result in rough shell morphology (Figure 1a) with detrimental effects on charge transport in these heterostructures. Previous work have used *ex-situ* techniques to etch Au and then grow epitaxial Si shells (2) or to grow long Ge NWs followed by amorphous shell growth and employ post-growth annealing for Si shell re-crystallization (3). Such growth procedures introduce contaminants and complexity into the growth of Ge/Si heterostructures. An improved understanding of the Au diffusion mechanism and control over such diffusion by interface engineering is necessary for growth Ge/Si core/shell NWs in a single growth run.

To gain insights into the Au diffusion mechanism and involved energy considerations, we have carried out systematic growth and temperature cycling studies to verify the origin of Au diffusion on small diameter NWs. Utilizing the catalytic effect of the liquid Au growth seed, we deposited at 280 ° C a thin

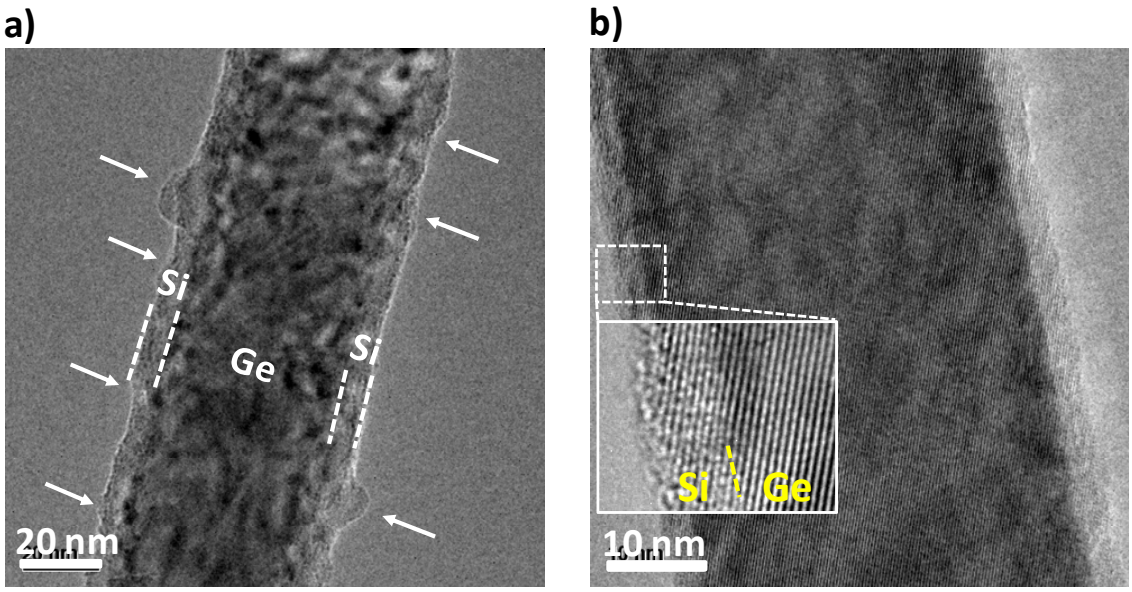

Figure 1: TEM images of Ge/Si core/shell NWs with (a) and without (b) Au diffusion. Au diffusion catalyzed the growth of thicker Si shells and rough surface morphology marked by white arrows in (a). Single crystal Ge/Si core/shell NW with smooth morphology is shown in (b). Inset is a zoom-in high resolution TEM image at the edge of the NW in (b) showing lattice fringes extending from the Ge core to the Si shell with a well-defined interface.

Si interfacial barrier layer underneath the Au to increase the surface energy on the NW sidewalls and prevented Au diffusion to the Ge surface. Subsequent temperature elevation to those suitable for Ge and Si shell growths have resulted in epitaxial Ge/Si core/multi-shell NWs without any observed Au on the NW sidewalls as verified by high resolution electron microscopy and X-ray analysis (4). Figure 1b shows an example of a single crystal Ge/Si core/shell NW. Such control over core/shell growth allows realization of core/multi-shell NWs for high on-currents and transconductances in heterostructure FET (HFET) devices, not accessible before in planar or NW growth techniques. We discuss in this paper the design considerations for such HFETs by numerical simulations and demonstrate experimentally Ge/Si core/multi-shell devices with high on-current drives.

Design Ge/Si core/multi-shell NW HFETs

Early demonstrations of undoped Ge/Si core/shell NWFETs have shown promising transport behavior (5,6) but did not utilize the design flexibility and advantages available from core/shell growth in the radial direction. Specifically, strain and quantum confinement may enable improvements in hole mobility and on-current drives in these HFETs, but these could benefit as well from appropriate radial doping profiles that increase the gate capacitance and charge carrier density in the channel. Such radial doping profiles would lead to significant improvements in performance such as higher transconductances and on-current drives.

To investigate the effects of radial doping profiles on the performance of Ge/Si core/multi-shell HFETs, we employed 3D Silvaco Atlas semi-classical simulations within

the framework of the drift-diffusion mode-space method. In this formalism, quantum confinement effects are captured by solving Schrodinger's equation in the

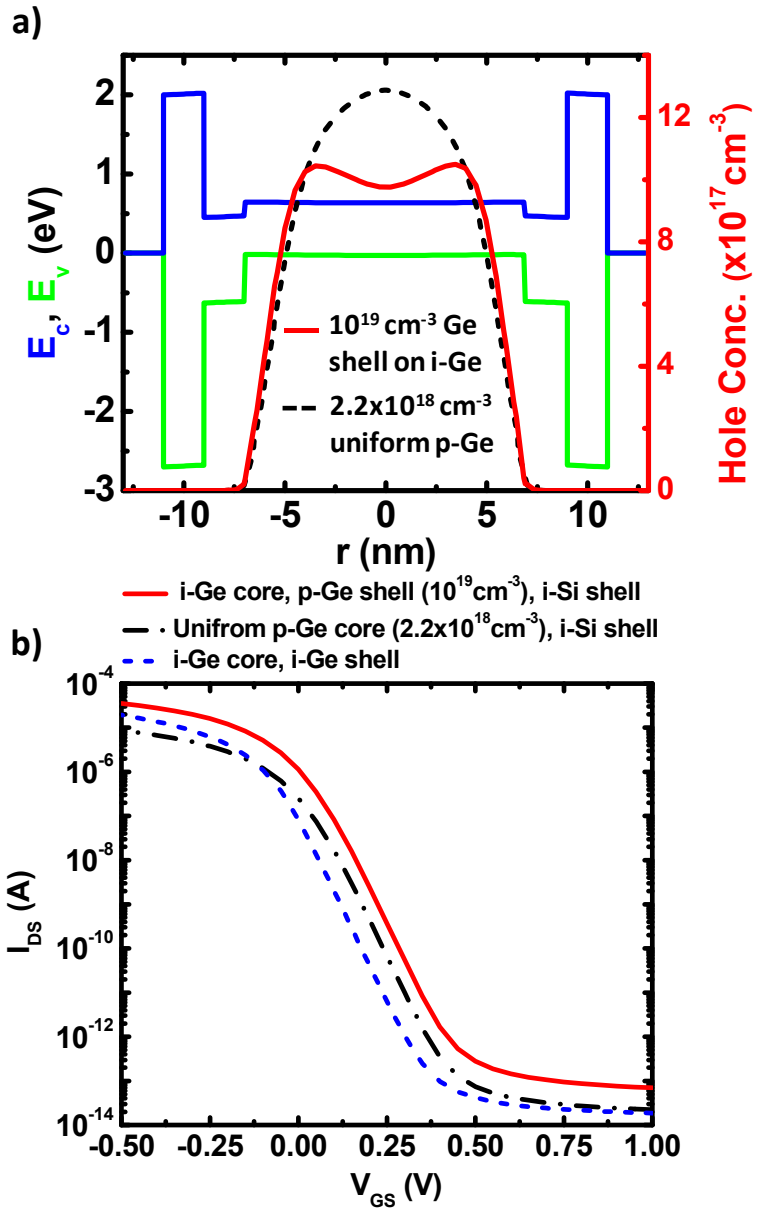

Figure 2: a) Band-edge structure and hole concentration in an i-Ge/p^+-Ge/i-Si core/multi-shell heterostructure NW showing peak hole concentration at the edges of the Ge core. The dashed black line shows hole concentration in a p-Ge/i-Si core/shell NW which peaks at the center of the NW. b) Simulated transfer curves for different Ge/Si core/shell doping configurations as indicated in the legend above at V_{DS}=0.5 V. L_{SD}, the source-drain separation is 50 nm and L_G is 30 nm for all devices considered above. Ge core diameter is 14 nm and the Si shell thickness is 2 nm with a 2 nm Si_3N_4 gate dielectric layer.

transverse (radial) direction and 1D transport equations are solved for each energy subband. Carrier densities and currents are computed afterwards by integrating over all energy subbands and weighting with the square of the corresponding wave function (7).

Three doping situations are considered: (i) 6 nm i-Ge core/ 1 nm p^+-Ge shell ($10^{19}cm^{-3}$)/ 2 nm i-Si shell; (ii) 7 nm p-Ge core ($2.2x10^{18}$ cm^{-3})/ 2 nm i-Si shell; (iii) i-Ge core/ i-Si shell. For the doped core/shell NWs, the dopant densities were chosen such that the total areal charge density remains the same for direct comparison as the radial doping profile is changed in these two cases. A 2 nm Si_3N_4 gate dielectric was used throughout.

Figure 2a shows the energy band-edge diagram across the diameter of a Ge/Si core/shell NW and the radial hole density profile for the two doping situations discussed above. It can be seen from Figure 2a that the i-Ge/p^+-Ge/i-Si case results in peak hole densities near the Ge/Si interface and thus high carrier densities closer to the gate electrode, when compared with the p-Ge/i-Si core/shell NW. This in turn leads to a larger gate capacitance and enhanced transconductances and on-currents for the i-Ge/p^+-Ge/i-Si case. Figure 2b shows the simulated transfer curves of the three situations discussed above. As anticipated the i-Ge/p^+-Ge/i-Si core/multi-shell NW is predicted to result in higher transconductance and on-currents compared to the p-Ge/i-Si case. The i-Ge/i-Si core shell NWs with no doping is seen to result in the lowest transconductance. Such device architectures for core/multi-shell NW with designed doping profiles can be grown with our core/shell growth described above and the resulting performance is indeed superior to other core/shell Ge/Si NW HFETs as we show below.

Experimental Realization of Ge/Si core/multi-shell NW HFETs

The i-Ge/p^+-Ge/i-Si core/multi-shell Ge/Si NWs were grown with our technique described earlier according to the radial dopant density profile discussed above. NWs with and without Au diffusion were fabricated and tested. Post-growth, the NWs were transferred to SiO_2/Si surfaces and HFET devices were fabricated using e-beam lithography in a similar technique used earlier for NW FETs (8). Ni contacts were used as source/drain electrodes and Ti/Au was used for the top-gate metal, as shown in Figure 3a.

The output curves of two Ge/Si NW HFET devices with gate length, L_G=1 μm, is shown in Figure 3a. Solid lines are measured on devices with no Au diffusion and dashed lines are measured on devices with Au diffusion that results in a rough surface morphology and shown for the same sequence of gate voltage steps. Transfer curves for the same devices are shown in Figure 3b. The on-currents and transconductances measured on NW HFETs with no Au diffusion are significantly higher than those measured on NW HFETs with Au present on the NW sidewalls.

The i-Ge/p^+-Ge/i-Si has a radial thickness of ~ 19nm/3nm/2.5nm for the NW with no Au diffusion and ~ 16.5nm/3nm/6nm for the NW with Au diffusion. In each case the gate dielectric was 8 nm thick Si_3N_4 PECVD layer with dielectric constant ~ 3-4. The ratio of the gate capacitance (oxide capacitance) of the NW HFET with no Au diffusion to that with Au diffusion is ~ 1.18. Since $L_G^2 \partial g_m / \partial V_{DS} = \mu_h C$, where g_m is the "intrinsic" transconductance, μ_h is the hole mobility, and C is the gate capacitance in Farads (and since the ratio of the measured slope of g_m with respect to V_{DS} for the NW HFETs with no Au diffusion to that with Au diffusion is ~ 2 for the same gate length), we conclude that μ_h for NW HFETs with no Au diffusion is ~ 1.7X that for NW HFETs with Au diffusion for this particular device. Results for more than 10 measured devices gave ~ 2X on average. Since the two types of NWs have relatively similar dopant profiles, performance enhancement in on-currents and transconductances is due to higher μ_h values for these NWs that utilize our new growth approach that eliminates Au diffusion.

For another device that utilized an L_G= 400 nm with a total Ge diameter of 61 nm, the maximum measured current was 205 μA at V_{SD}= 1V. The normalized on-current to

the physical dimensions of the device and the applied V_{DS} bias can be expressed as $I_{max}=I_{SD}L_G/\pi DV_{SD}$, where D is the NW diameter. This results in a normalized I_{max}=430 μA/V compared to an earlier best result of 211 μA/V (9). The higher on-currents obtained in our devices is enabled by the optimized radial dopant profile compared to uniform i-Ge/i-Si core shell wires in (9) as further validated by our simulations presented in Figure 2.

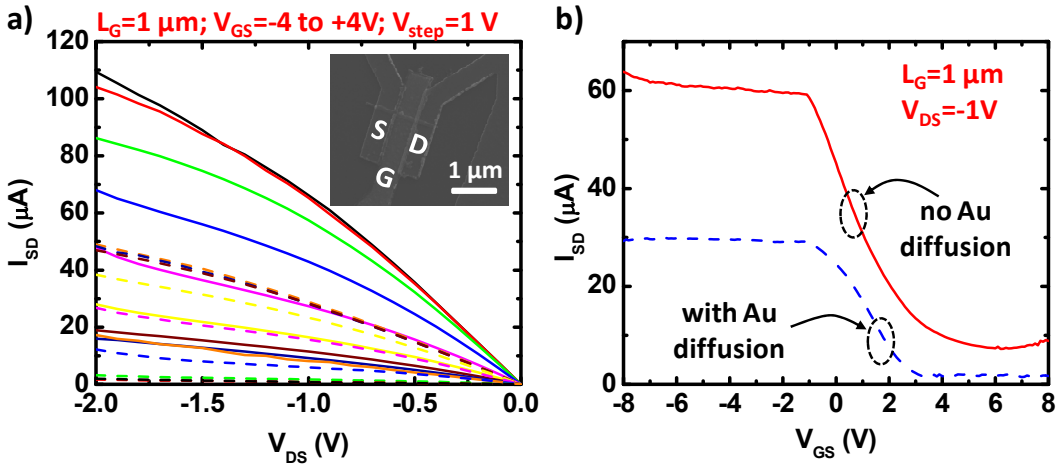

Figure 3: a) Output curves of Ge/Si core/multi-shell NW HFETs with (dashed) and without (solid) Au diffusion for the same channel length of 1 μm. Inset is a top-view SEM image of a representative device. b) Transfer curves corresponding to the same devices in (a) showing higher on-current and transconductance for the device with no Au diffusion.

Conclusions

We have devised a new growth procedure for optimal control over the core/multi-shell growth of Ge/Si heterostructure NWs that enable dopant and composition modulation and eliminates Au diffusion on the NW sidewalls. This growth procedure enabled the design of a new type of Ge/Si HFETs that resulted in higher on-currents than achieved previously and in improved hole mobility and transconductances over similar NWs with Au diffusion.

Acknowledgments

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