Silicon and Germanium Nanowires: Growth, Properties, and Integration

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Semiconducting nanowires are an area of widespread interest in nanomaterials research because of the ability to fabricate one-dimensional structures with tailored functionalities not available in bulk materials. Silicon and germanium nanowires have received particular attention because of the important role played by these materials systems in contemporary microelectronics and their potential for applications ranging from novel electronic devices to molecular level sensing and to solar energy harvesting. This paper provides an overview of the widely used vapor-liquid-solid technique for nanowire growth and its application to our recent silicon and germanium nanowire studies.

INTRODUCTION

Nanoscale materials are of great interest because of the possibilities they offer for obtaining new properties at small size. Basically, when structures approach the ~100 nm size regime their properties may change with decreasing size for the same atomic composition. This size dependence derives from three basic effects: surfaces become a large volume fraction of the structure, with those surface atoms having greater energy and different coordination; interfaces between nanostructures become a major component of the structures, with their modified electronic properties, strain gradients, and influence on the flow of defects, charge carriers, phonons, etc.; and sufficiently reduced dimensions lead to quantum size effects and coherent interactions between structures. These size-dependent effects result in changes in the physical properties of nanomaterials as well as changes in the interaction of electromagnetic energy with and transport of energy through nanomaterials. For example, electronic, optical, magnetic, and mechanical properties are altered, chemical reactivities change, new collective properties may emerge for arrays of nanostructures, and electromagnetic fields may be locally enhanced, for example in plasmonic effects.

One-dimensional (1-D) structures such as nanowires provide a particularly attractive class of nanomaterials. One can tailor the functionality of nanowires in a variety of ways and their geometry is optimal for achieving new regimes of 1-D transport of charge carriers and heat to realize new devices. Semiconducting nanowires are particularly versatile because of the wide range of properties that can be achieved. Thus much attention has been focused on these structures and their potential applications in such areas as electronic[1,2] and photonic devices,[3,4] chemical and biomolecular sensing,[5,6] and energy harvesting[7–10] and storage.[11] Silicon nanowires have especially seen an enormous number of studies over the last decade.[12] This attention derives in part because of the simplicity of the growth of these and other nanowires by metal catalyzed chemical vapor deposition techniques and in part due to the importance of Si as an electronic device material. Compound semiconductor nanowires, especially GaAs, InGaAs, InAs, and ZnO, have also been widely studied,[4,12–14] particularly for their optoelectronic properties such as for light

How would you…

…describe the overall significance of this paper?

This paper describes the underlying mechanisms controlling the growth of silicon and germanium nanowires and the influence of these mechanisms on heterostructure growth and dopant atom incorporation. We illustrate how the small size of nanowires affects their electrical and chemical properties. Challenges in the integration of nanowires into microscale systems are highlighted because future progress in this area will be essential for their application.

…describe this work to a materials science and engineering professional with no experience in your technical specialty?

Nanowires are commonly synthesized in a liquid-mediated vapor-to-solid growth process. This growth method introduces many basic and fascinating materials science issues which can be appreciated by any materials scientist and which underpin a comprehensive understanding of the current status of nanowire materials research. In addition, integration of nanowire structures into 3-D functional systems provides insight into a key direction in current nanomaterials research.

…describe this work to a layperson?

Semiconductors are one of the most important materials in our technology-based world and all semiconductor devices must be connected by wires to transmit their information to and from them. Semiconducting nanowires represent the limit of today's capability to scale three-dimensional devices to ultra-small sizes with the wires "built-in" and are revealing electrical and other materials properties not found at larger scales. Discovering methods to manipulate and connect these materials into systems will determine their eventual usefulness for practical applications.

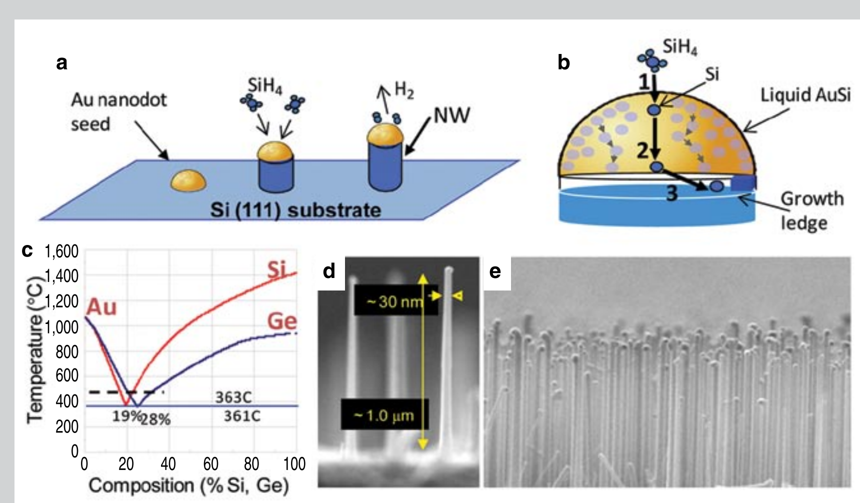

Figure 1. Vapor-liquid-solid (VLS) growth mechanism for nanowire (NW) synthesis. (a) Schematic of VLS Si NW growth from a liquid Au catalyst seed which floats on top of the NW as it grows and defines the growth diameter. (b) Enlarged view illustrating the three kinetic steps for NW growth: 1) silane decomposition at the vapor-liquid interface, 2) Si atom diffusion through the AuSi liquid, and 3) NW crystallization by Si incorporation into a step at the growing liquid-solid interface of the nanowire. (c) Binary phase diagrams for Au-Si and Au-Ge overlaid to illustrate their similar eutectic melt properties; dashed line indicates a typical growth temperature. (d) and (e) SEM images of $Si_{0.1}Ge_{0.9}$ alloy nanowires grown epitaxially from a Si(111) surface.[23]

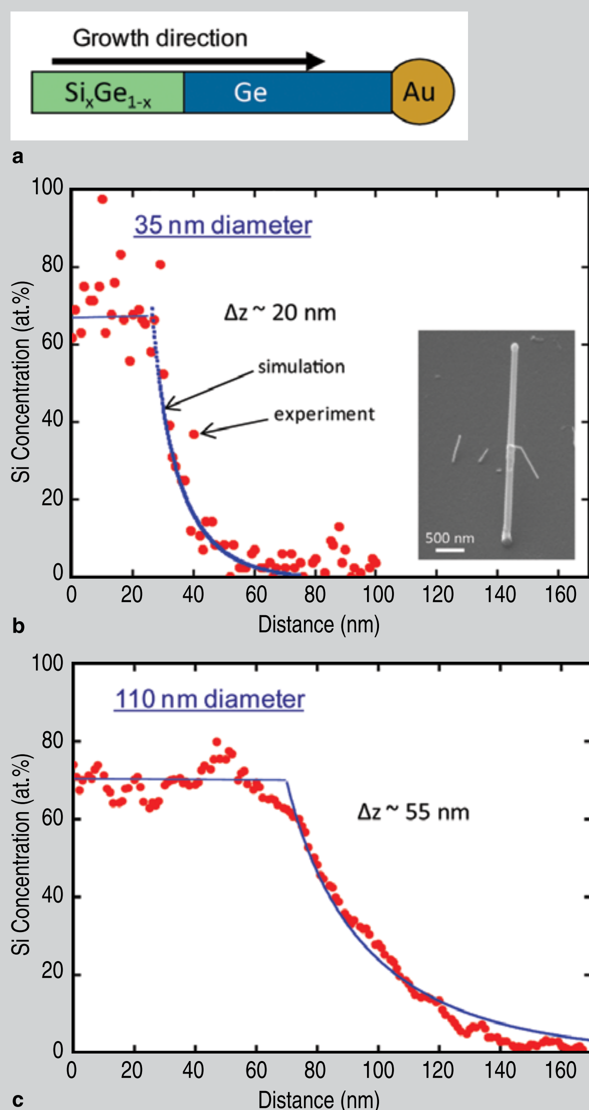

Figure 2. Composition profiles for $Si_{0.7}Ge_{0.3}$/Ge axial nanowire heterostructures. (a) Schematic illustration of the NW heterostructure. (b) Si concentration as measured by TEM energy dispersive x-ray analysis along the length of a 35 nm diameter NW. Inset shows SEM image of the NW illustrating a slight bulge at the transition from $Si_{0.7}Ge_{0.3}$ growth at 450°C to Ge growth at 260°C and a small side NW which grew in this case due to slight instability during the silane and germane to pure germane gas switching. (c) Si concentration profile as in (b) for a larger 110 nm diameter NW heterostructure. The solid lines in (b) and (c) are simulations with no adjustable parameters and show the 80 to 20% transition region to increase from ~20 to 55 nm as the NW diameter is increased from 35 to 110 nm.[31]

emitting diodes, nanoscale lasing, and photodetector structures, and for their piezoelectric properties. Another class of widely investigated 1-D structures is carbon nanotubes.[15] These nanostructures can be either semiconducting or metallic in nature, depending on the orientation at which their graphene sheets are wrapped into a tube. Carbon nanotubes have extremely high electrical conductivity, thermal transport, and strength, and have been considered for applications ranging from arrays for efficient field emitters to thermal materials, to fillers for structural composites, conductive plastics and adhesives, and electrodes for batteries and capacitors.[16] Semiconducting carbon nanotubes are interesting as electronic devices due to their unusually efficient transport characteristics and quantum effects.

For all these 1-D semiconducting nanomaterials the ability to integrate the structures into larger systems with the necessary manufacturing control and reproducibly, as well as an understanding of the new properties resulting from their surfaces and interfaces, will be critical to their eventual application. Due to the large breadth of the fascinating field of semiconducting nanowires we will restrict our focus here to Si and Ge nanowires. We give an overview of the growth and properties of these materials based on our recent studies and discuss some of the critical issues which must be controlled for their integration into larger scale structures and eventual applications.

NANOWIRE GROWTH

VLS Growth Technique

One of the most effective ways to fabricate semiconducting nanowires is by the vapor-liquid-solid (VLS) technique.[17] Gas precursor molecules or vapor containing the growth species are introduced into a furnace or chemical vapor deposition (CVD) reactor and liquid metal catalysts on a surface react with the source atoms to grow nanowires. In this approach a metal nanodot catalyzes the growth of the nanowire from a vapor source by forming a liquid metal droplet through which the growth atoms are transported to the crystallizing interface. This catalytic seed floats on top of the nanowire as it grows and

defines the nanowire diameter while the growth rate kinetics together with the growth time defines the nanowire length. Thus the nanowire 'self-assembles' in what is often referred to as a bottom-up synthesis technique. Typically, nanowires have diameters ranging from minimum values of ~5 nm up to several hundred nanometers, and lengths from ~100 nm to tens of micrometers.

Figure 1 illustrates the VLS method for Si and Ge nanowire growth. The schematic in Figure 1a shows silane molecules reacting at the Au surface through a hydrogen decomposition reaction sequence that introduces atomic Si into the Au nanodot (Figure 1b). The temperature is held near the eutectic temperature of 363°C and as the composition approaches the eutectic composition of 19 at.% Si (Figure 1c) melting occurs. Upon further addition of Si, the Si concentration in the liquid Au moves to the right of the liquidus line and the supersaturation becomes sufficient for crystallization of Si at the liquid-solid interface. The liquid drop size defines the liquid-solid interface and thus the area available for Si crystal growth. This maintains the nanowire growth at a fixed diameter as long as Au is not lost from the nanodrop. Since Si and Ge exhibit similar eutectic behavior with Au (see Figure 1c), Si, Ge, and SiGe alloy nanowires can all be readily grown by this same approach. Figure 1d illustrates a $Si_{0.1}Ge_{0.9}$ alloy nanowire. In general, Ge nanowire growth is carried out at ~275 to 375°C[18] and Si at 450 to 550°C,[19] since Ge precursors are more easily decomposed than Si precursors in the VLS process due to the greater reactivity of germane compared to silane. An important advantage of low growth temperatures is that conventional vapor-solid (VS) CVD growth on the nanowire sidewalls and Si substrate is minimized during nanowire VLS growth. Simultaneous sidewall growth reduces the maximum aspect ratios that can be achieved and results in a linear tapering of the nanowires. Tapering can also occur as a result of the loss of Au atoms from the nanowire tip if there is significant Au surface diffusion along the Si sidewall during growth, however this usually occurs only at ultra-high vacuums and low pressures and is not a consideration for usual CVD reactor growth conditions.[20]

There are three steps involved in the growth kinetics which combine to establish the nanowire growth rate (see Figure 1b). Step 1 is the decomposition reaction at the vapor-liquid interface which introduces Si into the liquid metal, step 2 corresponds to Si diffusion through the liquid to the solid-liq-

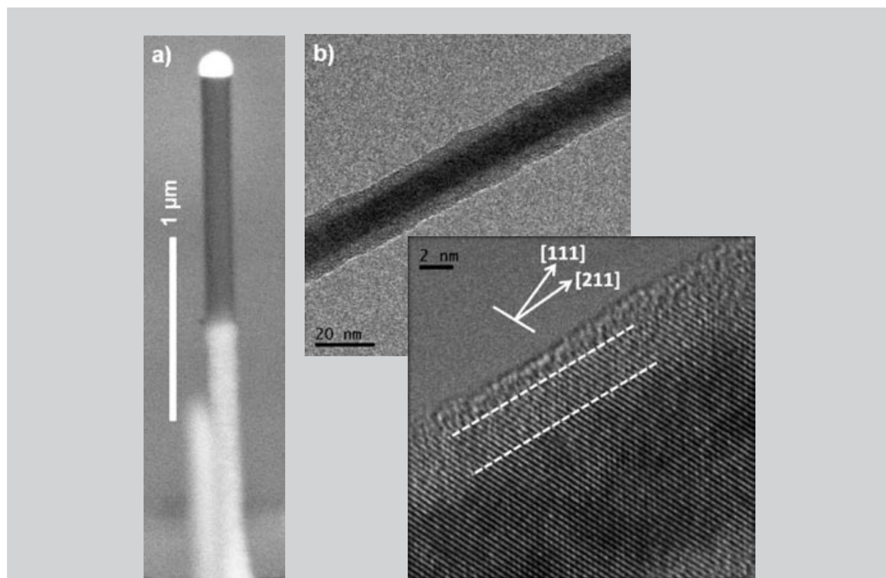

Figure 3. Electron microscopy images of axial and radial Ge/Si heterostructures synthesized with 100% composition change. (a) SEM image of a Ge/Si axial NW heterostructure epitaxially grown by the VLS method. Lighter region is Ge and darker region is Si. The bright hemispherical cap at the top of the Si segment is the Au growth seed. A second Ge segment of NW is visible behind the main image. (b) TEM images of Ge/Si radial NW epitaxial heterostructure formed by VS growth on the Ge NW sidewalls shown in low (upper image) and high (lower image) resolution. Outer radial region as defined by white dashed lines is Si and core region is Ge; (111) lattice planes are seen to extend continuously across the interface.[31]

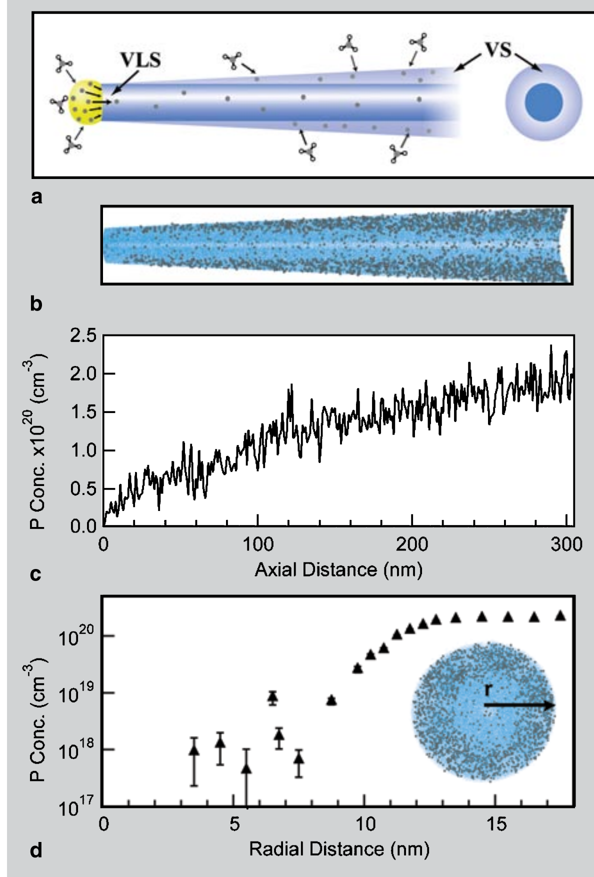

Figure 4. Growth and composition analysis of phosphorous-doped Ge nanowires. (a) Schematic showing VLS growth and P dopant incorporation through the liquid Au alloy along with some vapor-solid (VS) sidewall growth and P shell doping. VS growth gives rise to tapering of the NW along its length. (b) Black dots represent P atoms measured in a cross sectional slice of the Ge NW by the field atom tomography technique. (c) Total P concentration along the axial direction as a function of distance from the Au seed at the NW tip. (d) Average P concentration part way down the NW length as a function of radial distance from the center of the NW.[32]

uid interface, and step 3 is the Si crystallization at the liquid-solid interface which adds atoms to the nanowire surface. Typically the growth rates range from below 1 to 10's of nm/s so that the nanowire growth process is rapid. Since diffusion in liquids is fast for the few nanometer distances involved here, the transport in step 2 is rapid and not a limiting factor in the kinetics. The growth rate is then determined in steady state when the rates for step 1 and step 3 are equal and thus in equilibrium, both of which scale with surface area. Since the flux of the gas precursor molecules to the liquid Au surface is directly proportional to pressure, increasing the precursor partial pressure increases the available Si in step 1 and the resulting growth rate increases.[21] An increased pressure is equivalent to increasing the chemical potential difference between Si in the vapor and solid phases, which increases the Si concentration in the liquid Au and in turn the Si supersaturation which leads to an increase in the crystallization rate (step 3) at the liquid-solid interface. At larger Au seed sizes (~50 nm and larger) the growth rate is typically constant with nanowire diameter. However, decreasing the Au seed size at sufficiently small diameters increases the chemical potential in the liquid nanodot according to the Gibbs-Thomson effect, reducing both the forward chemical reaction rate introducing Si in step 1 and the crystallization rate in step 3, and thus decreases the growth rate. At sufficiently small Au nanodot diameters the chemical potential rises sufficiently to drop the supersaturation to zero and growth ceases.[22] This leads to a minimum diameter for which nanowires can be grown, which for typical growth conditions is ~5 nm.

Scanning electron microscopy (SEMs) images in Figure 1d and e shows $Si_{0.1}Ge_{0.9}$ alloy nanowires ~30 nm in diameter by 1 μm long for individual and dense arrays of nanowires, respectively, grown in a 50% silane and 30% germane in hydrogen gas mixture at a total gas pressure of 3 Torr.[23] An important feature of the VLS growth process is that it results in epitaxial growth of single crystal nanowires of high perfection oriented primarily along in the <111> crystal direction for Si and Ge with diameters greater than ~25 nm and along <211> and <110> directions at smaller diameters. The change in growth direction at small diameters is the result of overall energy minimization between the liquid-solid interface energy and the nanowire sidewall energy. The 30 nm diameter <111> oriented wires in Figure 1d and e are vertical because they grew epitaxially from a Si (111) oriented substrate. The VLS growth process does not always lead to straight nanowires. For example, instabilities due to changes in temperature, pressure, or gases present during growth can lead to instabilities in the liquid growth seed on top of the growing nanowire and result in kinking or twining along the growth direction.[24] For kinked Si and Ge, the growth often switches between the four available <111> directions which corresponds to a 55° tilt in the wire direction, or to another of the favored growth directions such as the <211> direction at a 19° tilt.

In addition to bottom-up VLS growth, top-down methods have also been used to form Si nanowires. They are often based on planar lithography definition of the wire width and length from Si-on-insulator structures.[25] Another approach is to lithographically or chemically induced patterning accompanied by preferential etching into an Si substrate to form arrays of vertical structures.[9] These top-down methods tend to be more challenging, either in control of the dimensions or due to rough nanowire sidewalls. In contrast, the VLS method has been much more widely used because it provides an easy route for synthesis and allows the growth of a wide variety of semiconducting materials, including Si, Ge, SiC, B, GaAs, GaP, InP, InAs, and ZnO, among others.[12]

Heterostructure Synthesis

The fabrication of heterostructures represents a key aspect in the operating principles and performance of many modern semiconductor devices. Thus control over the composition, doping, and crystalline perfection across functional interfaces and in heterostructures is essential for the fabrication of future high-performance nanowire devices.[26] Silicon/germanium compositional nanowire heterostructures are particularly interesting because of the large lattice mismatch of 4.1% for these diamond lattice structures, which gives rise to large local strains near interfaces and associated changes in the local bandstructure.[27] Compositional changes of up to 100% between Si and Ge axial and radial segments are predicted to be mechanically stable in nanowires at small diameters due to the lack of lateral confinement, whereas for conventional planar device geometries such structures cannot be realized due to the introduction of strain-relieving dislocations after only a few atomic layers of growth.[28]

Compositional heterostructure growth in the Si/Ge axial nanowire system has been challenging in the VLS growth method due to the instabilities created at the growing liquid-solid interface during switching of the growth precursor gases. This instability can lead to severe kinking of the nanowires and even loss of the liquid Au seed from the nanowire tip upon gas switching. As a result, previous axial Si/Ge heterostructures were typically limited to compositional changes of ~20% or less.[29,30] Recently, we have demonstrated Si/Ge nanowire growth with changes extending over the entire SiGe compositional range.[31] In Figure 2 compositional profiles for Si at the $Si_{0.3}Ge_{0.7}$/Si interface are shown for two different nanowire diameters. The abruptness of the interface transition region depends on the diameter, with the smaller diameter having a sharper transition. This chemical transition region for VLS synthesis arises from the liquid Au alloy composition during growth. Upon switching from growth species A to B, the liquid acts as a reservoir for the growth species A which must be depleted from the liquid by subsequent crystallization at the liquid-solid interface while B is added to the liquid for the transition to pure B growth to occur. The solid curve in Figure 2 is calculated based on our simulations, which only assume that the incorporation probabilities for Si and Ge are proportional to their concentrations in the liquid at the nanowire crystallization front (step 3 in Figure 1b). Other studies have shown similar behavior at smaller compositional changes with the width of the transition region proportional to the nanowire diameter.[30]

In Figure 3 both axial and radial 100% compositional heterostructures are shown for the Si/Ge system.[31] We have achieved these dislocation-free structures in both cases by in situ growth in our CVD system, using VLS growth for the axial case and subsequent VS growth for the radial case. For the case of radial VS growth, which will be discussed in more detail in the following section, the composition transition regions can be atomically sharp, provided high growth temperatures which can induce solid phase diffusion across the interface are not used.

Electrical Dopant Incorporation

To exploit the potential of semiconducting nanowires for electronic-based applications one needs to introduce electrical dopants during or after their growth. Electrical dopant incorporation is usually carried out for Si and Ge nanowires during their growth, since post-growth control of dopant location by ion implantation or other techniques in these small three-dimensional (3-D) structures is difficult to achieve. Doping during growth can be accomplished by introducing dopant precursors commonly used in CVD growth, such as diborane and phosphine for p- and n-type doping, respectively. High dopant concentrations can be achieved by this approach with similar VLS growth rates maintained during boron (B) doping and somewhat reduced growth rates for phosphorous (P) doping in Si and Ge, particularly at the highest doping levels ($>10^{19}/cm^3$).

A primary consideration in dopant atom incorporation during VLS growth is the control of the dopant spatial distribution, both radially and axially. An important recent advance in this area has been the application of atom probe tomography to obtain 3-D composition profiles of nanowires with the sensitivity needed to measure dopant atom distributions within nanowires at concentrations $\sim 5\times10^{17}/cm^3$ and higher.[32] Figure 4 illustrates this technique for P distributions both along the length of a Ge nanowire and radially from the nanowire center to the outer perimeter. From Figure 4 the issue of simultaneous dopant incorporation by VLS growth in the central region of the nanowire and by VS growth of a heavily doped shell region is clearly illustrated. Differences in dopant precursor decomposition and incorporation rates between the liquid catalyst for VLS growth and the solid nanowire surface for VS growth give rise to a heavily doped shell surrounding an under-doped core. These effects are significant for conventional dopants such as diborane and phosphine in Si and Ge nanowire growth. For example, under some CVD growth conditions VLS growth incorporates Ge into the growing nanowire 20 times more efficiently than VS growth incorporates Ge on the sidewall; in contrast, P is incorporated in the sidewall during VS growth seven times more efficiently than into the nanowire core by VLS growth. This VS sidewall doping effect complicates control of doping along the length of the nanowire, since the doping concentration will depend on the length of time of sidewall exposure to VS growth, and hence the distance from the nanowire tip. Vapor-solid dopant incorporation further complicates the growth of nanowire heterostructures such as an axial p-n junction. For example, during growth of the n-doped segment, the previous p-doped region will have a surrounding n-doped compensating shell via unwanted VS shell growth.[33] While lower growth temperatures or post-growth etching can reduce the extent of unwanted VS shell doping, further developments in VLS growth techniques are needed to eliminate this effect if full control over axial nanowire doping is to be achieved. However, one advantage of the incorporation of dopants by VS sidewall growth on nanowires is that radial doping of nanowires is possible. Thus radial p-n junctions can be obtained by emphasizing the VS sidewall growth process (for example, by higher temperatures and lower pressures). Relatively few studies of radial devices, such as for p-i-n solar cells,[34] have been demonstrated at this time.

PROPERTIES

Electrical, optical, thermal, and chemical properties are among those of greatest interest for semiconducting nanowires. Electrical transport is modified by the close proximity of the nanowire surface due to charge trapping and scattering with relevance to both minority and majority carrier devices. Diffuse optical scattering of incident light by Si nanowires due to the dielectric constant difference from air gives rise to the dark appearance of a dense nanowire surface. This shortens the distance for light absorption by about an order of magnitude from ~250 µm crystalline Si solar cells to ~10 µm for an array of Si nanowires and is one of the factors which make them of potential interest for photovoltaic applications.[35] Thermal transport occurs mainly by phonons in nanowires and the strong phonon scattering at small diameters greatly reduces heat transport through nanowires. This reduction is expected to significantly enhance thermoelectric efficiencies and has sparked interest in nanowires for thermoelectric cooling and electrical current generation applications.[9,10] Chemical properties of nanowires are changed in a number of ways due to the large effective surface area for a nanowire-covered surface. For example, Si nanowires can much more readily accommodate the several 100% volume change by radial expansion upon cycling of Li in and out of Si and have the potential to increase the charge storage capacity of Li battery anodes by a factor of 10 if they can be shown to have sufficient lifetimes.[11] Here we briefly discuss two examples for Si nanowires to illustrate their altered electrical and chemical properties from bulk materials.

Electrical

Electrical n- or p-type doping can be achieved in Si and Ge nanowires and thus controlled electron or hole carrier flow is accessible for devices. Field effect transistor (FET) devices have received the most attention in electrical transport studies, with current interest focused on such areas as achieving enhanced performance in tunneling FETs.[36] Typically, nanowire doping in Si and Ge ranges from $10^{17}/cm^3$ to maximum dopant solubility levels ($\sim 10^{20}/cm^3$). Doping levels below $\sim 10^{17}/cm^3$ usually result in negligible free carrier concentrations due to electrical compensation of dopant charges by surface charged trap states. Under these conditions ambipolar FET behavior is observed, whereas at $\sim 10^{18}/cm^3$ doping levels normal field modulation of current flow in nanowire FETs is achieved.

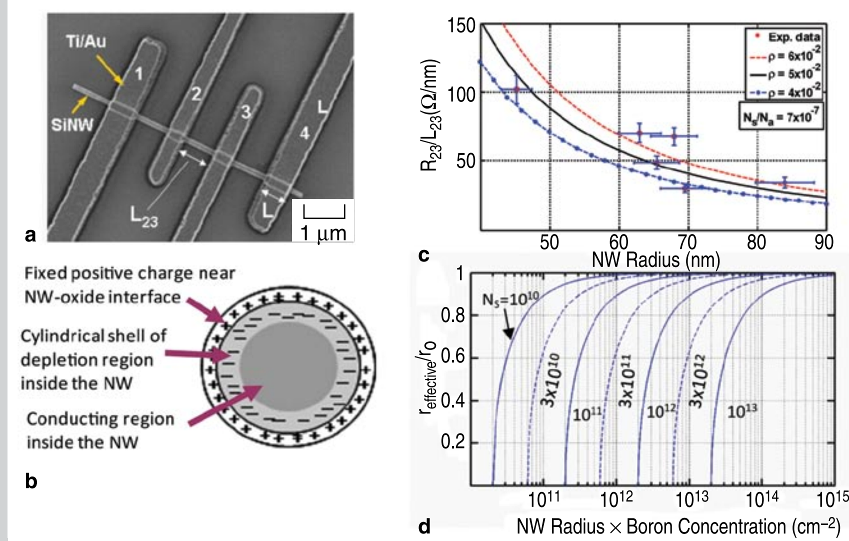

Figure 5. Electrical transport in B-doped Si nanowires. (a) SEM image of NW with 4 probe Au/Ti contacts. (b) Schematic of nanowire cross section illustrating the outer thin oxide layer, fixed positive charge near the oxide/NW interface, depleted shell in outer NW region, and inner NW conducting region. (c) Resistance per unit length in the NW as a function of NW radius. Lines represent the predicted curves for NW resistivities of 0.4, 0.5 and 0.6 mΩ-cm at a fixed surface charge density to electrically active B concentration ratio of 7×10^{-7} cm×d) Predicted reduction in effective radius for charge transport due to surface charge vs. the NW radius times B concentration as a function of surface charge density. The parametric curves allow estimation of the minimum doping concentration required to compensate the oxide surface charge for hole transport within an uncompensated region of radius r_{eff} as a function of surface charge density.[38]

Comparison of the relative effects of surface traps vs. nanowire doping on electrical transport can be appreciated by a specific example. Figure 5 illustrates 4 point measurements of p-type transport in Si nanowires which were uniformly doped by B diffusion and annealed to achieve relatively low surface trap state concentrations.[37] The positive trapped charge expected at the Si surface oxide and oxide/nanowire interface is illustrated schematically in Figure 5b along with the corresponding compensating depletion region within the B-doped nanowire. With decreasing nanowire radius (or decreasing B concentration) this depletion region becomes an increasing fraction of the nanowire cross section, thus reducing the uncompensated conducting region. This effect is observed (Figure 5c) experimentally by the increased resistance per unit length in a series of nanowires of decreasing radius doped to the same concentration.[38] The best fit to these results corresponds to a fixed surface charge density at the NW-oxide interface, N_s, of $6 \times 10^{11}/cm^2$ and electrically active B concentration, N_a, of $8 \times 10^{17}/cm^3$. The B concentration-nanowire radius product at which the surface charge becomes significant for transport can be easily estimated based on the parametric curves of Figure 5d, where typical values for surface states are in the 10^{11} to $10^{13}/cm^2$.

At higher carrier concentrations surface state effects do not directly give rise to significant depletion into the nanowire, but still have an important influence on electrical transport due to surface scattering and recombination. For example, nanoprobe electrical transport studies across the Au-catalyst/Ge-nanowire Schottky diode interfaces for n-type electrical carrier doping in the 10^{18} to $10^{19}/cm^3$ range have shown electron-hole recombination at the nanowire surface to be the dominant charge transport mechanism.[39] The resulting nanowire conductance behavior is strongly influenced and diameter dependent. The extent to which these diameter-dependent changes in electrical transport behavior will be important or be exploited in nanowire electronic applications is not yet known.

Chemical

The chemical properties of surfaces with a high density of nanowires present can be quite different from smooth surfaces, due to their high effective surface area. For example, an Si surface with 50 nm diameter vertical Si nanowires 10 µm long at an areal density of 25/µm² represents a fill factor of only 5% of the surface area and yet increases the effective surface area (total surface of Si per unit area of surface) by a factor of 40. Thus the influence of many surface properties can be greatly multiplied if extended to surfaces covered by nanowires.

The hydrophobicity of surfaces illus-

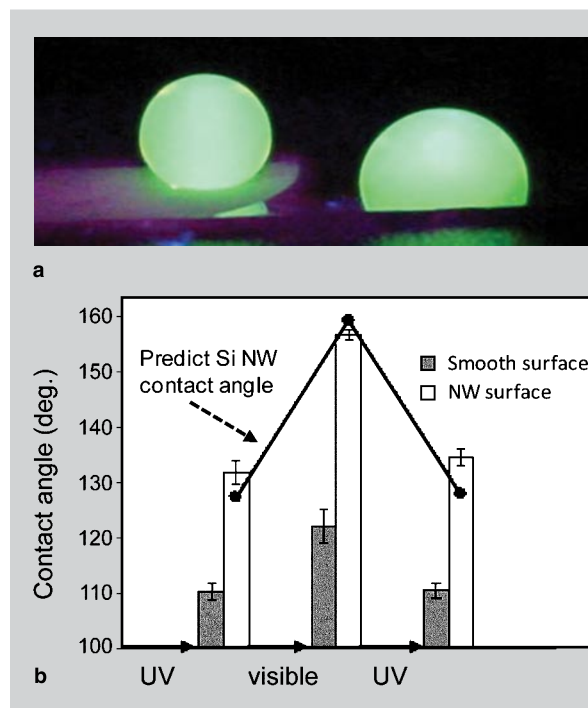

Figure 6. Chemistry and morphology of nanowire surfaces combine to control surface hydrophobicity. a) Photograph of water droplets containing green fluorescent dye on PFOS-treated Si NW (left side) and smooth Si surfaces (right side) illustrating the increase from hydrophobic to superhydrophobic behavior. b) Advancing contact angle for Si NW (white bars) and smooth Si (shaded bars) surfaces with photoresponsive spiropyran-linked monolayers after UV and visible light exposure. Circles are the predicted values for the NW surface based on a Wenzel model for fractally rough surfaces. The large change in switching angle allowed the water droplets to be moved solely by the light-induced change in surface energies.[40]

trates an area where such surface chemical effects are pronounced. Surface wetting properties of a hydrophobic or hydrophilic surface are well known to be amplified by rough surfaces with their increased surface areas. Since silicon dioxide surfaces are easily modified chemically by functionalizing with a wide variety of molecular species, Si nanowires on a Si substrate with their air oxidized surfaces provide a natural platform to examine such surface

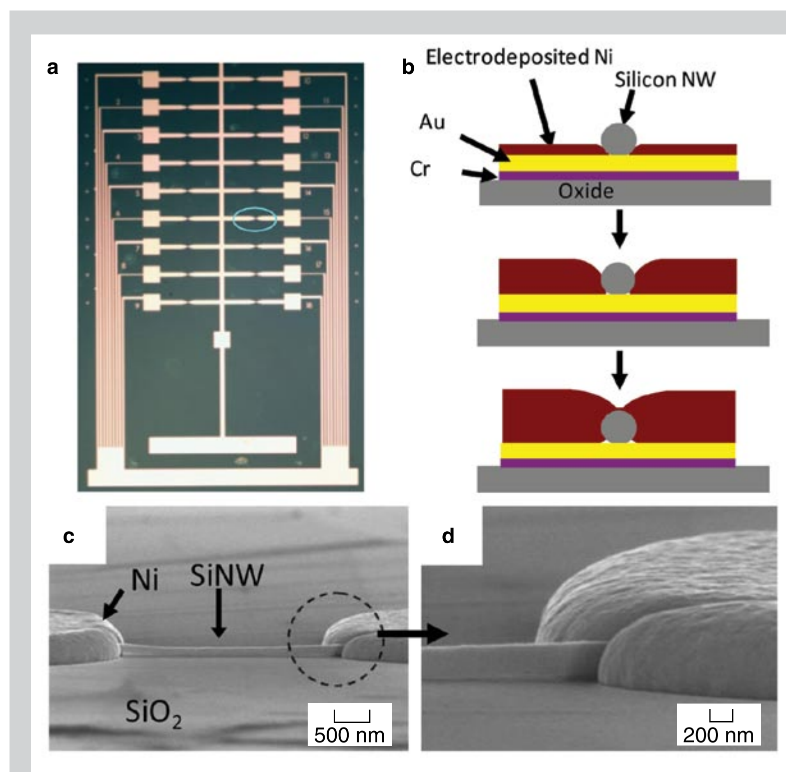

Figure 7. Directed assembly of Ni contacts to Si nanowires by selective electrodeposition. (a) Au electrode pattern for dielectrophoretic alignment of Si NWs as well as for definition of location where Ni electrodeposition will be deposited. Blue oval shows the location of one of the 18 Au electrode pairs. (b) Schematic illustration of the Ni electrodeposition step following NW dielectrophoretic alignment. (c) and (d) SEM images of the electrodeposited Ni contact which is only deposited on the conducting Au substrate regions showing the Ni surrounding the Si NW (scale bars are 500 and 200 nm, respectively).[43]

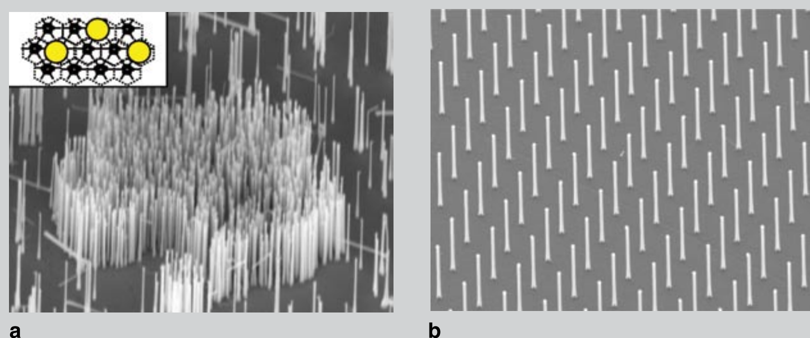

Figure 8. Vertical arrays of Ge <111> nanowires grown epitaxially by the VLS method on Ge (111) substrates. (a) NW growth seeds are formed by nanobiotemplating of 20 nm Au colloidal catalysts which attach to the vertices (see inset) of s-layer sheets from Deinococcus radiodurans (NWs in central region of image).[46] (b) NW growth seeds are formed by electron beam lithography patterning, 20 nm Au film deposition, and pattern lift-off.[47] SEM images are at a 45° angle and Ge NWs are ~1.5 nm long.

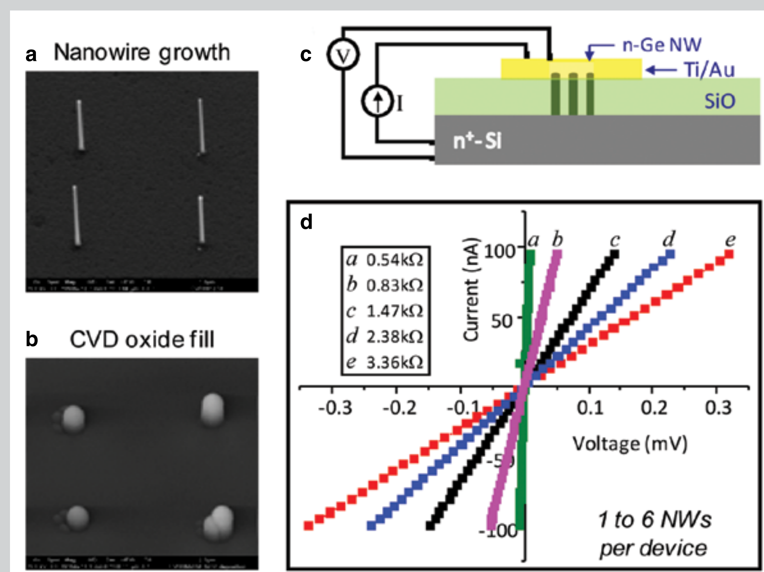

Figure 9. Vertical P-doped Ge nanowire resistors on a Si substrate: processing and electrical measurement. (a) SEM of ~1.5 μm long Ge <111> NWs grown from Au colloids chemically assembled into electron beam patterned holes. (b) SEM of same surface after CVD oxide deposition. (c) Schematic of three contacted vertical NWs on Si substrate prepared for electrical measurements. (d) Electrical I-V curves for devices with between 6 (data labeled a) and 1 (data labeled e) NWs per contact.[48]

chemical effects. Figure 6a contrasts the wetting of a droplet of water on Si nanowire (left side) and smooth Si (right side) surfaces after functionalization with perfluorooctyl-trichlorosilane (PFOS). The wetting angle which is only slightly greater than 90° on the smooth hydrophobic surface greatly increases on the superhydrophobic nanowire surface. Further, if the surfaces are functionalized with a monolayer of photochromic-containing molecules such as spiropyran, the surface bound molecules can be switched between nonpolar and polar forms under visible and ultraviolet (UV) irradiation.[40] Thus, light can be used to switch the hydrophobicity of the surface. In this way a nanowire surface morphology has been shown to significantly amplify the light-induced change in water contact angle.[40] As illustrated in Figure 6b the change in contact angle between visible and UV irradiation increased from 12° on a smooth Si surface to 23° on the spiropyran-coated nanowire surface, whereas the contact angle hysteresis for water droplet motion on the surfaces decreased from 37 to 17°. As a result, the advancing water contact angle under UV irradiation is lower than the receding water contact angle under visible irradiation, which allowed water droplets to be moved on the roughness-magnified photoresponsive nanowire surface solely by the light-induced lowering of the surface energy. While many types of nano- and microscale surface chemical modifications are used to alter surface energies for applications ranging from petroleum extraction to soil-resistant cloth, this example illustrates the significant effect of the greatly increased surface area for nanowires.

INTEGRATION

Integration has played a pivotal and revolutionary role in the development of nearly all science and technology, with very large scale integrated circuits being one of the most striking examples. Even greater challenges exist as nanomaterials are integrated into new architectures to form functional systems. Nanowire integration leads to the formation of interfaces and surfaces whose structure and properties can dominate the electronic, optical, chemical, and mechanical properties of the system. New directed- and self-assembly approaches must be developed for facile assembly and greater functional control. Combined bottom-up and top-down synthesis and assembly techniques are needed to allow controlled, large-scale formation of micro-scale systems. Establishing these processes for integration of nanowires will be of paramount importance for their application in nanotechnology.

Directed Assembly and Contacting of Nanowire Arrays

Methods to organize large numbers of nanowires into regular arrays for specific functions are needed for electronic and electromechanical applications. For lateral nanowire arrays, top-down patterning methods have been demonstrated to both synthesize and form ultra-high density array of metal and semiconductor nanowires.[41] Approaches based on bottom-up assembly of nanowires, for example to incorporate VLS grown nanowires into large arrays, have been more challenging. One successful method has been to pre-pattern surfaces with metal contacts and use dielectrophoretic alignment by ac electromagnetic fields for the directed assembly of the nanowires. This method allows the simultaneous alignment of large numbers of nanowires in a fluid suspension into well-defined arrays. This approach has been used to assemble large numbers of functionalized Si nanowires into cantilever resonator arrays.[42] In this combined top-down and bottom-up approach lithography is used to pre-pattern the chip, establishing the overall placement of electrical conduction lines and metal contacts. Then in bottom-up processing the nanowires are introduced, assembled, and their electro-mechanical connection with the pre-patterned metal contacts established by metal electrodeposition. Thus once the nanowires were introduced, no additional lithography steps were required.

We have explored Si nanowire dielectrophoretic assembly combined with electrodeposition for electrically contacting the nanowires for electrical transport sensor arrays. The focus of these earlier studies was on the contact directed assembly process.[43] Figure 7 illustrates this approach for the assembly of the electrical contacts to Si nanowires after dielectrophoretic alignment onto the pre-patterned Au leads. The Si nanowires are, in essence, buried by the electrodeposited Ni. Brief thermal anneals are then required to form good electrical contact to the nanowires. As for the cantilever arrays these methods, which mimic the biological solution-based approach to self assembly, offer the advantage of nanowire manipulation and assembly without further lithography. Further advances in combined bottom-up assembly with top-down patterning are needed, however, if efficient and reproducible manufacturing methods are to be obtained by this approach.

Vertical Arrays and Devices

An efficient way to exploit the small size of nanowires in high-density, large-scale integration is to form vertical arrays of devices. While individual vertical nanowire FETs have been demonstrated,[44,45] arrays of individually addressable vertical devices have not yet been achieved. A first step in this objective is to develop processes to reproducibly form arrays of highly vertical nanowires. We have recently made good progress in this direction for electrically doped Ge <111> oriented nanowires grown on Ge (111) substrates. Figure 8 illustrates such arrays for two very different templating methods for positioning the nanowires. In Figure 8a the nanowire patterning is carried out by a new nano-biotemplating approach where s-protein shells from Deinococcus radiodurans are used to attach Au colloidal growth catalysts to their vertices (see inset).[46] The Ge nanowires are subsequently grown by the VLS method from the Au colloids with significantly higher densities and greater percentages of vertical nanowires achieved at small nanowire diameters (~10 to 30 nm) than in non-templated regions. The mechanism by which the biotemplates enhance vertical growth is not fully understood, but is related to control of the initial Au wetting to the Ge surface. The primary limitation for this technique is establishing a predetermined registry for the nanowire array. The second approach

illustrated by a Ge nanowire array in Figure 8b is based on electron beam lithography patterning of the Au growth catalysts using Au film deposition and lift off. As seen this method provides good nucleation of highly regular Ge nanowire arrays by the VLS growth method.[47] Such methods should be extendable to parallel processing approaches for forming the growth catalysts, for example such as by nanoimprint lithography. A key aspect of this second approach for patterned array formation is again the combining of top-down and bottom-up methods.

Once vertical arrays are formed on conducting substrates, methods for the device processing of these 3-D structures must be developed to form addressable arrays of devices. One approach is to bury the vertical nanowires in a dielectric, planarize the surface by methods such as chemical-mechanical polishing (CMP), and then chemically expose the nanowire tips and lithographically pattern the top metal contacts. An example of this approach is shown in Figure 9 for Ge nanowires which have been grown in a patterned array, filled, planarized by CMP, and contacted by Ti/Au patterned deposition. Electrical I-V curves for these n-type nanowires show good linearity and scale as the number of nanowires grown under each contact.[48] For fully addressable arrays efficient architectures must be developed to individually contact both the top and bottom of the nanowires.

CONCLUSIONS

While the vapor-liquid-solid method, commonly used for the growth of semiconductor nanowires, was discovered over 50 years ago, it is only in the last 10 years that a wide range of nano-wire materials, properties, devices, and potential applications have been investigated. Silicon and germanium are among the most widely studied of these materials. For future applications increased control of the synthesis of nanowires, including their nucleation, heterostructure formation, and electrical doping is required. Equally important will be a more in-depth understanding of their properties together with the development of architectures and integration approaches to fully exploit their unique properties. Energy applications are one of the recent areas for semiconducting nanowires receiving much attention, due to their potential for new approaches to energy storage in batteries and energy harvesting in solar cells and thermoelectric devices. Progress in these and other application areas will benefit by significant advances in the integration of 3-dimensional arrays of nanowires into micro- and macroscale systems.

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