Analysis of local carrier modulation in InAs semiconductor nanowire transistors

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The authors have used scanning gate microscopy combined with numerical simulations to analyze local carrier and current modulation effects in InAs semiconductor nanowires grown by metal-organic chemical vapor deposition. Measurements of current flow in the nanowire as a function of probe tip position, at both high and low drain bias, reveal that carrier and current modulation is strongest when the probe tip is near the source and drain nanowire contacts, and decreases at greater tip-contact distances. The measured transconductance is approximately 80% greater near the source contact for high drain bias condition and 120% greater near the drain contact for low drain bias condition, respectively, than at the center of the nanowire. Numerical simulations for different tip positions relative to the metal contact confirm that carrier modulation should be stronger when the tip is closer to the source or drain contact than at the center of the wire, consistent with the experimental measurements.
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I. INTRODUCTION

With the end to traditional silicon transistor scaling in sight, there is intense current interest focused on identifying alternatives which will enable continued improvements in performance of future electronic systems.[1] Of the various material systems and structures being investigated, semiconductor nanowires are particularly intriguing due to the flexibility afforded in heterostructure formation and their scalability to very small sizes. In recent years semiconductor nanowires have been extensively explored as building blocks for nanoscale electronic devices,[2–4] optoelectronics,[5–7] sensors,[8] and high performance logic circuits.[9,10] Among these, the semiconductor nanowire field effect transistor[11,12] (SNWFET) has drawn particular interest, both as a vehicle for basic carrier modulation investigation or transport study and as a potential future high performance electronic device for large-scale integrated systems.[13]

In optimizing the performance of SNWFET device structures, understanding and optimizing the coupling between gate and channel play a major role in improving device performance. Back-gate,[7,14] top-gate,[11,12,15,16] and surrounding-gate[17,18] SNWFET geometries have been successfully demonstrated. Top-gate and surrounding-gate devices exhibit excellent electrical characteristics, including steep subthreshold slope and high transconductance, a significant improvement relative to back-gate devices, which typically suffer from use of a thicker gate dielectric. Top-gate devices are also suitable for high frequency applications, thanks to their smaller overlap capacitance between gate, source, and drain compared with that of back gate. Compared to a surrounding-gate geometry, a top-gate structure has the advantage of being more easily integrated in conventional fabrication process due to its planar structure.

To understand and optimize device performance in the top-gate geometry, we need to examine more closely and at the nanoscale how a top gate influences the carrier modulation and transconductance along the channel of the SNWFET. For this purpose, scanning gate microscopy[19,20] (SGM), which has been used successfully to characterize local nanoelectronic properties in other material systems, is a very attractive candidate. In this measurement, we use a conductive atomic force microscope (AFM) tip, which can be viewed as a very narrow top gate, to scan over the sample while biasing the two-terminal device at a constant source-drain voltage. Using SGM we observe that, at both positive and negative tip voltages, modulation of current flow in the nanowire varies as the tip distance from source/drain contacts changes: modulation is stronger when the tip is close to a contact and weaker when the distance is greater. Numerical simulations corroborate our observations and show that carrier modulation is strongly dependent on the probe tip (ultra small gate) position, where the maximum effect is attained when the tip is close to the source/drain contacts. These results provide insight into the design of highly scaled devices with a top-gate geometry to attain improved device characteristics such as higher transconductance and better i_{on}/i_{off} ratio.

II. EXPERIMENT

The InAs nanowires used in these studies were grown by metal-organic chemical vapor deposition using colloidal Au nanoparticles ~40 nm in diameter for nucleation of nanowire growth on thermally oxidized Si (001) substrates. Growths were conducted at a chamber pressure of ~100 Torr and a substrate temperature of 350 °C. The nanowires were unintentionally doped *n* type, and for each

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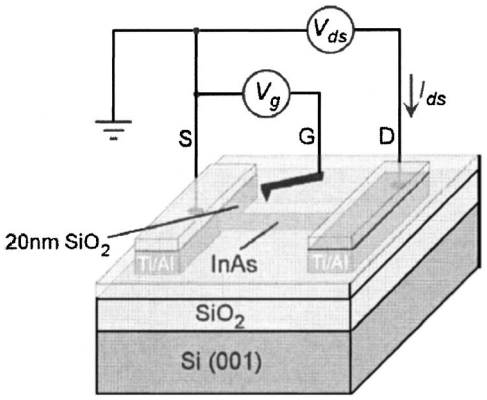

FIG. 1. Schematic diagram of experimental probe tip and sample geometry and electrical measurement configuration. A dc voltage V_g is applied to the conductive AFM tip and current through the nanowire I_{ds} is measured for fixed bias voltage V_{ds} as a function of tip position, with the probe tip serving as a top gate to the nanowire in a three-terminal device measurement.

growth, nanowire diameters typically were in the range of 40–100 nm. Following sonication to release the nanowires into solution, the nanowires were deposited onto a 600 nm SiO_2 layer produced by thermal oxidation on a n^+ Si (001) substrate. Electron beam lithography followed by 15 nm Ti/85 nm Al metallization and a standard lift-off process was used to create Ohmic contacts to the randomly positioned nanowires. The well-known phenomenon of Fermi-level pinning above the conduction-band edge of InAs (Ref. 21) enabled ready formation of low-resistance Ohmic contacts to the InAs nanowires. After two-terminal devices were fabricated in this manner, a 20 nm SiO_2 layer was sputtered on top of the sample to prevent damage to the nanowires when large bias voltages are applied via a conducting probe tip in the SGM measurement. Finally, the microfabricated Ohmic contact pads are wire bonded to a custom built sample holder using a 10 μm diameter Au wire for connection to external electronic instrumentation.

Figure 1 shows a schematic diagram of the experimental configuration used in the scanning gate microscopy measurement. A dc potential $V_g \equiv V_{\text{tip}}$ is applied to the AFM probe tip, while a separate bias voltage V_{ds} is applied between the source and drain contacts to the InAs nanowire, with the source contact grounded. The resistance or conductance of the nanowire is then measured as a function of tip position over the nanowire. The biased AFM probe tip, acting as a local gate contact, changes the electrostatic potential of the nanowire, and induces either accumulation or depletion of electrons, depending on the bias voltage, and in this way alters the nanowire conductance. While scanning the tip over the sample at a fixed tip voltage at a typical scan speed of 1.8 μm/s, the image of the nanowire current as a function of tip position can be used to reveal different responses to changes in the electrostatic potential at each local position inside the nanowire. In the SGM measurement, the system performs a two-pass scan: on the first pass, the topography of the sample surface is recorded, and on the second pass, the tip is lifted to a predefined height, 5 nm in this measurement,

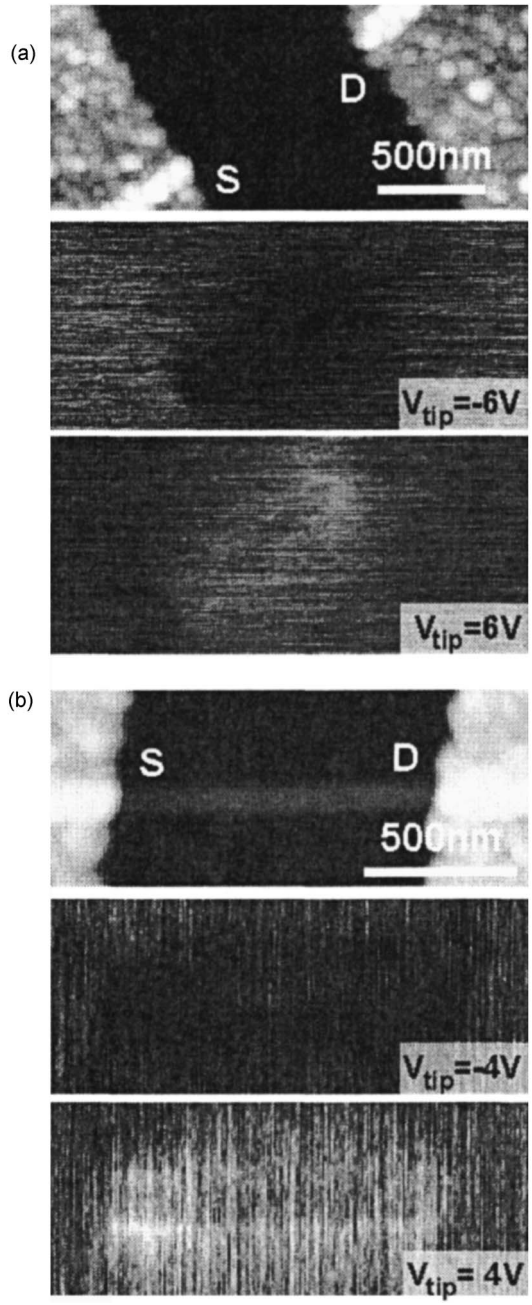

FIG. 2. (a) AFM topograph and SGM images of InAs nanowire at low bias voltage (V_{ds}=0.045 V). (b) AFM topograph and SGM images at high bias (V_{ds}=0.3 V). In the current images, the darker regions are where the current is reduced as the AFM tip depletes the nanowire.

and follows the topographic profile while at the same time, a voltage is applied and nanowire current measured. In this manner, topographically induced imaging artifacts can be minimized or eliminated.

III. RESULTS AND DISCUSSION

Figure 2 shows AFM topographs of an InAs nanowire and the source and drain Ohmic contacts to the wire, from which a channel length of ~1 μm and a nanowire diameter of 45 nm (corresponding to the nanowire height measured by

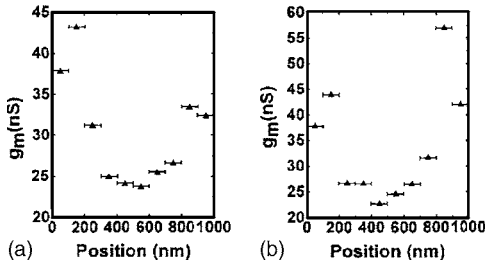

FIG. 3. Transconductance g_m generated from the SGM current images as a function of tip-source contact distance, for a device with source-drain separation of 1 μm at (a) high drain bias (V_{ds}=0.3 V) and (b) low drain bias (V_{ds}=0.045 V).

AFM) can be determined. Figure 2(a) shows an AFM topograph and SGM current images acquired for a fixed drain-source bias V_{ds}=0.045 V (low field) at V_g=−6 and +6 V and a scan frequency of 0.3 Hz. The current data were captured around every 6 nm on the sample. At V_g=−6 V, we can see that the current flow through the InAs nanowire is reduced when the tip is scanned over the nanowire (darker region in the current image), which occurs due to the electron depletion under the negatively biased tip. For V_g=+6 V, the SGM image reveals that current through the nanowire increases (bright region in the current image), due to increased electron accumulation and electrical conductivity in the portion of the nanowire closest to the probe tip.

Figure 2(b) shows an AFM topograph and SGM current images acquired for V_{ds}=0.3 V (high field), at V_g=−4 and +4 V. Behavior qualitatively similar to that observed at low fields is observed, with current flow through the nanowire decreased at negative gate (tip) bias voltages and increased for positive gate voltages. We also note that, for both low and high field conditions, the strongest current modulation is observed when the gating probe tip is positioned near one of the metal contacts. As discussed below, we expect, and have confirmed via numerical simulations, that the strongest current modulation is indeed to be expected near the contacts rather than at or near the midpoint of the nanowire, and the observed asymmetry in current modulation near the contacts may be a consequence of the nature of potential barrier formation in the nanowire channel. In addition, the SGM images at both low and high fields show that current modulation is stronger when the probe tip is located near the edge of, rather than directly atop, the nanowire. We interpret this observation as a consequence of the fact that, given the approximately conical shape of the probe tip, the effective tip-sample contact area is substantially larger when the probe tip is near the edge of the nanowire than when located directly atop the nanowire axis, and the possibility that the insulating SiO_2 layer between the tip and nanowire is thinner on the sides of the wire than on top.

The observation in Fig. 2 that at both positive and negative tip bias, carrier modulation is stronger when the tip is near the source or drain contact, and diminishes towards the midpoint between the two, can be analyzed more quantitatively. Figure 3(a) shows the transconductance, $g_m \equiv dI_{ds}/dV_g$, extracted from a series of SGM images obtained at high drain bias, V_{ds}=0.3 V, as a function of tip bias voltage for several different distances between the tip apex and the source contact. Each data point is obtained by averaging the measured current in the nanowire over a 100 nm interval along the length of the nanowire. The transconductance, corresponding to the slope of each I_{ds}-V_{tip} curve, is then a measure of the effectiveness of the probe tip in modulating current flow in the nanowire. From the figure we see that the transconductance peaks for the interval corresponding to distances of 100–200 nm from the source contact are slightly lower for distances of 0–100 nm from the contact, and decrease steadily as distance to the source contact increases: g_m in these measurements increases by as much as ~80% as the tip moves from the midpoint between the source and drain contacts to the interval at which maximum transconductance is observed. Qualitatively similar behavior but with slightly lower transconductances is observed near the drain contact. The transconductance values observed here are relatively low, which we attribute to a combination of three factors: (i) the probe tip effectively contacts only a small fraction of the nanowire circumference, reducing its ability to modulate carriers within the nanowire; (ii) there is a small (~5 nm) air gap between the probe tip and the sample surface, which substantially reduces the gate capacitance per unit area; and (iii) the relatively high tip scan speed effectively results in a high voltage slew rate, which separate studies have shown reduces nanowire carrier modulation due to the presence of charged trap states at the InAs surface.[22]

Figure 3(b) shows g_m as a function of gate (probe tip) location, obtained in the same manner as described above, for low drain bias, V_{ds}=0.045 V. Once again, we see that g_m is minimized when the gate is near the midpoint between the source and brain contacts, and maximized approximately 100–200 nm away from each contact. For low drain bias, an increase in g_m of as much as ~120% is observed as the probe tip position moves from the midpoint of the InAs nanowire to the intervals at which maximum transconductance is observed. In comparing the transconductance behavior in the low and high drain bias regimes, we note that for high drain bias the transconductance is greatest near the source contact, while for low drain bias the transconductance is greatest near the drain contact. While asymmetries at the nanoscale in InAs nanowire structure or contact morphology may contribute to these observations, an additional factor under high drain bias conditions may be that local gate modulation near the source contact will create a barrier for electron transport into the channel, thereby increasing the transconductance, while for gate modulation near the drain contact carriers accelerated by the electric field within the channel may be able to surmount the local gate-induced potential barrier, as has been postulated for high-bias transport in carbon nanotubes.[23] In addition, we note that the transconductance as a function of distance from the source contact to the nanowire is very similar for both low and high drain bias except near the drain contact; this suggests that most of the potential drop within the nanowire associated with applica-

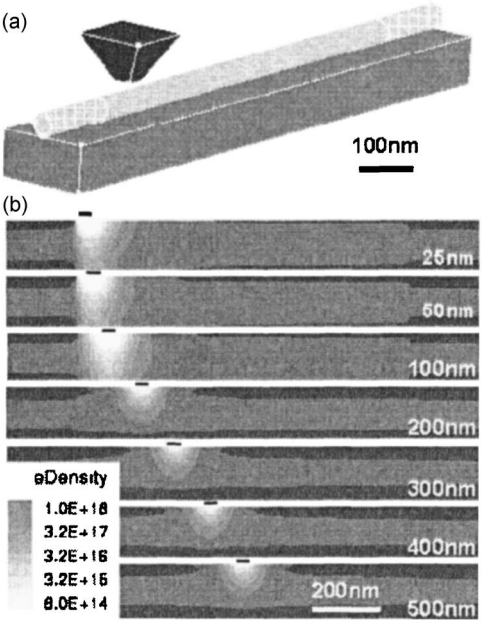

FIG. 4. (a) Schematic 3D geometry used in the ISE simulation of gating effect in the tip-nanowire structure. (b) Two-dimensional cross section of electron concentration in the nanowire as a function of tip distance from the source contact at $V_g=-5$ V for tip-contact distances of 25, 50, 100, 200, 300, 400, and 500 nm. The black bar above each cross section indicates the tip position. All data are shown on the same scale, showing that gate modulation is more pronounced when the gate is close to the metal source or drain contact.

tion of V_{ds} occurs near the drain contact—otherwise, g_m for this range of bias voltages would be expected to increase approximately linearly with V_{ds}.[16]

To further assist in the interpretation of these SGM results, we have performed detailed numerical simulations of the device and probe tip structures employed in the SGM measurements. A few groups have attempted to model the electrostatic potential of the scanning gate structure combined with a carbon nanotube or nanowire.[24,25] However, these models are mostly quite simple and do not account for certain key factors in the SGM experiment, such as tip geometry and boundary conditions between different dielectrics and the semiconducting nanowire material. We have therefore performed a three-dimensional (3D) numerical simulation of the measurement structure using the Integrated System Engineering[26] (ISE) simulator, taking into account the factors mentioned above.

Figure 4(a) shows the schematic configuration of the 3D structure used in the ISE simulations. A 50 nm diameter InAs nanowire with channel length of 1 μm is placed on top of 100 nm SiO_2. The dopant concentration in the bulk region of the n-type nanowire is 5×10^{16} cm^{-3}. To account for the Fermi-level pinning in the conduction band of InAs at the surface, we introduce an electron concentration of 1×10^{18} cm^{-3} in a cylinder within 10 nm of the nanowire surface. Previous studies[27] suggest that at this concentration, the Fermi level is pinned above the conduction band edge at an energy very close to previously reported experimental and theoretical values.[28] Source and drain contacts 200 nm in length are placed at both ends of the nanowire and set to ground potential. A pyramid-shaped probe, with tip diameter ~30 nm, is positioned 20 nm above the nanowire and a dc bias voltage is applied to the probe. The rest of the space in the figure is defined as vacuum for the purpose of setting up the 3D meshes. Electrostatic potential, electron concentration, electric field, etc., at each mesh point are calculated using the finite element method to solve Poisson's equation.

Figure 4(b) shows the simulated electron concentration distribution in a two-dimensional cross-sectional plane bisecting the nanowire along its axis. As indicated in the figure, a conductive AFM tip, biased at −5 V, is placed at different distances from the contact, ranging from 25 to 500 nm. When the tip is close to a contact, i.e., 25–100 nm from the left contact in the figure, the electrons are fully depleted both at the surface and in the bulk of the nanowire under the tip. When the tip is positioned farther from the contact, the depletion is weaker and only electrons at the surface are fully depleted; minimum depletion occurs when the tip is above the center of the nanowire. It should be noted that the maximum depletion is achieved at a distance of 100 nm. This is because when the tip is very close to the source, the screening effect from the metal becomes significant, thus weakening the effective carrier modulation from the gate. The maximum carrier modulation at 100 nm is a combined result of these gating and screening effects. The same behavior is observed experimentally in the scanning gate measurements, although in the SGM measurements there is the additional possibility of the tip-nanowire separation increasing when the distance between the tip and sample is comparable to the probe tip radius (~20–50 nm) due to the nonzero contact metallization thickness causing the tip to ride up the contact. These results corroborate and help us explain more fully the SGM measurement results, confirming that the current contrast shown in Fig. 2 arises from position-dependent modulation of the nanowire electron concentration by the local top gate.

These results offer important information on the effect of gate geometry and position on carrier modulation that is likely to be useful in the design of highly scaled nanowire-based and potentially other nanoelectronic devices. We see, in both experimental measurements and simulation, that carrier modulation by the narrow top gate strongly depends on the gate position. When the tip is near the source or drain electrode, the carriers are modulated more effectively, which means the device can be turned on and off more easily and, correspondingly, the i_{on}/i_{off} ratio and transconductance should be larger. In addition, at large source-drain bias voltages V_{sd}, the combined effects of V_g and V_{ds} can influence the channel potential profile and lead to maximization of transconductance for gate positions specifically near the source rather than the drain contact. Such positioning of the gate would also be consistent with the desire in a field-effect transistor to minimize source resistance via reduction of the gate-source separation, and to enable realization of increased breakdown voltages by increasing the gate-drain spacing.

IV. CONCLUSIONS

In summary, we have performed scanning gate microscopy studies and numerical simulations of an InAs semiconductor nanowire with a local conductive probe acting as a gate contact, and we have shown that electron concentration and current modulation in a scaled semiconductor nanowire device can be strongly dependent on the gate geometry: carrier and current modulation is strongest when the local gate contact is near the source and drain contact regions, and weakens when the gate is moved farther away from the contacts. Experimentally, variations in transconductance up to approximately 80% are observed as the probe tip serving as the gate contact is moved from the midpoint between the source and drain contacts to the point of maximum current modulation near the source in the high field measurement, and up to 120% for gate positions near the drain in the low field measurement. 3D numerical simulations confirm that carrier modulation is maximized when the gate (probe tip) is positioned ~100 nm from the source or drain contact, and steadily decreases as the probe tip is moved away from the contact. For tip-contact distances of less than ~100 nm, numerical simulations show that screening by the metal contact reduces carrier modulation, corroborating experimental observations of a reduction in transconductance as the probe tip gate contact is moved very close to the metal contact. We expect that these observations should have substantial implications both for the understanding of carrier transport behavior at the nanoscale, and the design of highly scaled nanowire-based field-effect transistor structures.

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[1]R. Chau *et al.*, IEEE Trans. Nanotechnol. **4**, 153 (2005).
[2]L. Samuelson *et al.*, Physica E (Amsterdam) **21**, 560 (2004).
[3]D. D. Ma, C. S. Lee, F. C. K. Au, S. Y. Tong, and S. T. Lee, Science **299**, 1874 (2003).
[4]C. Thelander, T. Martensson, M. T. Bjork, B. J. Ohlsson, M. W. Larsson, L. R. Wallenberg, and L. Samuelson, Appl. Phys. Lett. **83**, 2052 (2003).
[5]M. H. Huang *et al.*, Science **292**, 1897 (2002).
[6]F. Qian, S. Gradecak, Y. Li, C. Wen, and C. M. Lieber, Nano Lett. **5**, 2287 (2005).
[7]X. Duan, Y. Huang, R. Agarwal, and C. M. Lieber, Nature (London) **421**, 241 (2003).
[8]Y. Cui, Q. Wei, H. Park, and C. M. Lieber, Science **293**, 1289 (2001).
[9]Z. Zhong, D. Wang, Y. Cui, M. W. Bockrath, and C. M. Lieber, Science **302**, 1377 (2003).
[10]R. Beckman, E. Johnston-Halperin, Yi Luo, J. E. Green, and J. R. Heath, Science **310**, 465 (2005).
[11]Q. Wang, A. Javey, R. Tu, H. Dai, H. Kim, P. McIntyre, T. Krishnamohan, and K. Saraswat, Appl. Phys. Lett. **83**, 2432 (2003).
[12]J. Xiang, W. Lu, Y. Hu, Y. Wu, H. Yan, and C. M. Lieber, Nature (London) **441**, 489 (2006).
[13]S. Jin, D. Whang, M. C. McAlpine, R. S. Friedman, Y. Wu, and C. M. Lieber, Nano Lett. **4**, 915 (2004).
[14]J. Goldberger, D. Sirbuly, M. Law, and P. Yang, J. Phys. Chem. B **109**, 9 (2005).
[15]D. Wang, Y. Chang, Q. Wang, J. Cao, D. Farmer, R. Gordon, and H. J. Dai, J. Am. Chem. Soc. **126**, 11602 (2005).
[16]S. A. Dayeh, D. P. R. Aplin, X. Zhou, P. K. L. Yu, E. T. Yu, and D. Wang, Small **3**, 326 (2007).
[17]J. Chen, S. Klaumuenzer, M. C. Lux-Steiner, and R. Koenenkamp, Appl. Phys. Lett. **85**, 1401 (2004).
[18]J. Goldberger, A. I. Hochbaum, R. Fan, and P. Yang, Nano Lett. **6**, 973 (2006).
[19]M. A. Topinka, B. J. LeRoy, S. E. J. Shaw, E. J. Heller, R. M. Westervelt, K. D. Maranowski, and A. C. Gossard, Science **289**, 2323 (2000).
[20]A. Bachtold, M. S. Fuhrer, S. Plyasunov, M. Forero, E. H. Anderson, A. Zettl, and Paul L. McEuen, Phys. Rev. Lett. **84**, 6082 (2000).
[21]C. A. Mead and W. G. Spitzer, Phys. Rev. Lett. **10**, 471 (1963).
[22]S. A. Dayeh, C. Soci, P. K. L. Yu, E. T. Yu, and D. Wang, J. Vac. Sci. Technol. B (accepted).
[23]M. Freitag, Y. Zhou, A. T. Johnson, and W. F. Smith, Appl. Phys. Lett. **79**, 3326 (2001).
[24]M. Freitag and A. T. Johnson, Phys. Rev. Lett. **89**, 216801 (2002).
[25]Thomas Ihn, Springer Tracts Mod. Phys. **192**, 223 (2004).
[26]Integrated System Engineering (ISE), Technology CAD (TCAD) software products, covering processing, device modeling, circuit, and system simulation up to package simulation.
[27]X. Zhou, S. A. Dayeh, D. Aplin, D. Wang, and E. T. Yu, J. Vac. Sci. Technol. B **24**, 2036 (2006).
[28]C. A. Mead and W. G. Spitzer, Phys. Rev. Lett. **10**, 471 (1963).