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# Diameter-Independent Hole Mobility in Ge/Si Core/Shell Nanowire Field Effect Transistors

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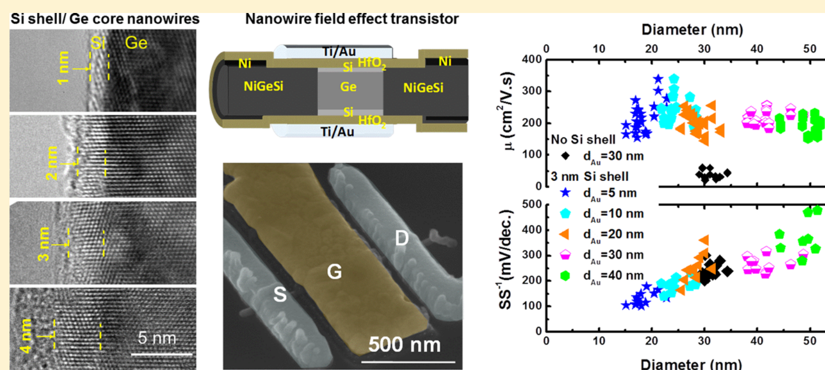
Supporting Information




**ABSTRACT:** Heterostructure engineering capability, especially in the radial direction, is a unique property of bottom-up nanowires (NWs) that makes them a serious candidate for high-performance field-effect transistors (FETs). In this Letter, we present a comprehensive study on size dependent carrier transport behaviors in vapor−liquid−solid grown Ge/Si core/shell NWFETs. Transconductance, subthreshold swing, and threshold voltage exhibit a linear increase with the NW diameter due to the increase of the transistor body size. Carrier confinement in this core/shell architecture is shown to maintain a diameter-independent hole mobility as opposed to surface-induced mobility degradation in homogeneous Ge NWs. The Si shell thickness also exhibits a slight effect on the hole mobility, while the most abrupt mobility transition is between structures with and without the Si shell. A hole mobility of 200 $cm^2/(V\cdot s)$ is extracted from transistor performance for core/shell NWs with a diameter range of 15−50 nm and a 3 nm Si shell. The constant mobility enables a complete and unambiguous dependence of FET performance on NW diameter to be established and provides a caliper for performance comparisons between NWFETs and with other FET families.

**KEYWORDS:** *Ge/Si, core/shell, nanowire, field effect transistor, mobility, diameter dependence, bandgap engineering*

Ge/Si core/shell nanowires[1] (NWs) have been receiving a lot of attention due to their epitaxially abrupt interfaces and the special type II band alignment between the two constituent materials. They offer great flexibility in material growth beyond that achieved in planar films[2] and therefore additional potential for band-edge and strain engineering for diverse applications such as electronics,[3−8] thermoelectrics,[9−11] and energy harvesting.[12,13] The role of the Si shell on electrical transport properties has been previously demonstrated,[3,14] showing an enhanced conductivity associated with hole accumulation in the Ge NW core due to the lower valence band-edge level in the Si shell than in the Ge core. High-performance field-effect transistors (FETs) based on Ge/Si core/shell NWs have been realized[4] and exhibited superior performance compared to planar Si p-MOSFETs.[6] Recently, a performance comparison of Ge/SiGe core/shell NWFETs with different Si content in the SiGe shell revealed that enhanced mobility due to stronger confinement with higher Si content was responsible for the FET performance improvement.[7] Based on these significant advances, it is important to distinguish the roles of carrier accumulation and carrier confinement on performance enhancement and determine how these would evolve with different core/shell thicknesses.

Diameter-dependent charge transport has been widely utilized to assess the impact of surface scattering on carrier mobility in NW devices. The trend for mobility is highly materials and device structure dependent as the literature has shown opposite trends.[15] Most commonly, carrier mobility in NWs with smaller diameters is observed to decrease, due to a greater influence of surface scattering processes,[15−20] impairing the demand for smaller diameter devices for reduced short channel length effects.[21] However, some other NW materials and device structures with sub-10 nm diameters or in highly strained systems exhibit enhanced mobility attributed to strain-

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induced change in the band structure.[22,23] These inconsistent mobility trends for different material systems suggest the necessity for additional detailed and systematic studies that can validate the use of certain performance figures of merit for comparison between NWFETs and with other FET technologies.

In this Letter, a comprehensive diameter dependence study was conducted from a large number of Ge/Si NWs with different diameters. The diameter-dependent trends are presented for a wide set of figures of merit in VLS grown NWFETs: transconductance ($g_m$), subthreshold swing ($SS^{-1}$), and threshold voltage ($V_T$). The linear increase of the transconductance with the diameter suggests that the hole mobility stays constant in the diameter range of the study (15–55 nm), proving the advantage of heterostructured Ge/Si core/shell architecture in minimizing surface scattering processes. The constant mobility in turn ensures that the performance dependency on diameter is due to device geometry. Small diameter NWFETs exhibit a steep subthreshold slope and a small threshold voltage, while larger diameter NWFETs suffer from a gate-bias sensitive, large subthreshold slope and threshold voltage due to more severe short-channel length effects.

For this work, Ge/Si core/shell NWs were grown in a low pressure, cold wall chemical vapor deposition (CVD) system using the previously reported conditions.[24] Ge core NWs on Ge (111) substrates were grown using Au colloids with nominal diameters of 5, 10, 20, 30, and 40 nm, and the Si shell thicknesses were calibrated to be 0 (no Si shell), 1, 2, 3, and 4 nm in different growth runs. The actual Si shell thickness was measured by high-resolution transmission electron microscopy (HRTEM) as shown in Figure 1a–d. For NWFET fabrication, NWs were sonicated and suspended in isopropyl alcohol (IPA) then drop-casted on a $Si_3N_4$ template with predefined contact pads and alignment marks. E-beam lithography and e-beam metal evaporation were utilized for 130 nm thick Ni source/drain contacts, followed by a 30 s rapid thermal annealing (RTA) at 300 °C to facilitate solid state reaction between Ni and Ge/Si to form $NiGe_x/NiSi_y$ ohmic contacts to the NW,[6] as depicted schematically in Figure 1e. The device channel length ($L$) after RTA was measured by scanning electron microscopy (SEM) (Figure 1f) After atomic layer deposition of $HfO_2$ gate dielectric, 400 nm width, 30 nm Ti/100 nm Au thick gate contacts were designed to fully overlap the source/drain contacts to minimize stray resistance of the ungated NW segments (Figure 1g). Further details on the growth and device fabrication can be found in ref 25.

The diameter-dependent transport behavior is revealed from the first batch of devices that utilized NWs grown from nominally 5, 10, 20, 30, and 40 nm Au colloids with 3 nm Si shells. The $HfO_2$ dielectric thickness was fixed at 10 nm as calibrated by HRTEM (not shown). Figure 2 shows the transfer curves ($I_{DS}$ vs $V_{GS}$) at $V_{DS}$ = −100 mV of representative NWFETs from each group of Au colloid diameter. All devices exhibit p-type FET characteristics with the on-regime at negative $V_{GS}$ voltages. The current increase at large positive $V_{GS}$ is due to the electron conduction. This ambipolarity behavior was previously observed in Ge/Si NWFETs and can be eliminated by partially overlapped gate configuration.[4] Despite the Ge NW's diameter being in the middle of the core/shell NWs' diameter range, a distinct $I_{DS}$–$V_{GS}$ characteristic between the Ge NWFET (black curve) and the core/shell devices (colored curves) is observed. The Ge NWFET is a

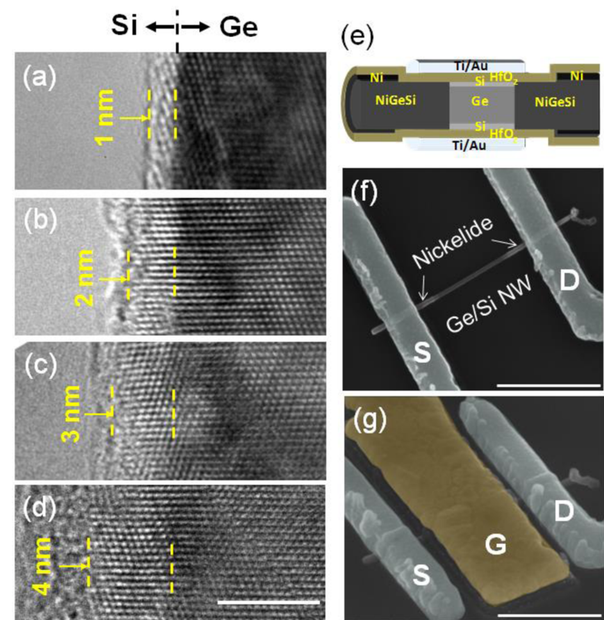


**Figure 1.** High-resolution transmission electron micrographs of Ge/Si core/shell NWs illustrating precise control of Si shell thickness: (a) $t_{Si}$ = 1 nm, (b) $t_{Si}$ = 2 nm, (c) $t_{Si}$ = 3 nm, and (d) $t_{Si}$ = 4 nm. Scale bar = 5 nm. (e) Schematic diagram of the device structure. (f) Top-view scanning electron micrograph of a device after drain/source formation and rapid thermal annealing; reacted $NiGe_x/NiSi_y$ segments are in bright contrast. (g) 45° tilt SEM image of a complete device structure with gate metal overlapping with the reacted $NiGe_x/NiSi_y$ drain/source. Scale bars for f and g are 500 nm.

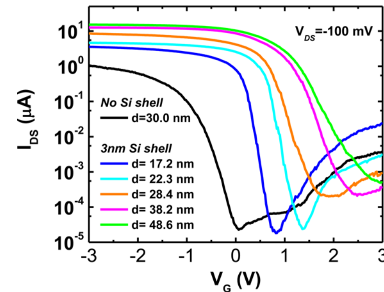


**Figure 2.** $I_{DS}$ vs $V_{GS}$ transfer curves at $V_{DS}$ = −100 mV of representative devices with different diameters from different Au colloids. The shell thickness for all samples is 3 nm, except for the reference homogeneous Ge NW with no Si shell.

normally off device, while core/shell devices are normally on, due to hole accumulation associated with the band offset between the Ge core and the Si shell.[3] This accumulation induces to a shift of threshold voltage toward positive $V_{GS}$ for core/shell structures; however, it could not explain the superior on-current in the negative $V_{GS}$ range. The higher on-currents in the core/shell devices compared to Ge core only devices are due to the enhanced hole mobility as will be discussed in detail below. Among the core/shell NWFETs, there is also a clear trend with diameter. Lager diameter NWFETs possess larger on-current but suffer from a worse subthreshold swing, as indicated by the more slanted slope in the subthreshold regime. The turn-point of the ambipolar behavior is also seen to be diameter-dependent.

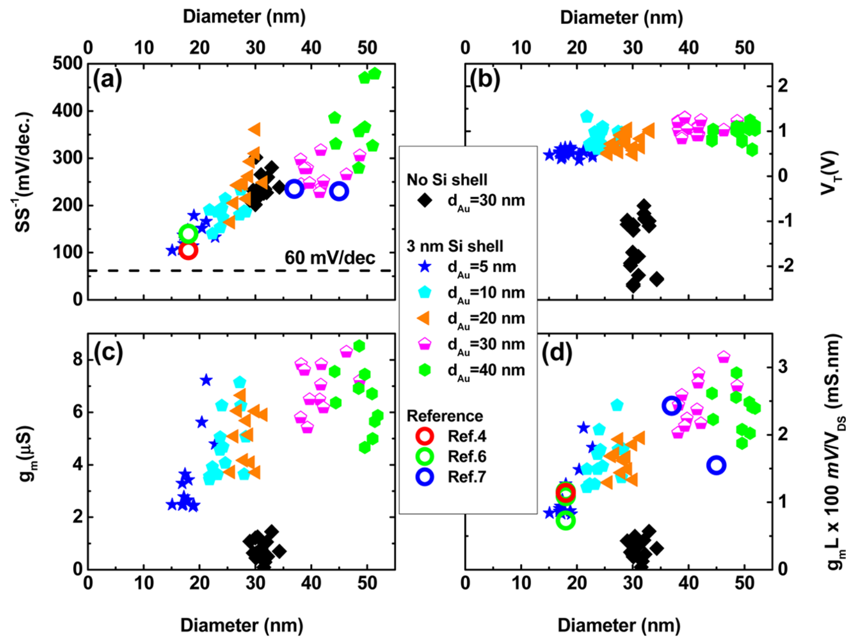


**Figure 3.** NW FET performance as a function of diameter: (a) subthreshold swing, (b) threshold voltage, (c) maximum transconductance, and (d) maximum transconductance-channel length product. Data from refs 4, 6, and 7 are normalized and added in panels a and d for comparison.

To better assess the diameter dependencies, basic FET characteristics were extracted from the transfer curves using eqs 1−3 and are displayed in Figure 3.

$$SS^{-1} = \left(\frac{d \log|I_{DS}|}{dV_{GS}}\right)^{-1} = kT \ln 10\left(1 + \frac{C_{dep} + C_{trap}}{C_{ox}}\right) \quad (1)$$

$$g_m = \frac{d|I_{DS}|}{dV_{GS}} = \frac{\mu C_g V_{DS}}{L^2} \quad (2)$$

$$V_T = V_{FB} + 2\psi_s - \frac{Q_{dep}}{C_{ox}} \quad (3)$$

where $C_{dep}$, $C_{trap}$, and $C_{ox}$ are the depletion, interface trap, and oxide capacitance respectively, $\mu$ is the hole mobility, $C_g$ is the gate capacitance, $L$ is the channel length, $V_{FB}$ is the flat band voltage, $\psi_s = [E_i - E_F]/q$ is the material parameter at $V_{FB}$, and $Q_{dep}$ is the fixed charge density in the space-charge region depleted from free carriers in the off-state. In eqs 1 and 2, the middle expressions of the equations are the definition for the terms that can be evaluated from experimental measurements, and the far right-hand sides of the equations are their theoretical correlation with intrinsic FET parameters. The extracted SS$^{-1}$ and $g_m$ are taken at the minimum and maximum of the derivative data, respectively.

In Figure 3a, the subthreshold swing shows a monotonic decrease with decreased diameters in the studied range. At smaller diameters, the trend should asymptotically approach the thermal limit of ~60 mV/dec. The minimum SS$^{-1}$ of ~100 mV/dec for ~17 nm diameter is larger than the thermal limit but is among the best subthreshold swings reported for Ge/Si NWFETs.[4] The deviation from the thermal limit is commonly believed due to the presence of interface traps but can also come from intrinsic geometrical design of the device, as has been reported for SOIFETs.[26−29] Interestingly, data for Ge NWFET without the Si shell line up perfectly with the trend for Ge/Si core/shell devices. This is because the SS$^{-1}$ is governed by static capacitances, which do not involve carrier concentration or mobility, thus are solely dependent on geometrical form of the devices and their surface quality. The threshold voltage ($V_T$), however, is dependent on the carrier concentration and therefore shows a clear delineation between core/shell and homogeneous Ge NWs (Figure 3b). Holes accumulated in the Ge core of the Ge/Si core/shell structure require a larger voltage to deplete, hence larger $V_T$.

In the on-regime above threshold, the superior transconductance of core/shell NWFETs to homogeneous Ge NW devices is due to the change in mobility. As can be seen from eq 2, the transconductance is dictated by the mobility and gate capacitance. The latter quantity depends mostly on the geometrical shape of the devices and thus should not have much variation from Ge NWs to Ge/Si core/shell NWs. For core/shell devices, the $g_m$ and $g_mL$ also show an increasing trend with diameter (Figure 3c−d). Due to the variation of NWFETs' channel length (between 250 and 450 nm for all devices tested), which is caused by nonuniform extension of NiGe/NiSi segments for a fixed annealing condition, the extracted $g_m$ data are spread out for a given diameter and their variance reduces when $g_m$ is multiplied with the channel length measured with SEM. In fact, the $g_mL$ quantity equals to the $\mu C_g V_{DS}/L$ term, which is channel length independent (see eq 4 for C or $C_g$), assuming negligible tangential fringing on the capacitances. A small deviation from large diameter data points ($d_{Au}$ = 40 nm) is likely due to the incomplete coverage of metal contacts (source/drain or gate), which was observed under SEM (not shown). The diameter-dependent trend of $g_mL$ product is similar to the quasi linear dependence of the gate capacitance, suggesting that the hole mobility stays constant with diameter, which will be justified in detail below (see Figure 6 and associated discussion).

Data from refs 4, 6, and 7 are added in panels a and d of Figure 3 for comparison. The discrepancy of SS$^{-1}$ in ref 4 and 6 vs ref 7 can now be justified by the diameter dependence of the subthreshold swing as they all line up with the trend drawn by this work. In Figure 3d, the $g_mL$ product is normalized with $V_{DS}$

($g_mL \times 100$ mV/$V_{DS}$) to account for different measurement voltages. Coincidently, all works utilized similar gate dielectric thickness (4 nm $HfO_2$ and 7 nm $ZrO_2$ in refs 4 and 6 and 8 nm $HfO_2$ in ref 7 in comparison with 10 nm $HfO_2$ in this work), which enables a similar trend for $g_mL$.

To reinforce the above analysis, charge distribution as a function of gate voltage was numerically simulated by solving the Poisson-Schrodinger equations with a 2D Atlas simulator by Silvaco Inc. Simulation parameters are listed in the Supporting Information. Interface traps were intentionally excluded to reflect the intrinsic diameter dependence of the nanowire geometry and thus the resulting simulations are only intended to provide a qualitative description of the detailed device operation. The interface traps, however, are significant in the subthreshold regime, as evidenced in the $SS^{-1}$ values above the thermal limit. Figure 4a shows the simulated hole

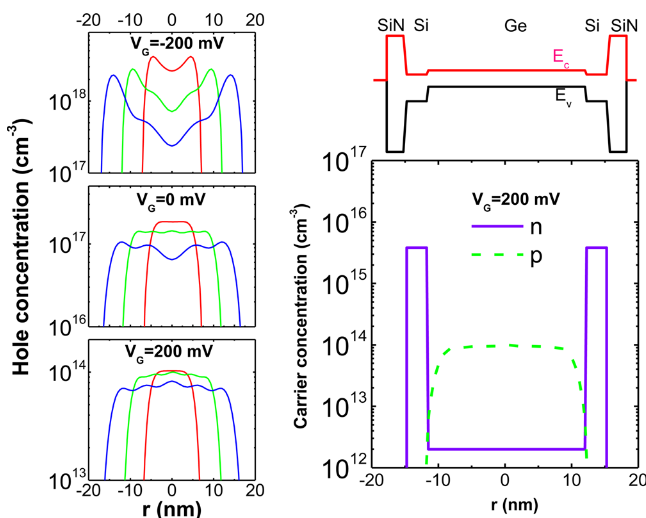


**Figure 4.** Numerical simulation of carrier concentration with Atlas, Silvaco. (a) Hole concentration at $V_{GS}$ = −200 mV (on-regime), 0 mV (subthreshold), and 200 mV (ambipolar turn on), respectively, and (b) conduction/valence band alignment and electron/hole density profile at $V_{GS}$ = 200 mV.

concentration profile of core/shell NWs with a 3 nm Si shell and a total diameter of 10, 20, and 30 nm, respectively. $V_{GS}$ = −200 mV illustrates the on-regime where holes are attracted toward the NW's perimeter, and their density peaks at ∼2−3 nm from the Ge/Si interface due to the quantum confinement effect.[30] This agrees with the experimental observation that the transconductance (proportional to total number of carriers) scales with diameter. At $V_{GS}$ = 0 mV the device gets into the subthreshold regime where holes are repelled from the NW surface. It would require more voltage to deplete larger diameters, thus giving rise to larger $V_T$ and $SS^{-1}$ values for larger diameters. $V_{GS}$ = 200 mV depicts the deep subthreshold regime with smaller hole concentrations and smaller hole currents. However, as shown in Figure 4b, electrons in the conduction band are attracted by the positive gate voltage and reside in the Si shell. Since the gate overlaps with the drain, the action of the gate bias also reduces the depletion width of the Schottky barrier at the interface between the metallic NiGe/NiSi contact and the semiconductor NW. This facilitates electron tunneling through the barrier and causes the ambipolar behavior as observed experimentally.

As discussed earlier, one of the main goals of this study is to assess intrinsic parameters of the core/shell NW materials such as carrier mobility, based on the experimental diameter dependent trends. However, before performing data processing and extraction, it is important to evaluate possible sources of error, for example the contribution of contact resistance, and effects of Si shell and $HfO_2$ thicknesses. Transmission line measurements (TLM) were performed on a separate set of individual NWs to extract the contact resistance. Details of the fabrication and measurement are described in the Supporting Information. Consistently, the contact resistance between NiGe/NiSi and Ge/Si is below 10 kΩ, which is well below the total wire resistance (∼100 kΩ) at the voltage conditions where $g_m$ is extracted (Figure S3). The contact resistance is thus considered negligible and should not require additional correction in the extraction of mobility. For the effect of oxide and shell thicknesses, new batches of samples with different $HfO_2$ thicknesses (while keeping the same 3 nm thick Si shell) and different Si shell thicknesses (while keeping the same 10 nm thick $HfO_2$) were processed and measured. Figure 5 summarizes the subthreshold swing and "normalized" transconductance of newly processed devices, referenced with previously presented data for 10 nm thick $HfO_2$ and 3 nm thick Si shell. Both $SS^{-1}$ and $g_mL$ exhibit little sensitivity to the change of Si or $HfO_2$ thicknesses. This is partially because the gate capacitance is composed of the dielectric, shell, and core capacitances in series; thus the effect due to changing one component is minimal. Another contribution to the insensitivity of the performance with $HfO_2$ thickness is the thickness dependence of the $HfO_2$ dielectric. Capacitance measurements on metal−insulator−semiconductor (MIS) structures with different $HfO_2$ thicknesses deposited with the same ALD deposition conditions used for experiments in this study suggested an empirical expression for the dielectric constant: $\varepsilon = 0.485t + 12.9$ with $t$ being the dielectric thickness in nm. This thickness dependent dielectric constant was taken into account for the extraction of mobility shown in Figure 6. In this extraction, dielectric, shell, and core (centroid) capacitances are modeled analytically using cylindrical capacitance approximation

$$C = \frac{2\pi\varepsilon L}{\ln(r_{out}/r_{in})} \tag{4}$$

where $\varepsilon$ is the material's dielectric constant, $L$ is the channel length, and $r_{out,in}$ are the outer and inner radii of the capacitor. The dielectric constants of Ge and Si are taken to be 16 and 12, respectively, while that of $HfO_2$ was linearly interpolated from thickness-dependent capacitance−voltage measurements on metal−oxide−semiconductor structures as discussed above. It is important to note that the cylindrical capacitance overestimates actual capacitance due to incomplete coverage of the metal gate over the NWs. In addition, the interface state capacitance further reduces the gate capacitance; thus the extracted mobility is an underestimated value.[31] As illustrated in Figure 6a−b, the extracted lower bound mobility is not sensitive to the NW's diameter and stays in the range of 150−250 $cm^2/(V\cdot s)$. More scattered data in the small diameter range are due to larger error in measuring the NW size with SEM. The $HfO_2$ thickness does not appear to affect the mobility. The Si shell, however, is crucial to achieve high mobility. Without the Si shell (homogeneous Ge NWs), the mobility is only 40−50 $cm^2/(V\cdot s)$, while the presence of the shell enhances the mobility by a factor of 4−5. This is a strong evidence for the


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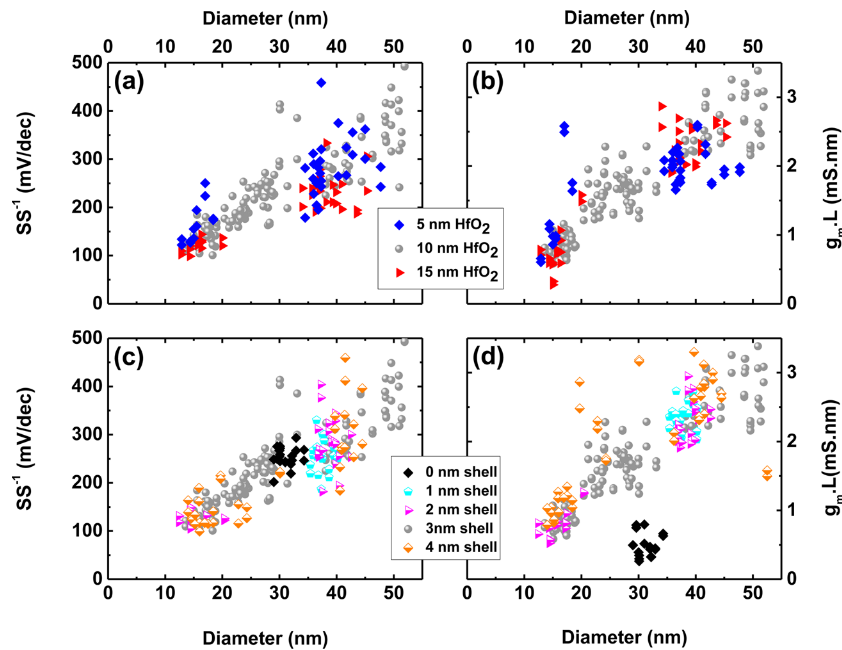


**Figure 5.** Effect of the $HfO_2$ thickness on (a) $SS^{-1}$ and (b) maximum $g_mL$ product at $V_{DS} = -100$ mV; and effect of the Si shell thickness on (c) $SS^{-1}$ and (d) maximum $g_mL$ product at $V_{DS} = -100$ mV.

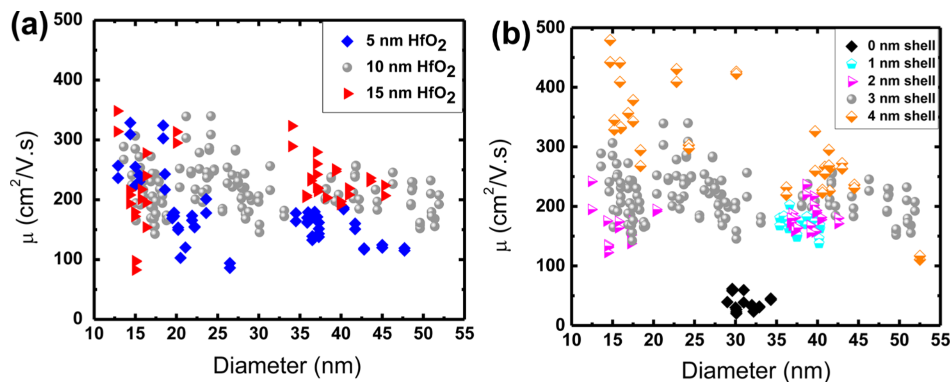


**Figure 6.** Extracted lower bound hole mobility in core/shell NW FETS with (a) different $HfO_2$ dielectric thicknesses and (b) different Si shell thicknesses.

advantage of the Ge/Si core/shell structure over homogeneous Ge NWs. As the Si shell gets thicker from 1 to 4 nm, the hole mobility increases slightly, and the Si shell capacitance decreases. These two effects compensate each other in the transconductance expression which remained insensitive to the Si thickness as shown in Figure 5d. This mobility improvement with increased Si shell thickness can be attributed to a number of reasons. First, a thicker Si shell increases carrier confinement such that holes reside further from the semiconductor/dielectric interfaces and become less subject to detrimental surface scattering. Second, thicker Si could induce more compressive strain on the Ge core, which enhances the hole mobility as proven both theoretically[32] and experimentally.[33,34] Lastly, thicker Si shells with smaller capacitance could reduce the orthogonal field of the gate bias, thus alleviating the field-induced mobility reduction. The constant mobility observed in our experiment justifies the linear dependence of transconductance with diameter (Figure 3c) and experimentally validates the normalization of on-characteristics with diameter for comparison between different sizes or different NW technologies. Based on the above analysis and experimental observation, the core diameter rather than the total diameter should be used for the normalization. In this work, $g_m/d_{core} \sim$ 285 $\mu$S/$\mu$m for core/shell devices with 250 nm channel length and measured at $V_{DS} = -100$ mV. This normalized value is similar to the best reported results[4,6,7] when accounting for a voltage and channel length differences as shown in the discussion of Figure 3a,d. The extracted mobilities in different works, however, are scattered within the same order of magnitude (despite similar oxide thicknesses), likely due to different values taken for the dielectric constant, and different approximations used for the gate capacitance. Nevertheless, the difference in mobility extraction methods will not alter the conclusion on constant mobility with diameter, as it is calculated consistently using the same approximation.

The devices were then measured at different source/drain voltages ($V_{DS}$) to assess the bias dependence performance of NWFETs with different diameters. The transconductance scales with $V_{DS}$ for all diameters as expected (Figure S4); however, the subthreshold swing stays constant only for small diameter NWs, and those with larger diameters exhibit a worse subthreshold swing at larger bias. This is because large diameter

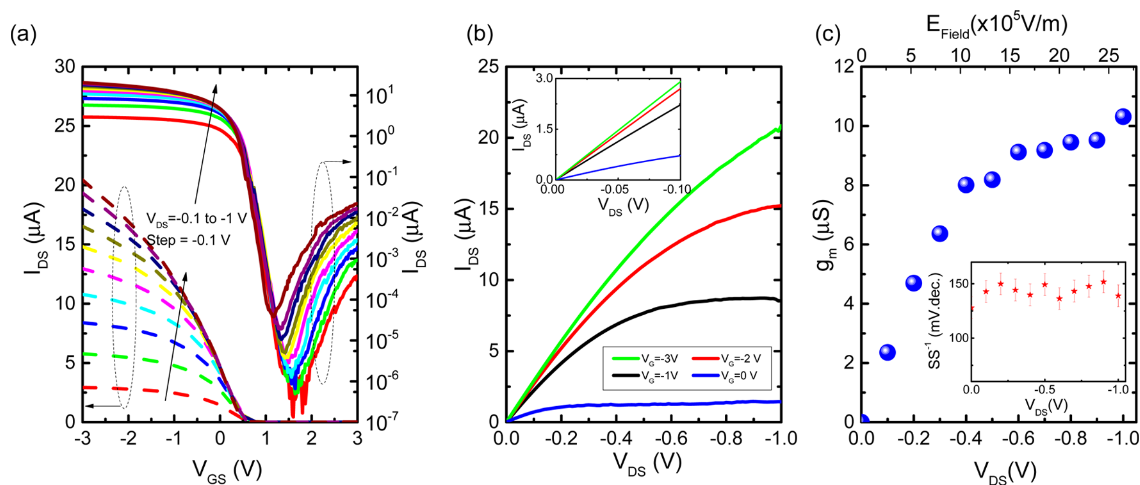


**Figure 7.** (a) $I_{DS}$ vs $V_{GS}$ transfer curves of a 17.2 nm diameter core/shell NWs at different $V_{DS}$, (b) $I_{DS}$ vs $V_{DS}$ output curves of the device at different $V_{GS}$, and (c) maximum transconductance $g_m$ as a function of $V_{DS}$. Inset: $SS^{-1}$ vs $V_{DS}$.

NWs are more prone to the short channel length effects as the $d/L$ ratio is larger for larger diameter. It is also known that larger NWs experience more challenges in the processing, that is, incomplete metal coverage, which were shown to result in more nonuniformity in FET performance compared to that of smaller diameters (Figures 3 and 5). Figure 7a shows the bias-dependent transfer curves of a 17.2 nm diameter core/shell NWFET. It can be seen that the curves maintain the low subthreshold swing over a large current range (more than 6 orders of magnitude for small $V_{DS}$ and more than 4 orders of magnitude for $V_{DS} = -1$ V) before the ambipolarity kicks on at larger gate voltage. The output curves exhibit linear $I_{DS}$ vs $V_{DS}$ relationship at small $V_{DS}$ (Figure 7b, inset), justifying the absence of a Schottky barrier at the contacts. At larger $V_{DS}$, the current is "pinched off" at small gate voltage, and the saturation bias $V_{DS,sat}$ increases with increased $V_{GS}$. The transconductance of the device is shown as a function of $V_{DS}$ (bottom axis) and lateral electric field (top axis—assuming negligible voltage drop across the contacts, i.e., $R_{channel} \gg R_{contact}$ at $g_m$ extraction bias) in Figure 7c. Below −0.4 V, $g_m$ increases linearly with $V_{DS}$, suggesting that the mobility is bias-independent for a small $V_{DS}$ range. At higher bias (field), the mobility starts to decrease because of the saturated velocity at high field. However, the subthreshold swing, as it does not depend on mobility, stays constant across the whole measurement bias range (Figure 7c, inset) indicating minimal short channel effects for this device.

In summary, we have presented a diameter-dependent transport study as strong and comprehensive evidence for the advantages of Ge/Si core/shell NW structures for FET performance. The presence of the Si shell creates a hole accumulation that shifts the threshold voltage of the NWFET toward the positive side and requires larger $V_T$ for a larger diameter. The enhancement in transconductance, however, is due to the confinement of accumulated hole in the Ge core, separating the carriers from the semiconductor/dielectric interface and reducing interface scattering. The constant mobility of ~200 $cm^2/(V{\cdot}s)$ is observed for core/shell NWs with diameter between 15 and 55 nm, while the mobility is degraded to 50 $cm^2/(V{\cdot}s)$ in 30 nm diameter homogeneous Ge NWs due to severe surface scattering. This study also confirms that small diameter NWs are needed for high-performance FETs due to their steeper on/off switching characteristics and immunity to short channel length effects. The constant mobility is the key advantage of the core/shell system over conventional nanostructures that suffer from size-dependent mobility.

## ■ ASSOCIATED CONTENT

### Supporting Information

Further details of experimental methods and measurements. This material is available free of charge via the Internet at http://pubs.acs.org.

## ■ AUTHOR INFORMATION


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### Notes

The authors declare no competing financial interest.

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