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Heteroepitaxial Growth of Vertical GaAs Nanowires on Si (111) Substrates by Metal−Organic Chemical Vapor Deposition

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ABSTRACT

Epitaxial growth of vertical GaAs nanowires on Si (111) substrates is demonstrated by metal−organic chemical vapor deposition via a vapor−liquid−solid growth mechanism. Systematic experiments indicate that substrate pretreatment, pregrowth alloying temperature, and growth temperature are all crucial to vertical epitaxial growth. Nanowire growth rate and morphology can be well controlled by the growth temperature, the metal−organic precursor molar fraction, and the molar V/III ratio. The as-grown GaAs nanowires have a predominantly zinc-blende crystal structure along a ⟨111⟩ direction. Crystallographic {111} stacking faults found perpendicular to the growth axis could be almost eliminated via growth at high V/III ratio and low temperature. Single nanowire field effect transistors based on unintentionally doped GaAs nanowires were fabricated and found to display a strong effect of surface states on their transport properties.

III−V compound semiconductors have advantages, such as higher carrier mobilities, superior optoelectronic properties (direct band gap), and have demonstrated band gap engineering over a wide energy range, compared to the silicon, which has dominated the semiconductor industry. Direct integration of III−V semiconductors with Si could yield low-cost, high performance systems, extending mature silicon technologies to higher speed or frequency circuits, functional optoelectronic device elements, such as light-emitting sources and detectors for photonic applications, and next-generation hybrid computing. However, direct planar epitaxial growth of defect-free III−V semiconductors on Si is challenging due to lattice mismatch and significant differences in coefficient of thermal expansion.[1−3] Benefiting from their small lateral dimensions, nanowire (NW) structures can relieve the strain due to the lattice mismatch via lateral relaxation within the critical diameters[4,5] and enable high quality direct heteroepitaxy. Toward the integration of high performance III−V NW-based devices, such as light emitting devices,[6] high mobility and high frequency devices,[7−9] single electron devices,[10,11] and vertical surrounding-gate field-effect transistors (FETs),[12] with the mature Si-based technology, it is highly desired to have well-controlled NW morphology, dimension and uniformity, crystallinity, and orientation, positioning, and electric and optical properties. Recently, epitaxial growth of III−V NWs on Si substrates through the vapor−liquid−solid (VLS) growth mechanism has been reported with various qualities.[13−19] For GaAs NWs, undefined growth orientation and growth along the nonvertical ⟨111⟩ equivalent directions are common problems.[13,15] In this work, the successful epitaxial growth of vertical GaAs NWs on Si (111) substrates was demonstrated with Au colloidal nanoparticles as catalysts using metal−organic chemical vapor deposition (MOCVD) through careful control over the nucleation stage including substrate preparation, baking process, and growth temperature. The NW morphology and growth rate were systematically studied at various growth temperature and molar fractions of the reactant precursors (molar flow rate of the reactants divided by the total gas molar flow rate). The as-grown GaAs NWs have a predominant zinc-blende (ZB) crystal structure and their density of stacking faults (SF) was found to be strongly correlated to

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growth conditions. Moreover, single GaAs NW FETs were also fabricated and characterized as a preliminary assessment of their electronic transport properties.

The cleaning and treatment of Si substrates prior to NW growth is crucial for vertically epitaxial growth of GaAs NWs. The p-type Si (111) substrates were cleaned (ultrasonicate in trichlorethylene, acetone, isoproponal, and deionized water sequentially) and etched in buffered oxide etch solution (BOE, 6 parts 40% NH_4F and 1 part 49% HF). The BOE etching is important, although both BOE and HF solution can be used to remove the native oxide and form a hydrogen-terminated surface,[13] the BOE treatment was found to have higher yield of vertical NWs than the HF treatment (images not shown). It is probably due to BOE etching produces flatter Si surfaces compared to HF solution etching[20] and improves the nucleation uniformity for vertical growth. After BOE etching, the substrate surface was treated with a poly-L-lysine solution (0.1% w/v) and 40 nm diameter Au nanoparticles were deposited onto the substrate using diluted colloidal Au in water (Ted Pella Inc.). The typical nanoparticle deposition time was ~10−30 s; a reduction of the NW epitaxial quality was observed with longer deposition time (greater than 60 s) due to reformation of the SiO_2 layer upon exposure to air. No obvious effect on the NW growth was observed other than a lower overall density and uniformity without poly-L-lysine treatment, considering the previous discussions.[21,22]

The NW growth was carried out in a close-coupled showerhead MOCVD system (Thomas Swan Scientific Equipment, Ltd.), using AsH_3 (arsine) and TMG (trimethylgallium) precursors in H_2 carrier gas (total flow rate of 20 L/min) at 100 Torr chamber pressure. The substrate was first baked at high temperature (~600−700 °C) for 5−10 min and then lowered and stabilized at the designed growth temperature, which varied within the range from 388 to 488 °C. The growth was initiated by simultaneous introduction of AsH_3 and TMG to the reactor and was terminated by stopping the TMG flow. The AsH_3 flow was retained during cool down to 250 °C to suppress decomposition of the NWs. NWs grow at temperature ranging from 388 to 488 °C, however, the vertical epitaxial GaAs NWs with relatively uniform morphology were found to grow only in a narrow temperature window from 417 to 455 °C. A baking temperature of ~600−700 °C was also found to be essential for the highly aligned epitaxial growth, which maybe related to alloy formation between the Au nanoparticle and the Si substrate.[15] A possible explanation is proposed here. It is known that the Au−Si eutectic temperature for bulk materials is 363 °C with 18.6 at % Si in the alloy[23] and could be slightly shifted due to the size effect.[24] By increasing the baking temperature above the eutectic temperature the percentage of Si atoms dissolved in the Au−Si alloy particle will increase (~27−31 at % at ~600−700 °C); the higher the Si concentration in the alloy, possibly the better the alloy/Si interface quality due to Si atom precipitation from the alloyed particle during cool-down to the growth temperature (~20−22 at % at ~420−460 °C). Baking temperatures higher than this range are not suitable because, above 750 °C, the Au−Si alloy droplets start to wet with other facets and above 800 °C the Au particles evaporate and migrate quickly on the surface leaving behind silicon residue.[25,26]

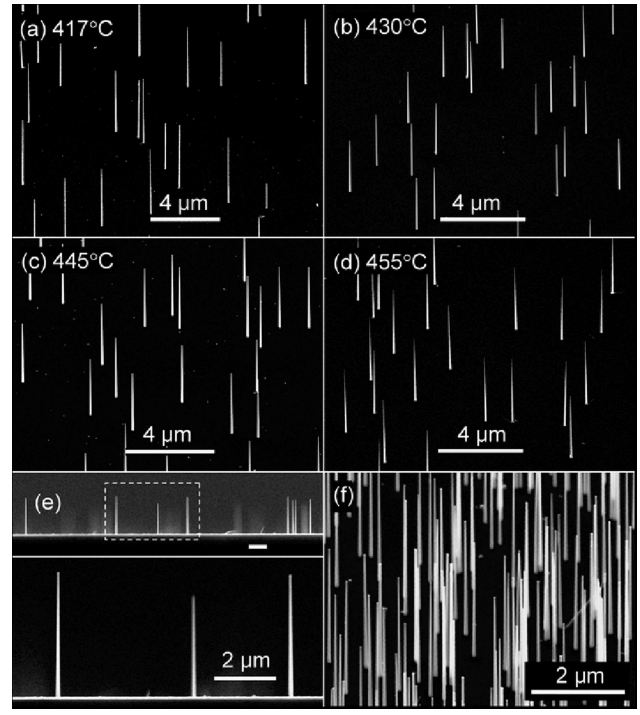

Figure 1. Tilted 45 °FE-SEM images of GaAs NWs grown vertically on Si (111) substrate at TMG and AsH_3 molar fractions of $\chi_{TMG} = 5.56 \times 10^{-5}$ and $\chi_{AsH3} = 1.38 \times 10^{-3}$, respectively, with temperatures and growth times: (a) 417 °C, 360 s, (b) 430 °C, 240 s, (c) 445 °C, 200 s, and (d) 455 °C, 240 s. (e) The upper panel shows the cross-sectional view of a cleaved sample grown at 445 °C. The high magnification image for the section marked in the dashed frame is shown in the lower panel. (f) High-density vertical epitaxial GaAs NWs on Si (111) substrate grown at 445 °C.

Figure 1 shows field-emission scanning electron microscope (FE-SEM) images of GaAs NWs on Si (111) substrates grown with optimized conditions, namely growth temperature between 417 and 455 °C and high V/III ratio (above ~20). The GaAs NWs are slightly tapered, and most of them have grown vertically on the Si substrates. The growth along nonvertical ⟨111⟩ equivalent directions[15] was rarely observed in this temperature range unless the substrate was improperly etched or baked. The proportion of vertical epitaxial NWs versus nonvertical wires was reduced if the growth temperature is either increased or decreased out of this range because of no proper nucleation between Au−Si/GaAs at lower temperatures while higher temperatures increase nonepitaxial growth. Figure 1e shows a cross-sectional view of NWs grown at 445 °C, demonstrating vertical epitaxial growth of GaAs NWs on the Si (111) substrate when the optimal growth conditions are met. A high yield of vertical epitaxial NW growth could be obtained even for large NW densities (Figure 1f) with higher concentration Au nanoparticle solution, and over large surface areas (see also Supporting Information, Figure S1).

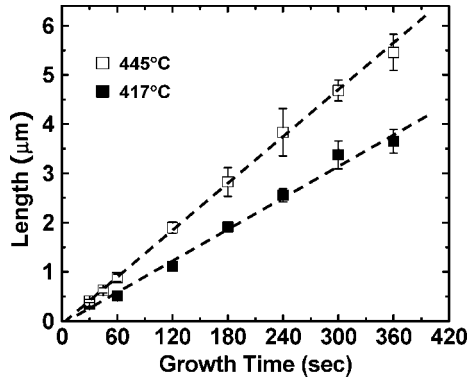

Figure 2. Plot of the NW length as a function of time for GaAs NWs grown on Si (111) substrates at 417 °C (solid squares) and 445 °C (hollow squares). The dashed lines are linear fittings to the data. AsH_3 and TMG molar fraction were 1.38×10^{-3} and 5.56×10^{-5}, respectively.

Besides the orientation, NW morphology and growth rate are also important factors for NW applications. The uniform-diameter NWs are preferred for better performance such as enhancement on the optical properties[27] and the well-controlled growth rate is important to determine the required NW length for device applications. Before detailed discussion about the dependence of NW growth rate and morphology on growth conditions, the NW growth rate was defined from the time dependent growth. The NW length was studied as a function of growth time at two different temperatures (417 and 445 °C) with fixed TMG and AsH_3, as shown in Figure 2. Each data point represents an average length of ~30−50 NWs sampled from the edge and the center areas of the substrate, and the standard deviation is plotted as the error bar. The linear dependence of NW length on growth time indicates that the growth rate is a constant for a given temperature within the growth window, up to several micrometers in length. The extrapolation of the linear fit lines intercept the time axis very close to the origin, indicating that NW growth proceeds promptly after a very short nucleation time of few seconds, which is very similar to the growth on GaAs substrates.[28] Thus, the growth rate can be simply obtained from dividing the NW length by the growth time and this also provides a simple method to precisely control the NW length.

Once epitaxial GaAs NWs are nucleated on Si substrates, the growth temperature and precursor flow rates are key parameters to the NW growth. The growth rate and morphology of the GaAs NWs were studied as a function of temperature with fixed AsH_3 and TMG molar fractions of 1.38×10^{-3} and 5.56×10^{-5}, respectively. The NW growth rate is plotted as a function of reciprocal temperature on a semilogarithmic scale in Figure 3. The NW growth rate increases with increasing temperature, peaks at ~475 °C, and decreases quickly at higher temperature. Through linear fitting of the data in the low temperature region, an activation energy E_A of ~57 kJ/mol was calculated, which is smaller than the activation energies of the Au-catalyzed GaAs NW growth on GaAs (111)B substrates from the previously reports (E_A ~ 67−75 kJ/mol)[29] and from the comparison experiments carried out in the same MOCVD system as used

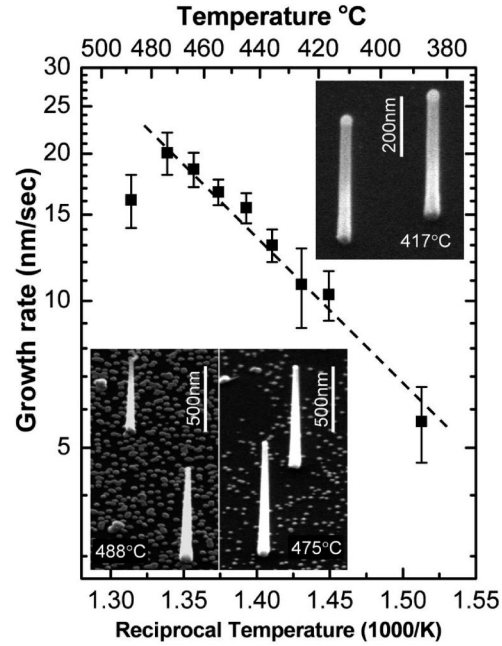

Figure 3. Temperature dependence of the growth rate and the morphology of GaAs NWs grown on Si (111) substrates at $\chi_{AsH3} = 1.38 \times 10^{-3}$ and $\chi_{TMG} = 5.56 \times 10^{-5}$. Insets are the tilted 45 °FE-SEM images of GaAs NWs grown for 60 s at 417 °C (upper right), 475 °C (lower right), and 488 °C (lower left).

here (E_A ~ 80−100 kJ/mol).[28] The presence of the Si (111) substrate seems to play an important role in lowering the activation energy for NW growth, most likely increasing the rate of pyrolysis of the precursors at low temperatures. At high temperatures, the growth rates on Si and GaAs substrates are very close where the rate of pyrolysis is near 100% already and hence the substrate effect on pyrolysis is no longer important. As shown in Figure 1 and in the insets of Figure 3, NW tapering and surface morphology changed noticeably by varying the growth temperature from 417 to 488 °C: NWs are quite uniform at low temperatures and become more tapered with increasing temperature; more apparent growth on the substrate surface and on NW sidewalls appears at high temperatures (above ~480 °C) and results in the drop of the growth rate due to the depletion of the reactants, which agrees with the previously reported results.[29,30] Therefore, relatively uniform NWs with low density surface growth can be achieved in the narrow window of growth temperatures between ~417 and 455 °C, and the lower the temperature, the more uniform the diameter and the less surface growth. The growth temperature also plays an important role for the NW crystal structure and defect density as discussed later.

TMG and AsH_3 molar fractions were found to have profound effects on the NW growth rate and morphology, studied at a fixed growth temperature of 417 °C when uniform NWs grow. At a fixed AsH_3 molar fraction of 1.38×10^{-3}, the growth rate is initially linearly dependent on the TMG molar fraction up to $\chi_{TMG} = 1.1 \times 10^{-4}$ (Figure 4a), which is with large V/III ratio and is defined as the As-rich growth region. With further increases in TMG molar fraction, the growth rate gradually departs from the linear

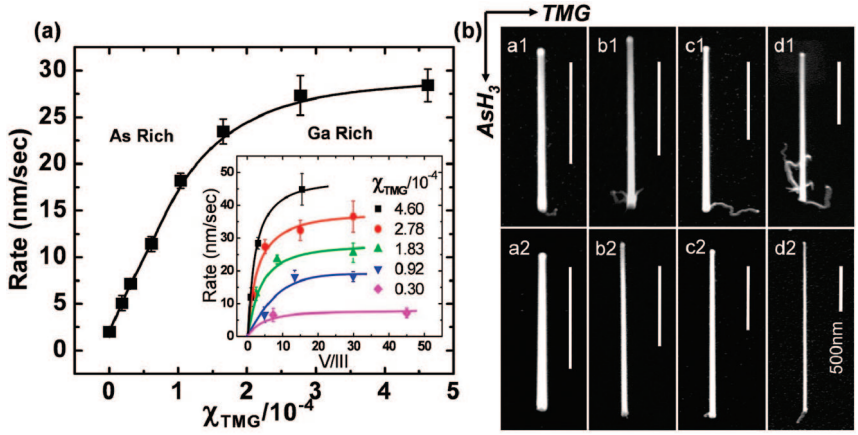

Figure 4. Dependence of NW growth rate and morphology on TMG and AsH_3 molar fractions. (a) NW growth rate as a function of TMG molar fraction with fixed $\chi_{AsH3} = 1.38 \times 10^{-3}$; the inset shows the growth rate as a function of V/III ratio for different TMG molar fractions. The continuous lines are a guide to the eye. (b) Morphology of GaAs NWs grown at 417 °C with different TMG and AsH_3 molar fractions. NWs in the first row were grown at low AsH_3 molar fraction of 1.38×10^{-3} and TMG molar fractions of (a1) 0.92×10^{-4}, (b1) 1.83×10^{-4}, (c1) 2.78×10^{-4}, and (d1) 4.60×10^{-4}; keeping the same TMG setting as used in the first row, NWs in the second row were grown with AsH_3 molar fractions of (a2) 2.80×10^{-3}, (b2) 5.60×10^{-3}, (c2) 4.20×10^{-3}, and (d2) 7.22×10^{-3}.

dependence and saturates at high molar fractions above $\chi_{TMG} = 4.5 \times 10^{-4}$ where the V/III ratio is smaller than 3 (Figure 4a) and is described as the Ga-rich growth region. The explicit dependence of the growth rate on the V/III ratio is shown in the insert of Figure 4a, where the AsH_3 molar fraction was varied while the TMG molar fraction was kept at different constant values. Independent of the TMG molar fraction, the NW growth rate tends to saturate gradually with AsH_3 molar fraction at large enough V/III ratios (above ~20), while it decreases at lower V/III ratios due to the lack of As constituents. For the same V/III ratio, NW growth rate increase with increasing TMG flow rate. As shown in Figure 4b (first row), a new "worm-like" surface growth becomes apparent by increasing TMG flow at low V/III ratios (Ga rich). This is most likely caused by Ga droplet formation and self-catalytic GaAs NW surface growth occurring in Ga-rich environments, similar to the case of InAs NWs.[31] With increased AsH_3 molar fraction, i.e., increased V/III ratio, the "worm-like" surface growth is effectively removed (Figure 4b, second row). Except for "worm-like" surface growth, TMG and AsH_3 molar fractions do not significantly affect the NW uniformity in diameter (Figure 4b). Except for "worm-like" surface growth, TMG and AsH_3 molar fraction do not significantly change the NW morphology (Figure 4b) but do affect the defect density (as shown in Figure 5) and NW growth rate. TMG and AsH_3 flow rates affect surface morphology at extreme values of the V/III ratio.

Crystal structure and uniformity of the GaAs NWs grown at different conditions were characterized using high-resolution transmission electron microscope (TEM). Figure 5 shows TEM images of NW grown at 417 and 445 °C with high (~25) and low (~3) V/III ratios. The contrast marked by the arrows in parts a, c, and d of Figure 5 are stacking faults (SFs) that are distributed randomly along the NWs. In between the SFs is high quality ZB single crystal as shown in Figure 5b. The other contrast visible is simply due to diffraction from wire bending (bend contours). The SAD patterns taken from the stacking fault free regions of the NW show the dominating crystal structure of the as-grown NWs is ZB and the NW growth is along a ⟨111⟩ direction. With a constant V/III ratio at ~25, the stacking fault linear density was dramatically reduced from ~10/μm (Figure 5a) to almost SF free (only the occasional one as shown in Figure 5d) when the growth temperature was decreased from 445 to 417 °C, indicating lower temperature results in a more uniform crystal phase. On the other hand, the SF density increased from almost SF free (Figure 5d) dramatically to ~50/μm (Figure 5c) when the V/III ratio was decreased from ~25 to ~3 with a constant AsH_3 molar fraction under the same growth temperature at 417 °C. Abundant stacking faults are commonly observed perpendicular to the ⟨111⟩ growth direction in III−V VLS grown semiconductor NWs.[32−36] While the mechanism of stacking fault formation is not yet very clear,[34,37,38] a low density of stacking faults is preferred due to the possible effects upon the optical and electronic properties from the offset between zinc-blende (ZB) and wurtzite (WZ) structures.[39] The advantage of the low growth temperature to eliminate SFs has been reported in GaAs NWs growth on ⟨111⟩ B GaAs substrates by a two-temperature growth procedure,[22] while a similar two-temperature growth procedure applied to GaP NWs grown on Si substrates (a small lattice mismatch of ~0.4%) helped improve uniformity of the NW diameters but did not remove the high density SFs,[36] which indicates the growth temperature is not the only key parameter. The low density of SFs obtained through tuning both the growth temperature and V/III ratio in the GaAs NWs grown on Si (111) substrates here is remarkable when considering the larger lattice mismatched interface (~4.1%) compared to GaP nucleation on Si.

It is very important to understand and control the key electrical properties of NWs and moreover, correlate to rational growth to implement structure design for device applcation. The electronic transport properties of the GaAs NWs grown on Si substrates were studied by single NW field effect transistors (FET) fabricated from NWs grown at 417 °C with a V/III ratio of ~25, which have the least

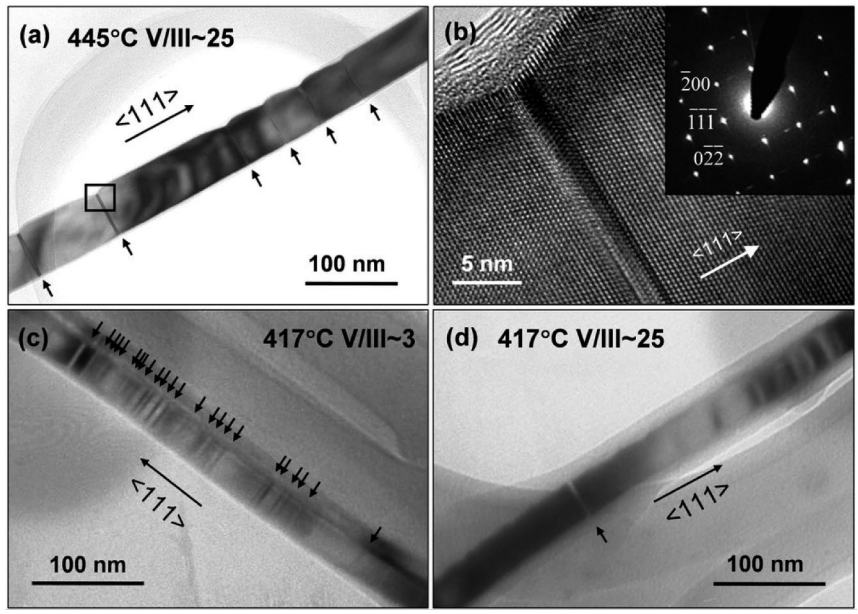

Figure 5. TEM micrographs of GaAs NW's grown at different temperature and V/III ratio with a constant $\chi_{AsH3} = 1.38 \times 10^{-3}$. Stacking faults are indicated with arrows. (a) Bright field image of a NW grown at 445 °C with V/III ~25. (b) High magnification TEM image of the region marked with a rectangle in (a). The selected area diffraction pattern (⟨011⟩ zone axis) taken from the stacking fault free segment indicates a ZB crystal structure (inset). Bright field TEM images taken from NWs grown at 417 °C with V/III ~3 and V/III ~25 are shown in (c) and (d), respectively.

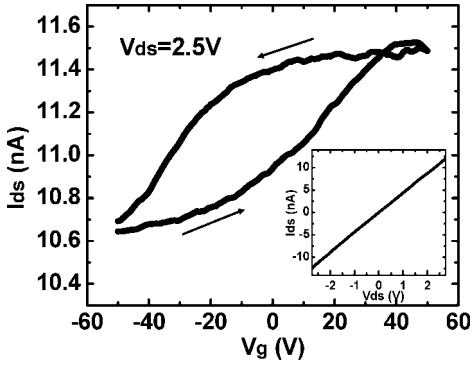

Figure 6. Transport properties of a single NW FET based on unintentionally doped GaAs NWs grown on Si (111) substrates. NWs used for devices were grown at 417 °C with $\chi_{AsH3} = 1.38 \times 10^{-3}$ and $\chi_{TMG} = 5.56 \times 10^{-5}$. The insert shows a linear $I_{ds}-V_{ds}$ curve at zero gate bias.

stacking faults (Figure 5d). The NWs were contact-transferred to the SiO_2/Si substrate, and 22 nm/45 nm/10 nm Ge/Au/Ni as source/drain electrodes were photolithographically defined, sputtered, and annealed at 420 °C in N_2 for 2 min (Supporting Information, Figure S2). The heavily doped Si substrate was used as the global back gate. The linear drain−source current versus drain−source voltage ($I_{ds}-V_{ds}$) curve shown in the inset of Figure 6 indicates the contacts to the GaAs NW are ohmic. The GaAs NWs are very resistive with weak gate modulation and large hystereses yet show a clear n-type behavior (Figure 6). The n-type behavior in unintentionally doped GaAs NWs is presumably caused by carbon background doping.[40] It is known that GaAs native oxide does not provide a favorable interface with the GaAs surface, and a high density of surface states results in a strong Fermi level pinning around the GaAs midgap at the GaAs surface.[41] The observed very low conductance indicates the GaAs nanowire could be depleted due to surface states (supported by the 2D Schrödinger−Poisson simulation shown in Supporting Information, Figure S3) and the hysteresis is due to charging and discharging the surface states.[42] NW-FET devices have also been fabricated with the NWs grown using different growth conditions (different temperature and V/III ratios, and presumably these NWs have large density of stacking faults, as shown in Figure 5) but only slight differences were observed, indicating the effects of surface states are dominating the transport properties. Furthermore, the GaAs NWs show very weak room temperature PL (not shown) due to the electron−hole recombination centers at surface. These preliminary results suggest that the influence of surface states in GaAs NW devices is more significant than that in planar devices due to the higher surface-to-volume ratio of NWs. The surface state density must be reduced in order to achieve higher performance FET devices based on GaAs NWs, which may be realized through surface passivation as used in planar devices[43,44] or formation of core−shell heterostructures.[45,46]

In summary, vertical epitaxial GaAs NWs were successfully grown on Si (111) substrates using MOCVD through strict Si substrate treatment prior to growth. The influences of growth conditions on NW morphology, growth rate, and crystal quality were also systematically studied. The GaAs NWs have predominantly ZB crystal structure in ⟨111⟩ direction with stacking faults. The growth temperature, TMG and AsH_3 molar fractions, and V/III ratio are systematically studied to understand the growth and as well to achieve the optimal growth condition for uniform GaAs NWs on Si substrate. Among the growth parameters, growth temperature has the largest effect on the NW morphology and V/III ratio has the most impact on the NW crystal structure homogene-

ity. Uniform and high quality NWs with remarkably low stacking fault densities are achievable at lower growth temperature with high V/III ratio, leading high device performance electronic and optoelectronic application. Preliminary measurements of the FET characteristics show a strong influence of surface states on the transport properties of GaAs NWs, suggesting the importance of core−shell heterostructures for III−V compound semiconductor NW device applications. The well-controlled vertical epitaxial growth of high quality single crystal GaAs NWs on Si substrate opens up significant opportunities for direct integration of functional III−V nanowire devices to Si for 3D electronics, Si photonics, and advanced hybrid computing systems.

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Supporting Information Available: Figure S1 shows a large area (100 μm × 75 μm) with vertically aligned GaAs NWs grown epitaxially on a Si (111) substrate. Figure S2 shows a SEM image of a single GaAs NW FET device. Figure S3 shows the energy band-edge profile for a 50 nm thick GaAs slab illustrating that the presence of negatively charged acceptor-type surface states, that pin E_F near midgap, lead to depletion of the NW body, even in the presence of a high n-type doping density. This material is available free of charge via the Internet at http://pubs.acs.org.

References

(1) Fang, S. F.; Adomi, K.; Iyer, S.; Morkoc, H.; Zabel, H.; Choi, C.; Otsuka, N. *J. Appl. Phys.* **1990**, *68*, R31–R58.
(2) Eisenbeiser, K.; Emrick, R.; Droopad, R.; Yu, Z.; Finder, J.; Rockwell, S.; Holmes, J.; Overgaard, C.; Ooms, W. *IEEE Electron Device Lett.* **2002**, *23*, 300–302.
(3) Ma, K.; Urata, R.; Miller, D. A. B.; Harris, J. S. *IEEE J. Quantum Electron.* **2004**, *40*, 800−804.
(4) Ertekin, E.; Greaney, P. A.; Chrzan, D. C.; Sands, T. D. *J. Appl. Phys.* **2005**, *97*, 114325.
(5) Chuang, L. C.; Moewe, M.; Chase, C.; Kobayashi, N. P.; Chang-Hasnain, C.; Crankshaw, S. *Appl. Phys. Lett.* **2007**, *90*, 043115.
(6) Gudiksen, M. S.; Lauhon, L. J.; Wang, J.; Smith, D. C.; Lieber, C. M. *Nature* **2002**, *415*, 617–620.
(7) Dayeh, S. A.; Aplin, D. P. R.; Zhou, X. T.; Yu, P. K. L.; Yu, E. T.; Wang, D. L. *Small* **2007**, *3*, 326–332.
(8) Parkinson, P.; Lloyd-Hughes, J.; Gao, Q.; Tan, H. H.; Jagadish, C.; Johnston, M. B.; Herz, L. M. *Nano Lett.* **2007**, *7*, 2162–2165.
(9) Logeeswaran, V. J.; Sarkar, A.; Islam, M. S.; Kobayashi, N. P.; Straznicky, J.; Li, X.; Wu, W.; Mathai, S.; Tan, M. R. T.; Wang, S.-Y.; Williams, R. S. *Appl. Phys. A: Mater. Sci. Process.* **2008**, *91*, 1−5.
(10) Kasai, S.; Hasegawa, H. *Physica E* **2002**, *13*, 925–929.
(11) Thelander, C.; Martensson, T.; Bjork, M. T.; Ohlsson, B. J.; Larsson, M. W.; Wallenberg, L. R.; Samuelson, L. *Appl. Phys. Lett.* **2003**, *83*, 2052–2054.
(12) Bryllert, T.; Wernersson, L. E.; Froberg, L. E.; Samuelson, L. *IEEE Electron Device Lett.* **2006**, *27*, 323–325.
(13) Martensson, T.; Svensson, C. P. T.; Wacaser, B. A.; Larsson, M. W.; Seifert, W.; Deppert, K.; Gustafsson, A.; Wallenberg, L. R.; Samuelson, L. *Nano Lett.* **2004**, *4*, 1987–1990.
(14) Watanabe, Y.; Hibino, H.; Bhunia, S.; Tateno, K.; Sekiguchi, T. *Physica E* **2004**, *24*, 133–137.
(15) Roest, A. L.; Verheijen, M. A.; Wunnicke, O.; Serafin, S.; Wondergem, H.; Bakkers, E. P. A. M. *Nanotechnology* **2006**, *17*, S271–S275.
(16) Tateno, K.; Hibino, H.; Gotoh, H.; Nakano, H. *Appl. Phys. Lett.* **2006**, *89*, 033114.
(17) Bakkers, E. P. A. M.; Borgstrom, M. T.; Verheijen, M. A. *MRS Bull.* **2007**, *32*, 117–122.
(18) Ihn, S. G.; Song, J. I.; Kim, T. W.; Leem, D. S.; Lee, T.; Lee, S. G.; Koh, E. K.; Song, K. *Nano Lett.* **2007**, *7*, 39–44.
(19) Mohseni, P. K.; Maunders, C.; Botton, G. A.; LaPierre, R. R. *Nanotechnology* **2007**, *18*, 445304.
(20) Higashi, G. S.; Becker, R. S.; Chabal, Y. J.; Becker, A. J. *Appl. Phys. Lett.* **1991**, *58*, 1656–1658.
(21) Seifert, W.; Borgström, M.; Deppert, K.; Dick, K. A.; Johansson, J.; Larsson, M. W.; Mårtensson, T.; Sköld, N.; Svensson, C. P. T.; Wacaser, B. A.; Wallenberg, L. R.; Samuelson, L. *J. Cryst. Growth* **2004**, *272*, 211–220.
(22) Joyce, H. J.; Gao, Q.; Tan, H. H.; Jagadish, C.; Kim, Y.; Zhang, X.; Guo, Y. N.; Zou, J. *Nano Lett.* **2007**, *7*, 921–926.
(23) Massalski, T. B.; Okamoto, H. *Binary Alloy Phase Diagrams*, 2 ed.; ASM International: Materials Park, OH, 1990; Vol. 1, pp 428−431.
(24) Adhikari, H.; Marshall, A. F.; Chidsey, C. E. D.; McIntyre, P. C. *Nano Lett.* **2006**, *6*, 318–323.
(25) Swiech, W.; Bauer, E.; Mundschau, M. *Surf. Sci.* **1991**, *253*, 283–296.
(26) Ressel, B.; Prince, K. C.; Heun, S.; Homma, Y. *J. Appl. Phys.* **2003**, *93*, 3886–3892.
(27) Chuang, L. C.; Moewe, M.; Crankshaw, S.; Chang-Hasnain, C. *Appl. Phys. Lett.* **2008**, *92*, 013121.
(28) Soci, C.; Bao, X.-Y.; Aplin, D. P. R.; Wang, D. *Nano Lett.* **2008**, in press. Manuscript number nl-2008-01986r.
(29) Borgstrom, M.; Deppert, K.; Samuelson, L.; Seifert, W. *J. Cryst. Growth* **2004**, *260*, 18–22.
(30) Dayeh, S. A.; Yu, E. T.; Wang, D. *Nano Lett.* **2007**, *7*, 2486–2490.
(31) Dayeh, S. A.; Yu, E. T.; Wang, D. *Small* **2007**, *3*, 1683–1687.
(32) Ohlsson, B. J.; Bjork, M. T.; Magnusson, M. H.; Deppert, K.; Samuelson, L.; Wallenberg, L. R. *Appl. Phys. Lett.* **2001**, *79*, 3335–3337.
(33) Hiruma, K.; Yazawa, M.; Katsuyama, T.; Ogawa, K.; Haraguchi, K.; Koguchi, M.; Kakibayashi, H. *J. Appl. Phys.* **1995**, *77*, 447–462.
(34) Johansson, J.; Karlsson, L. S.; Svensson, C. P. T.; Martensson, T.; Wacaser, B. A.; Deppert, K.; Samuelson, L.; Seifert, W. *Nat. Mater.* **2006**, *5*, 574–580.
(35) Bauer, J.; Gottschalch, V.; Paetzelt, H.; Wagner, G.; Fuhrmann, B.; Leipner, H. S. *J. Cryst. Growth* **2007**, *298*, 625–630.
(36) Zhang, G.; Tatenoa, K.; Sogawa, T.; Nakano, H. *J. Appl. Phys.* **2008**, *103*, 014301.
(37) Glas, F.; Harmand, J. C.; Patriarche, G. *Phys. Rev. Lett.* **2007**, *99*, 146101.
(38) Dubrovskii, V. G.; Sibirev, N. V. *Phys. Rev. B* **2008**, *77*, 035414.
(39) Murayama, M.; Nakayama, T. *Phys. Rev. B* **1994**, *49*, 4710–4724.
(40) Stringfellow, G. B., *Organometallic Vapor-Phase Epitaxy: Theory and Practice*, 2 ed.; Academic Press: San Diego, 1999.
(41) Spicer, W. E.; Lindau, I.; Skeath, P.; Su, C. Y. *J. Vac. Sci. Technol.* **1980**, *17*, 1019–1027.
(42) Dayeh, S. A.; Soci, C.; Yu, P. K. L.; Yu, E. T.; Wang, D. L. *Appl. Phys. Lett.* **2007**, *90*, 162112.
(43) Green, A. M.; Spicer, W. E. *J. Vac. Sci. Technol., A* **1993**, *11*, 1061–1069.
(44) Droopad, R.; Rajagopalan, K.; Abrokwah, J.; Zurcher, P.; Passlack, M. *Microelectron. Eng.* **2007**, *84*, 2138–2141.
(45) Titova, L. V.; Hoang, T. B.; Jackson, H. E.; Smith, L. M.; Yarrison-Rice, J. M.; Kim, Y.; Joyce, H. J.; Tan, H. H.; Jagadish, C. *Appl. Phys. Lett.* **2006**, *89*, 173126.
(46) Jiang, X. C.; Xiong, Q. H.; Nam, S.; Qian, F.; Li, Y.; Lieber, C. M. *Nano Lett.* **2007**, *7*, 3214–3218.

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