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Axial SiGe Heteronanowire Tunneling Field-Effect Transistors

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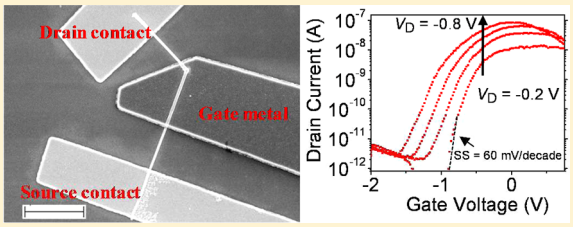
Supporting Information

ABSTRACT: We present silicon-compatible trigated *p*-Ge/*i*-Si/*n*-Si axial heteronanowire tunneling field-effect transistors (TFETs), where on-state tunneling occurs in the Ge drain section, while off-state leakage is dominated by the Si junction in the source. Our TFETs have high $I_{ON} \sim 2\ \mu A/\mu m$, fully suppressed ambipolarity, and a subthreshold slope SS ~ 140 mV/decade over 4 decades of current with lowest SS ~ 50 mV/decade. Device operation in the tunneling mode is confirmed by three-dimensional TCAD simulation. Interestingly, in addition to the TFET mode, our devices work as standard nanowire FETs with a good I_{ON}/I_{OFF} ratio when the source−drain junction is forward-biased. The improved transport in both biasing modes confirms the benefits of utilizing bandgap engineered axial nanowires for enhancing device performance.



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Modern vapor−liquid−solid (VLS) growth based on alloy catalysts has recently demonstrated the possibility of growing Si/Ge axial nanowires with controlled heterojunction abruptness,[1−3] combined with simultaneous control of both material composition (Si and Ge) and doping profile.[4] This advance opens up potential applications for electronic devices, especially for silicon-compatible tunneling field-effect transistors (TFETs). Tunneling devices can, in principle, switch more sharply and operate at lower bias than a standard FET because of their different carrier injection mechanism.[5−7] While in FETs the carriers are injected into the channel via gate-voltage V_G-controlled thermal injection from the source, in TFETs carriers are injected to the channel via band-to-band tunneling (BTBT) at the drain-channel (or source-channel) junction modulated by V_G. The high energy tail of Fermi−Dirac carrier distribution that limits the sharpness of conventional FET switching to a subthreshold swing (SS) of 60 mV/decade of current at room temperature is cut off by the bandgap in a TFET, providing the potential for sharper switching and lower SS, albeit usually over a limited range of V_G.[8,9]

Because BTBT depends on semiconductor bandgap E_G and maximum electric field E_{MAX} at the tunneling junction,[10] the Si TFET devices demonstrated to date have suffered from low I_{ON} due to the relatively large $E_G \sim 1.1$ eV bandgap of Si. Efforts have been made to fabricate Ge-based TFETs for its smaller bandgap and higher carrier mobilities, but experimentally the higher I_{ON} typically came with a compromised SS due to inferior Ge/dielectric interfaces and higher I_{OFF}.[11−13] Further, symmetric and scalable Si and Ge devices exhibit ambipolar response where tunneling can happen at either the source- or the drain-channel junction depending on V_G polarity,[14] which is undesirable for practical applications. This can be overcome either by doping or gate alignment asymmetry[11,15] or, as we report here, by compositional asymmetry in our Ge−Si hetero-nanowires (NWs). Our hetero-NW TFETs combine high $I_{ON} \sim 2\ \mu A/\mu m$ (normalized to wire diameter) with low $I_{OFF} \sim 40$ pA/μm, since tunneling happens in the Ge and Si sections of the NW in the on and off states, respectively, good trigate electrostatic control (compared to planar TFETs), an average SS of ~140 mV/decade over 4 orders of drain current I_D (with lowest SS of ~50 mV/decade), I_{ON}/I_{OFF} ratio of $\sim 10^5$, and suppression of ambipolar behavior. Three-dimensional Sentaurus TCAD as well as experimentally demonstrated ohmic contact behavior confirms that the operating mechanism is V_G-modulated BTBT current at the Ge−Si heterojunction, rather than gate-assisted Schottky barrier injection at the contact metal-Si interface as has been previously reported in axial Ge/Si hetero-NWs.[16] Finally, in addition to the TFET mode under reverse source-drain bias, our device can also operate as a conventional NW FET under forward source-drain bias, where instead of interband tunneling, V_G modulates the thermal injection barrier under the gate.

The axial *p*-Ge/*i*-Si/*n*-Si hetero-NWs were grown by the VLS method using 50 nm Au colloid nanoparticles on Ge(111) substrates in a cold-walled chemical vapor deposition (CVD) reactor and build on our growth results that demonstrated the

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first 100% composition modulated Ge/Si axial hetero-NWs.[17,18] GeH_4 (30% in H_2) and SiH_4 (50% in H_2) were used as the Ge and Si source precursors and B_2H_6 and PH_3 (both at 100 ppm in H_2) as *p*- and *n*-type dopants, respectively. The Ge(111) NW growth was initiated by nucleation at 380 °C for 3 min followed by growth at 280 °C for 30 min. Following growth of *p*-Ge segment, in situ catalyst alloying was accomplished by flowing vapor-phase trimethylgallium (TMGa) from a bubbler line for ~7 s at 380 °C. The TMGa provided a source of Ga to form a $Au_{1-x}Ga_x$ catalyst alloy in situ during growth where an increase in heterojunction abruptness has been shown with increasing Ga composition (x).[1] TMGa was then removed, and the temperature was raised to 495 °C. An *i*-Si segment was then grown for 15 min, followed by *n*-Si for 30 min. A total pressure of 2 Torr was maintained throughout the Ge growth and alloy formation, while the total pressure of 0.5 Torr was maintained for the Si growth. A significant fraction of the hetero-NWs developed a kink at the Ge/Si junction, which could be avoided by optimizing the growth conditions,[17] but actually proves helpful for prototype TFET fabrication. The wire diameter was ~55 nm, and the lengths of the *p*-Ge, *i*-Si, and *n*-Si were ~2.5, ~1.6, and ~3.4 μm, respectively. The length of each segment was estimated from the growth time and estimated growth rate of each respective segment; measurements of *p*-Ge segment after growth confirmed the estimation. Based on a previous work, the heterojunction width (i.e., the intermixed region) between the Ge and Si sections is estimated to be ~12−50 nm, of the same order as the wire diameter.[1]

After growth, the wires were dispersed on a heavily doped *p*-type silicon substrate covered by ~100 nm of thermally grown SiO_2. For TFET fabrication, hetero-NWs with a structural kink at the Ge/Si transition were preferentially chosen to precisely determine the junction position for top trigate placement. Contacts to the nanowires were made by e-beam lithography (EBL), followed by a 30 s diluted (1%) HF dip to remove the native oxide, the deposition of 100 nm of Ni metal, and lift-off. Trigate devices were fabricated by depositing 10 nm of high-κ HfO_2 at 200 °C by atomic layer deposition (ALD), followed by a second EBL step and lift-off to define the metal gate on top of the *i*-Si section with an intentional overlap over the *p*-Ge/*i*-Si junction. Finally, the samples were annealed at 350 °C for 1 min in forming gas to improve the contact resistance through GeNi and SiNi silicide formation.

To confirm rectifying behavior and determine the doping level, four-contact geometry devices were made as shown in Figure 1a (the inset shows a fabricated top-gated device). I_D−V_D measurements of the devices show good rectification with forward to reverse current ratios up to 3 orders (Figure 1b). Fitting the $I_D(V_D)$ characteristic in forward bias with ideal diode model:

$$I_D = I_0[\exp(qV_D/nkT) - 1] \quad (1)$$

we obtain an ideality factor $n \sim 3$, indicating that the dominant current-carrying mechanism in forward bias is generation and recombination.[19]

The doping type of Ge and Si sections was confirmed via backgate measurements. In this measurement a constant voltage was applied between contacts on the *p*-Ge and *n*-Si sections of the hetero-NW, with the current I monitored as a function of backgate voltage V_{BG} applied to the doped Si substrate and swept from −20 to 20 V. Transfer curves from such measurements are shown in upper inset of Figure 1b. The linear two-point I−V characteristics of the *p*-Ge and *n*-Si

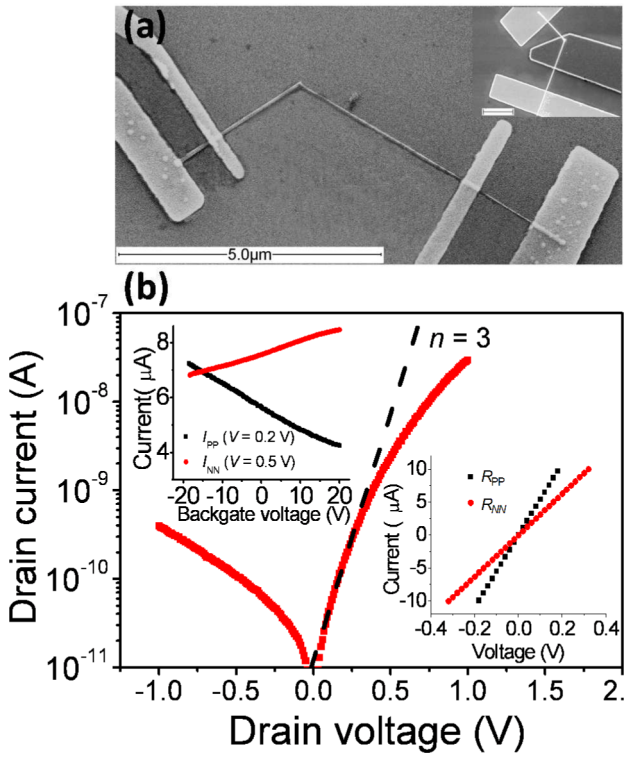

Figure 1. (a) SEM image of four-contact geometry of the kinked Ge−Si hetero-NW prior to gate metal deposition; inset shows a fabricated top-gated device (scale bar is 2 μm). (b) I_D−V_D rectification at T = 300 K, with the dashed line indicating a $n \sim 3$ ideality factor. Upper inset shows doping confirmation of *p*-Ge and *n*-Si sections via backgate V_{BG} response, lower inset showing two-point ohmic response of the *n*−*n* and *p*−*p* contacts at V_{BG} = 0 V used to infer the doping level in the *p*-Ge and *n*-Si sections.

sections at V_{BG} = 0 V, shown in Figure 1b lower inset, confirm good ohmic contacts and make it possible to estimate the doping values.[20] Taking bulk *p*-Ge and *n*-Si mobilities and an unpassivated surface state density of 5×10^{12} cm^{-2} in Ge[21] and 2×10^{12} cm^{-2} in Si,[22] we estimate *p*-and *n*-doping levels to be ~2−3 × 10^{18} cm^{-3} and ~1−2 × 10^{18} cm^{-3}, respectively, although true doping densities may be higher since the real mobility in our narrow NW materials is likely lower than in the bulk.

The operating principle of our Ge−Si hetero-NW TFETs is illustrated with the energy band diagram shown in Figure 2, calculated based on the expected composition and doping profile along the axis of our hetero-NWs.[4] In the TFET mode, Figure 2a, a negative drain voltage V_D is applied to the *p*-Ge section with respect to the grounded *n*-Si source. The gate voltage V_G modulates the intrinsic Si channel, as well as the electric field at the tunneling junction. In the off state, a negative V_G pulls the channel conduction band up, shifting the high electric field to *n*-Si source-channel junction and suppressing BTBT due to the wide bandgap of Si (see Figure 2a). Conversely, positive V_G lowers the *i*-Si channel's conduction band below the *p*-Ge valence band. The electric field at the drain-channel heterojunction, arising from a combination of V_G and V_D, promotes BTBT current from the Ge valence band in the drain to the *i*-Si conduction band, which is enhanced by the smaller Ge bandgap (see Figure 2b). The gate was positioned to extend over the *i*-Si channel into the *p*-Ge drain region (beyond the kink, see inset in Figure 1a), to

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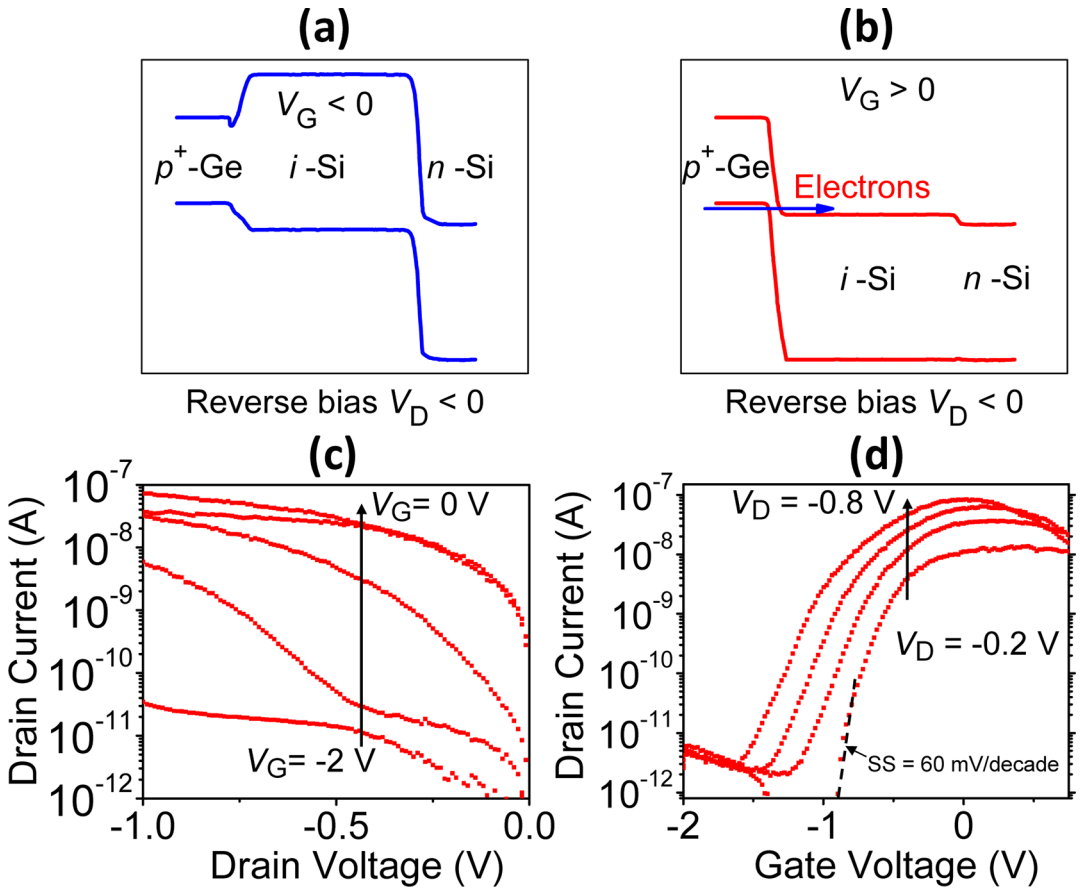

Figure 2. (a, b) Energy band diagrams of the device in TFET mode, where $V_D < 0$ and V_G modulates the tunneling current: (a) negative V_G shifts the high electric field to Si source-channel junction, where tunneling is limited, (b) positive V_G enables BTBT tunneling at the Ge−Si drain-channel heterojunction, turning on the device. (c) I_D−V_D output characteristics as a function of V_G = −2 to 0 V in 0.5 V steps, showing gate control of I_D. (d) I_D−V_G transfer characteristics at V_D = −0.2 to −0.8 V in 0.2 V steps. At V_G = 0.1 V, I_{ON} reaches ∼100 nA (∼2 μA/μm normalized to diameter). Dashed line indicates SS = 60 mV/decade.

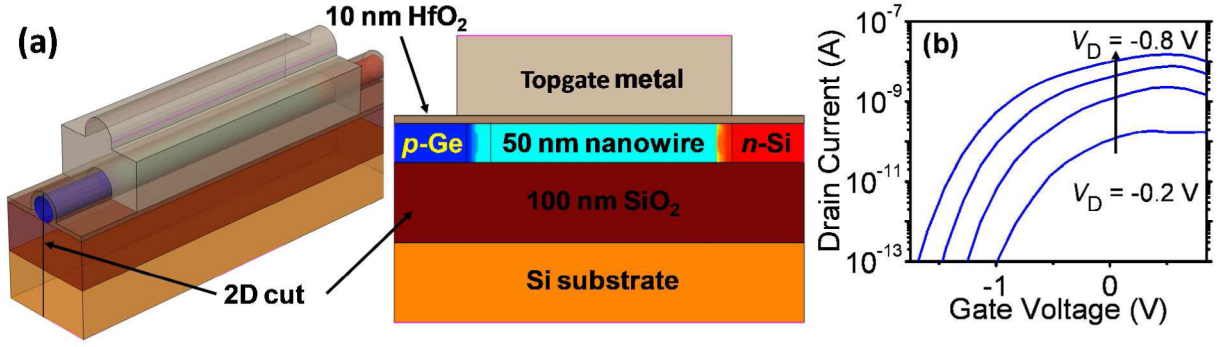

Figure 3. (a) 3D Sentaurus TCAD model and a 2D cut through the midpoint of the wire, with p-doped Ge shown as blue and n-doped Si as red, dashed line indicates the p-Ge/i-Si junction; (b) simulated I_D−V_G characteristics at V_D= −0.2 to −0.8 V in 0.2 V steps, showing good agreement with experimental data.

ensure that the maximum electric field at positive gate voltage, E_{MAX}, lies within the Ge section, maximizing tunneling current.[23] The shift in the tunneling junction between Ge and Si contributes to higher I_{ON} current and suppressed I_{OFF}.

Figure 2c shows I_D−V_D characteristics, measured from V_D = 0 to −1 V at a fixed V_G = −2 to 0 V in 0.5 V steps. At high positive V_G, the maximum electric field E_{MAX} at the tunneling heterojunction is largely determined by V_G and is only weakly dependent on V_D. At lower V_G, both V_G and V_D contribute to E_{MAX}, with I_D demonstrating nearly exponential dependence on V_D (similar to the drain-induced barrier lowering or DIBL observed in short-channel MOSFETs). Figure 2d shows the I_D−V_G transfer characteristics of our device at constant V_D = −0.2 to −0.8 V in 0.2 V steps. The maximum I_{ON} achieved in our device at V_G = 0.1 V and modest V_D = −0.8 V is ∼2 μA/μm (normalized to the wire diameter), comparable to or higher than that reported for Si-based NW,[24,25] Ge-based,[26] Ge-SiGe core−shell NW,[27] and the recently reported axial InP-GaAs hetero-NW TFET.[28] At even higher V_G > 0.1 V, I_D begins to drop, as the gate voltage begins to deplete carriers in the p-Ge

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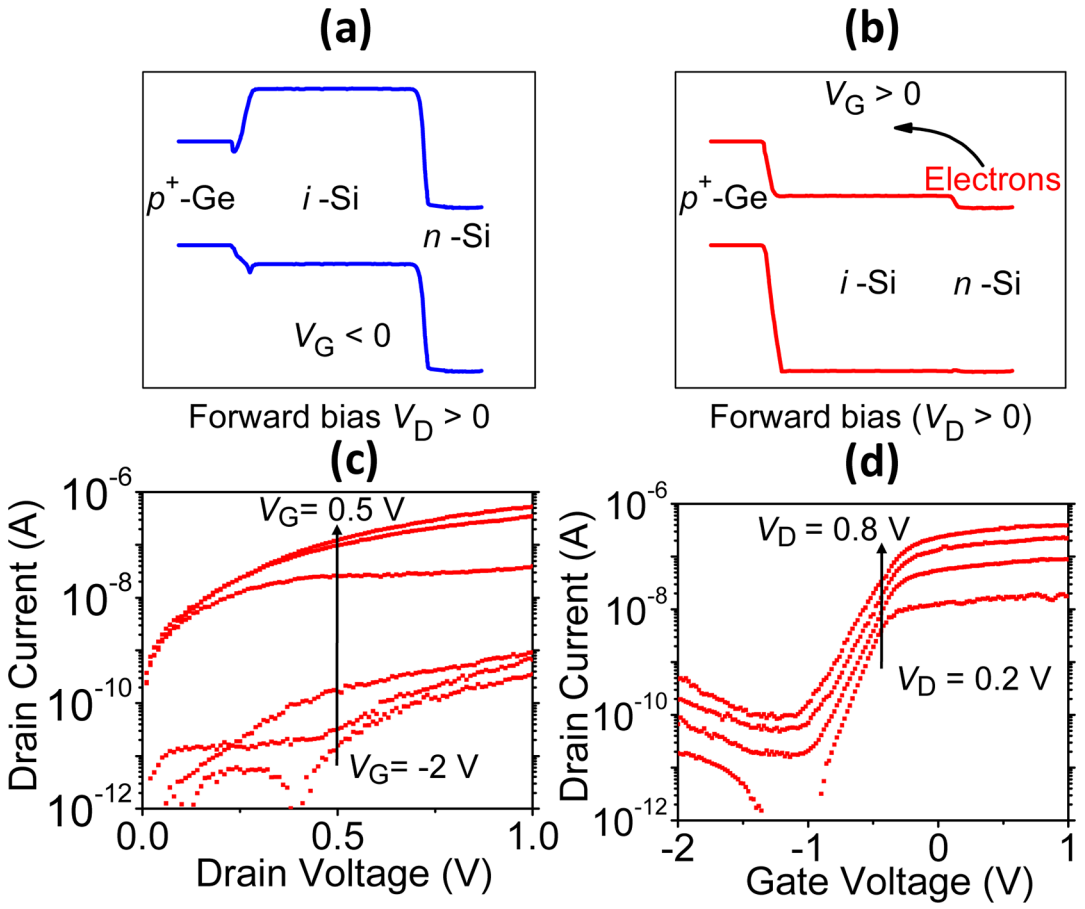

Figure 4. (a and b) Energy band diagram of the device in FET working mode where $V_D > 0$ positive and V_G modulates thermal injection of carriers: (a) negative V_G increases the *i*-Si channel barrier, preventing thermal injection of carriers into channel; (b) positive V_G lowers the *i*-Si barrier, turning on the device; (c) experimental I_D–V_D at different V_G = −2 to 0.5 V in 0.5 V steps; (d) I_D–V_G at positive V_D = 0.2 to 0.8 V in 0.2 V steps.

section resulting in lower E_{MAX} at the tunneling heterojunction. Due to our axial heterostructure, ambipolar behavior is suppressed with a very low $I_{OFF} \sim 10^{-12}$ A (corresponding to $I_{OFF} \sim 20$ pA/μm). The I_{ON}/I_{OFF} ratio of our devices is 5 decades of current, with an average subthreshold slope SS ∼ 140 mV/decade over 4 orders. The best SS, observed over the two lowest decades of I_D, is ∼50 mV/decade. Better device performance, meaning higher I_{ON} and smaller SS, could be realized by improving the heterojunction abruptness,[2] surface passivation, better electrostatic gate control (gate all-around structure, possible in a vertical layout demonstrated recently for Si TFETs[29,30]), and increased drain doping. Further, the evidence of tunneling behavior in our TFETs is self-contained, without the possibility of explaining the transfer characteristics through conventional field-effects or Schottky barrier action, given the biasing scheme depicted in Figures 2a and b and the observed SS < 60 mV/decades at low I_D.

To validate the experimentally measured results, three-dimensional (3D) TCAD simulations were performed using Synopsys Sentaurus. Figure 3a illustrates the simplified 3D structure of a nanowire TFET, comprised of a 100 nm thick and 10^{17} cm^{-3} *n*-doped Si layer, a 100 nm thick SiO_2 buried oxide, a straight cylindrical nanowire section of 50 nm diameter, a 10 nm thick HfO_2 top gate, and a nickel trigate metal. A cross-section down the midpoint of the cylindrical hetero-NW is also shown. The doping in the *p*-Ge drain and *n*-Si was taken as 5×10^{18} cm^{-3}, and the extent of the source and drain regions was taken as 150 nm. The decay of the doping into the nominally undoped *i*-Si channel (assumed to be 10^{15} cm^{-3} *p*-Si) was taken as 6 nm per decade of doping, whereas the transition between Ge and Si was taken to occur linearly over 50 nm, in reasonable agreement with experimental measurement (see S1 in the Supporting Information). We have also carried out simulations for different transition slopes (over 30–70 nm) and find that the resulting change in maximum electric field does not qualitatively change the results here.

Figure 3b represents the simulated I_D–V_G curves for the structure of Figure 3a in TFET mode. The simulations confirmed that the current conduction is due to BTBT in the region around the SiGe transition region near the *p*-Ge drain boundary. The rate of BTBT was determined using dynamic nonlocal tunneling model, where the tunneling path is dynamically updated in each iteration to align with the gradient of the potential, crossing the bandgap from the conduction band into the valence band. Since it is known that high-κ dielectric/semiconductor interface has a high trap density,[31] we assumed a positive fixed oxide charge of the density of 1.5×10^{13} cm^{-2} at the high-κ dielectric/SiGe interface, which effectively shifted the threshold voltage by ∼1.5 V, similar to our experiment. The tunneling reduced mass for Ge, which is a fitting parameter of the BTBT model, was modified from the default value of $m_r = 0.017m_0$ to $0.01m_0$.[32] With these assumptions, the simulation results in Figure 3b are in reasonable quantitative agreement with the data in Figure 2d, matching the experimentally measured I_{ON} values and subthreshold slopes, as well as the I_{ON}/I_{OFF} ratio of ∼10^5,

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and reproducing the saturation and turnover of I_D as V_G approaches 0.5 V, although the effect of V_D on I_D is somewhat larger in the simulated results.

The benefits derived from bandgap engineering along the length of our hetero-NW device architecture not only apply to TFETs but also can be used for adding a built-in electric field in the channel of a conventional MOSFET, due to the Ge/Si ~ 0.6 eV valence band offset. This effect is shown here by operating our device in forward bias mode, where a positive V_D is applied to the *p*-Ge drain with respect to the *n*-Si source, and V_G controls the thermal injection of carriers into the channel. The energy band diagrams corresponding to this bias configuration are shown in Figure 4a and b. Because of the difference between Ge and Si bandgaps, a negative V_G can push the conduction band of the *i*-Si channel above the conduction band of *p*-Ge drain, creating a barrier that effectively shuts down the thermal diffusion of electrons from the *n*-Si source to the *p*-Ge drain (Figure 4a). Conversely, a positive V_G pulls the *i*-Si channel conduction band down below that of *p*-Ge drain, enabling carriers to freely diffuse from the source to the drain when a positive V_D is applied (Figure 4b). This operating mode is experimentally verified in measurements shown in Figure 4c and d. In Figure 4c, I_D-V_D is shown as a function of V_G in the −2 to 0.5 V range, whereas Figure 4d plots the I_D-V_G transfer characteristic as a function of V_D = 0.2 to 0.8 V in 0.2 V steps. The device performance in this mode is, in fact, slightly less impressive than the TFET mode, with SS ~ 150 mV/decade and I_{ON} reaching ~0.5 μA (corresponding to ~10 μA/μm normalized to wire diameter). The higher I_{ON} in this operating mode is expected due to the fact that this mode requires no tunneling across a barrier for charge carriers to be emitted from the source to the channel, and transport is governed by drift-diffusion from the source to the drain. However, this mode of operation is fundamentally limited to SS of 60 mV/decade, whereas the TFET mode can overcome this diffusion-based limit.[6,7]

In conclusion, we have demonstrated the successful growth, fabrication, and characterization of axial *p*-Ge/*i*-Si/*n*-Si hetero-NW TFET. Our hetero-NWs were realized using the VLS method with better abruptness of axial modulation of doping and composition compared to earlier reports on NW TFETs. The trigated devices show good performance with I_{ON} of up to ~2 μA/μm (normalized to the wire diameter) with suppressed ambipolar behavior and average SS of ~140 mV/decade (SS ~ 50 mV/decade over the lowest two decades of I_D), with a potential for further improvement. A 3D Sentaurus TCAD model simulation confirms the device working principle based on band-to-band tunneling at the heterojunction. Due to the Ge−Si heterojunction, our device can also operate as nanowire FET with improved transport characteristics at forward source-drain bias, with no interband tunneling.

■ ASSOCIATED CONTENT

Supporting Information

SiGe composition profiles, obtained from atom probe tomography (APT) analysis. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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