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Field Dependent Transport Properties in InAs Nanowire Field Effect Transistors

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ABSTRACT

We present detailed studies of the field dependent transport properties of InAs nanowire field-effect transistors. Transconductance dependence on both vertical and lateral fields is discussed. Velocity-field plots are constructed from a large set of output and transfer curves that show negative differential conductance behavior and marked mobility degradation at high injection fields. Two dimensional electrothermal simulations at current densities similar to those measured in the InAs NWFET devices indicate that a significant temperature rise occurs in the channel due to enhanced phonon scattering that leads to the observed mobility degradation. Scanning transmission electron microscopy measurements on devices operated at high current densities reveal arsenic vaporization and crystal deformation in the subject nanowires.

The high electron mobility demonstrated recently in InAs nanowire field-effect transistors (NWFETs)[1] highlights the potential of such nanoscale devices for high performance electronic applications. Indeed, back-gate,[2,3] top-gate,[4] and wrap-gate[5] InAs based NWFETs have been already realized, and their low field transport properties have been reported. However, the vertical (gate—channel) and lateral (source—drain) field dependent transport properties in NWs and the consequences of high injection fields on device performance and morphology have not been fully explored. In this paper, we present detailed studies on the field dependent transport properties of InAs NWFETs and highlight the effects of high injection fields on their transport behavior from current—voltage ($I-V$), transmission electron microscope (TEM), and scanning TEM (STEM) characterization and support our experimental observations and analysis with two-dimensional (2D) electrothermal simulations.

The InAs NWs used in this study were grown by metal organic chemical vapor deposition on thermal SiO_2/Si substrates at a growth temperature of 350 °C and a V/III ratio (AsH_3/TMIn input molar ratio) of 10.[6,7] E-beam lithography was utilized to fabricate top-gate NWFETs from these NWs on 600 nm SiO_2/n^+-Si with a 73 nm ZrO_2/Y_2O_3 top-gate dielectric and 100 nm Al top gate.[1] Ti/Al (15 nm/85 nm) layers were then used to fabricate ohmic contacts. We have observed negative differential conductance in NWFETs fabricated from these NWs as well as from NWs grown on InAs(111)B substrates, and in this letter we will discuss in detail the field dependent transport properties of top-gate InAs NWFETs.

Figure 1a shows a representative field-emission scanning electron microscope (FESEM) image of a top-gate NWFET device and the corresponding equivalent DC circuit diagram.[4] Only the NW segment directly under the gate, of length $L_G < L_{SD}$, where L_{SD} is the source drain length, is considered to be the active portion of the NWFET device. Top-gated devices with extension regions are favored over devices with a gate overlapping the source/drain contacts to eliminate gate leakage currents when operating the devices at high fields, as well as to improve their breakdown characteristics. However, the series resistances, R_{s1}, associated with the drain contact plus extension region, and the source counterpart, R_{s2}, dominate the measured $I-V$ characteristics shown in Figure 1b for the following reasons: (i) the linear $I-V$ relation of the series resistances prevents observation of saturation in the output curves at high V_{DS}, and (ii) the source series resistance reduces the gate transconductance.[9] The gate transconductance is also decreased due to the presence of trap states at the dielectric—InAs interface, which introduce an additional capacitance that reduces the gate field and prevent full depletion of the InAs NWFET channel.[1] Thus, high off-current values are expected. The unmodulated portion of the NW channel under the gate can be modeled as a leakage resistance, R_{leak}, obtained from the lowest measured I_{DS} at sufficiently negative V_{GS}. By considering the potential drops across the series resistances as well as

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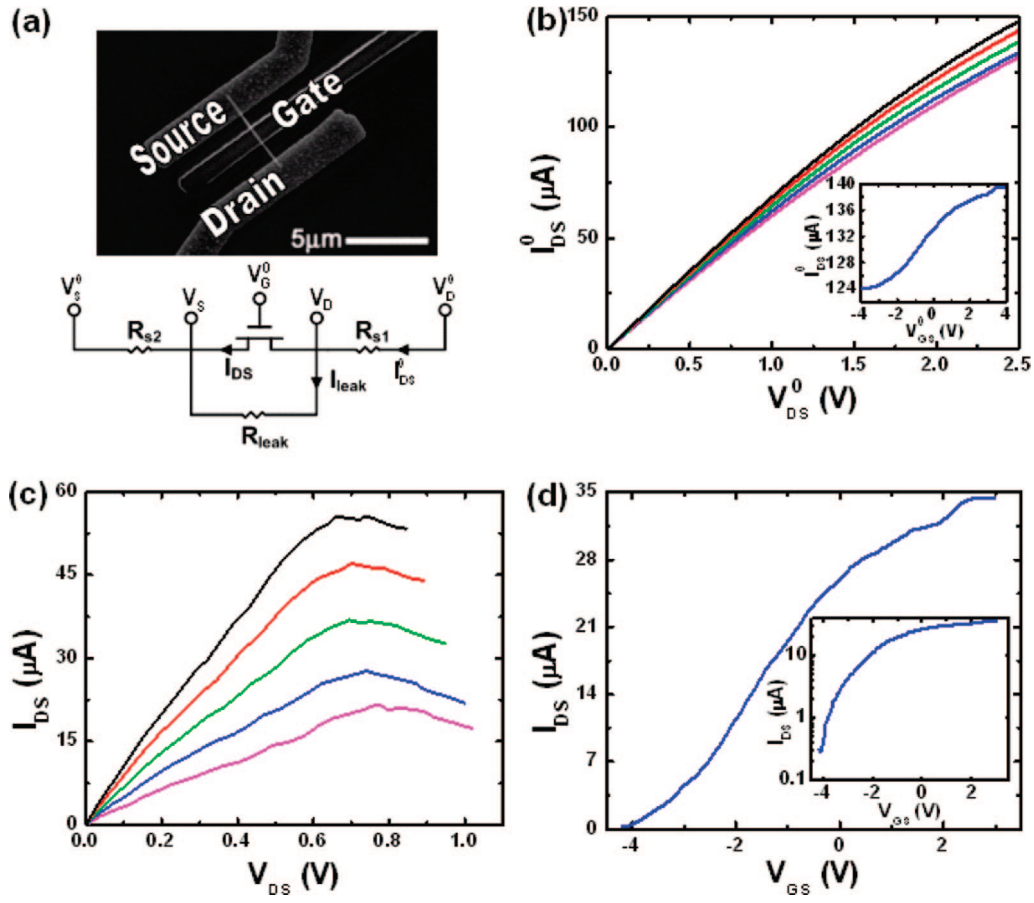

Figure 1. (a) FESEM image of a top-gate InAs NWFET and its corresponding DC equivalent circuit. (b) Measured output curves of an InAs NWFET device ($D = 90$ nm, $L_G = 0.97$ μm, $L_{SD} = 3.57$ μm). Inset is the measured transfer curve for the same device. (c) Extracted output curves. (d) Transfer curves from (b) by taking into account series and leakage resistances. Inset is the extracted transfer curve plotted in logarithmic scale.

the leakage resistance,[4] we are able to assess and extract the output and transfer curves inherent to the transport properties of the NW segment directly under the gate (see Supporting Information), as shown in Figures 1c and 2d. Note that (i) a substantial voltage drop is associated with the source and drain segments, and the potential drop corresponding to the NW segment directly under the gate is only 30−45% of the applied voltage, the magnitude of which also depends on the gate voltage bias, and (ii) for V_{DS} larger than 0.7−0.8 V, there is a decrease in current as V_{DS} is increased, i.e., negative differential conductance (NDC). We have also observed NDC in NWs grown on InAs(111)B substrates.

Transfer curves are typically used to extract the dependence of the transconductance and mobility on gate voltage, as shown in Figure 2a, where the field-effect mobility ($\mu_{FE} = g_m L_G^2/CV_{DS}$) is plotted for $V_{GS} \geq -1.9$ V, which corresponds to the linear operating regime. Here, g_m is the intrinsic transconductance, V_{DS} is the voltage drop across L_G, and C is the gate capacitance, which is equal to the oxide capacitance in the linear regime.[10,11] Note that at both positive and negative gate voltages, the field-effect mobility is low and increases as V_{GS} approaches the flat band voltage, V_{fb},[12] which is typically less than 0 V due to the presence of positively charged donor-type surface states[13] that shift V_{fb} to negative values. The $\mu_{FE}-V_{GS}$ dependence shown in Figure 2a follows the same trends as those observed in metal-oxide-semiconductor FETs[14] and heterojunction FETs.[15] For positive voltages in the accumulation regime, μ_{FE} decreases due to surface roughness scattering.[14,16] For negative gate voltages below V_{fb} in the depletion regime, Coulomb scattering due to fixed oxide charges, interface state charges, and ionized impurity charges reduces μ_{FE}.[17] Coulomb scattering is dominant at low carrier densities and is reduced at higher densities due to screening of the charged centers' potential. The $\mu_{FE}-V_{GS}$ dependence is typically asymmetric, with fast roll-off at voltages close to the threshold voltage.[14,15] For the InAs NWFETs, however, the large surface state density[1] leads to poor subthreshold characteristics and to the more symmetric appearance of the $\mu_{FE}-V_{GS}$ curve as shown in Figure 2a.

The transconductance and μ_{FE} are functions of both vertical and lateral fields.[10] To reveal both field effects, we have constructed a 2D plot of the transconductance as a function of both V_{GS} and V_{DS}. Figure 2b shows such an extrinsic transconductance map obtained from several $I_{DS}-V_{GS}$ curves measured for V_{DS} in the range of 0−2.5 V. The vertical gate field dependence in this case is similar to that of Figure 2a, where the extrinsic transconductance increases as V_{GS} approaches V_{fb}. However, as the lateral (source−drain) field is increased, we observe that the extrinsic transconductance

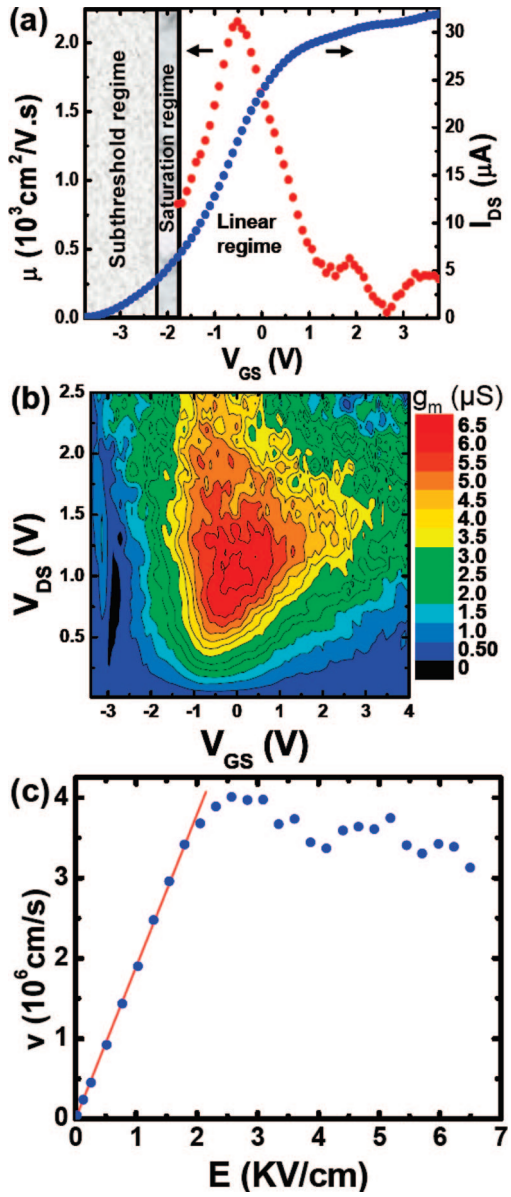

Figure 2. (a) Plot of the extracted transfer curve and field-effect mobility $\mu_{FE}(V_{GS})$ of an InAs NWFET ($D = 72$ nm, $L_G = 1$ μm, and $L_{SD} = 3.35$ μm) at $V_{DS} = 0.5$ V. (b) Contour plot of the extrinsic transconductance measured with V_{GS} sweep for different applied V_{DS} from the device in Figure 2. (c) Velocity-field plot for same device in Figure 1 extracted from several transfer and output curves.

increases linearly and peaks at some lateral field value, beyond which transconductance degradation takes place at a rate slower than that with the vertical field, which, to our best knowledge, has not been discussed in earlier NWFET transport studies. Reduction of the transconductance at high lateral fields explains the decrease in current in the extracted output curves of Figure 1b.

To assess the lateral field dependence of the transport behavior, we extract the electric field across the NW portion under the gate by taking into account the underlap and contact series resistances, R_{s1} and R_{s2}, and the leakage resistance, R_{leak}.[4] R_{s1}, R_{s2}, and R_{leak} are dependent on V_{DS}, and their values are extracted for each V_{DS} biasing voltage and used in the subsequent field, velocity and mobility calculations (R_s varies in the range of 10.3−14 KΩ and R_{leak} in the range of 2.5−7 KΩ).[4] In the linear operating regime, the drift velocity v can be calculated according to (See Supporting Information)

$$v = \frac{I^0_{DS}(1 + (R_{s1} + R_{s2})/R_{leak}) - V^0_{DS}/R_{leak}}{C(V^0_{GS} - V_T)/L_G - CI^0_{DS}R_{s2}/L_G} \quad (1)$$

If the series and leakage resistances are not taken into account, eq 1 simplifies to

$$v = \frac{I^0_{DS}}{C(V^0_{GS} - V_T)/L_G} \quad (2)$$

Equation 2 is typically used to obtain the field-effect mobility, $\mu_{FE} = g^0_m L^2_G/CV_{DS}$, at small V_{DS} in NW and carbon nanotube transistors[18] by assuming $v = \mu_{FE}E$, with $E = V_{DS}/L_G$ being the lateral electric field and $g^0_m = \partial I^0_{DS}/\partial V^0_{GS}|_{V_{DS}=cst}$ the extrinsic transconductance. To extract the lateral field dependent velocity, the transfer curves are measured for V^0_{DS} values in the range of 0−2.5 V, and v is then calculated at $V^0_{GS} = 0$ V using eq 1. The computed velocity values are plotted in Figure 2c as function of lateral electric field. At low fields, the slope of the velocity field plot is the low field effective mobility, which is typically calculated from the conductance[14] as in eq 1 rather than the transconductance and maintains a constant value of $\sim\mu_{eff} = 1900$ cm^2/V•s for $0 \le E \le 1.5$ KV/cm. The drift velocity increases as the lateral field increases and reaches a peak velocity $v_{peak} \approx 4 \times 10^6$ cm/s, which is lower than that of bulk InAs ($\sim 4 \times 10^7$ cm/s).[19] For $E \ge 2.7$ KV/cm, the extracted carrier velocity decreases with further increase in the applied lateral field as shown in Figure 2c. The NDC behavior is consistent in the velocity-field plots computed for several V^0_{GS} values (see Supporting Information, Figure S1) and have been obtained from several devices fabricated separately on similar InAs NWs.

Negative differential conductance and reduction of carrier velocity at high fields can arise for a number of reasons. First, intervalley scattering from the low-effective-mass direct conduction band minimum (Γ) to higher effective mass, higher valley/ band minima (X or L) may lead to NDC.[8] However, InAs has the largest energy separation between the conduction band minima among all high mobility III−V materials ($E_{\Gamma L} = 0.73$ eV and $E_{\Gamma X} = 1.02$ eV), resulting in minimal intervalley scattering. Second, intravalley or inter-subband scattering where electrons lose momentum when scattered from one energy subband with high momentum to another equivalent energy subband with lower momentum may lead to NDC.[9] This can be important in one-dimensional nanostructures where energy subbands are quantized and equivalent-energy transitions are associated with larger momentum differences. Third, nonparabolicity in the energy-momentum band diagrams may lead to NDC, where electrons with high energy encounter increased effective mass and reduced momentum relaxation time, both of which reduce the electron mobility.[19,20] This effect is pronounced for small bandgap materials such as InAs. Fourth, enhanced phonon scattering and momentum relaxation to the lattice where the relaxation time is effectively reduced at high injection fields and may lead to NDC. Although little theoretical work has been done on NDC in low dimensional semiconductors,

nonparabolicity in the energy-momentum band diagrams[21] and more recently hot phonon distribution were suggested to dominate the NDC in carbon nanotubes.[22] While pulsed current−voltage characteristics could be used to eliminate heating effects,[19] these techniques are not readily available for NWs due to the large parasitic impedances that impose constraints on such fast pulsing procedures.[2] We show next through 2D electrothermal simulations and STEM analysis on two-terminal InAs devices that thermal heating during normal device operating procedures is a dominant process that leads to the observed negative differential conductance behavior.

We first consider the case of a 90 nm thick InAs slab atop SiO_2/Si with Ti/Al top contact electrodes and dielectric passivation with Al top-gate similar to the actual device structure over which the negative differential conductance has been measured (Figures 1 and 2). The electrothermal properties for this structure is simulated in Silvaco-Atlas by taking into account a 350 μm thick Si substrate and 200 μm extension of the contact electrodes and substrate around the NWFET device. The entire device structure is shown in Figure S2 of Supporting Information. To calibrate the measured current density to that of the simulated one, a contact resistance value of 350 Ω per electrode and a mobility value of 16000 cm^2/V•s were found to give the best fit after several alterations. Both of these values are in good agreement with our extracted data from similar devices.[1] Extracted mobility values from NWFET measurements are apparent values that are influenced by the interface state capacitance and can vary with V_{GS} sweep rate, which determines the charge balance between carrier capture and emission from interface states.[1] Slow V_{GS} sweep rates have resulted in reduced hysteresis and high mobility values of 16000 cm^2/V•s, which are believed to be the actual carrier mobility values in the channel.[1] For the carrier concentration, we have used a bulk concentration of 5×10^{16} cm^{-3} and a positive fixed charge density of 2.7×10^{12} cm^{-2}. These were used in a Schrödinger−Poisson solver to fit experimental values of carrier concentration for NWs with diameters in the range of 70−120 nm and resulted in an average carrier concentration of $\sim 8 \times 10^{17}$ cm^{-3} (both measured and simulated) for a 90 nm InAs NW at $V_{GS} = 0$ V and constant $V_{DS} = 0.15$ V.[23] Figure 3a shows excellent agreement between the measured and simulated current density using these input device parameters. This agreement between simulated and extracted values of contact resistance and mobility validates our extraction procedure and highlights the ability to form low resistance ohmic contacts and obtain decent mobility values in excess of 10^3 cm^2/V•s from InAs NWs as demonstrated by us[1] as well as by other research groups.[2,5]

Figure 3b shows a contour plot of the temperature profile across the active portion of the device when biased at $V_{DS} = 2.5$ V, resulting in a current density of 2.3×10^6 A/cm^{-2} and a peak temperature of 506 K. This is a significant increase in the device temperature that leads to enhanced phonon scattering and mobility degradation. Indeed, such an increase of ~200 K above room temperature leads to a

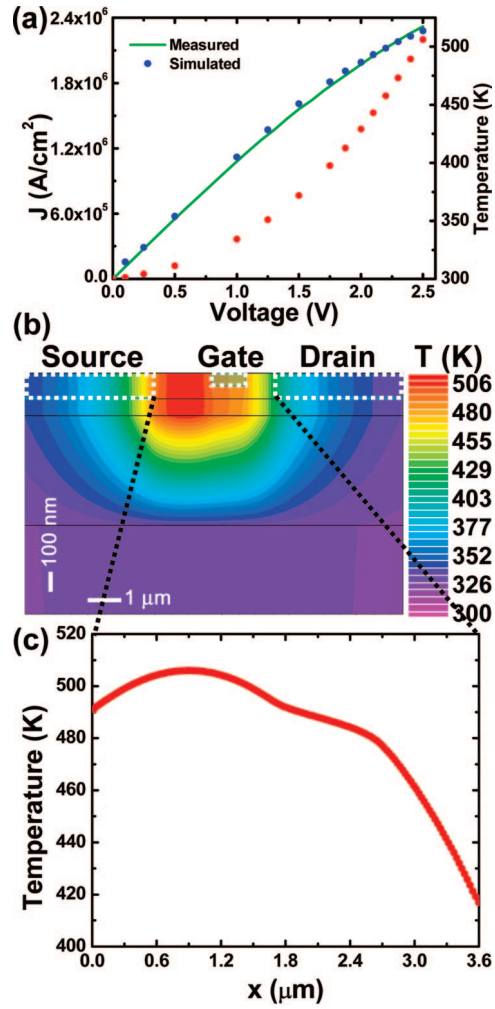

Figure 3. (a) Measured and simulated current density for a material stack similar to that of the device considered in Figures 1 and 2 ($V_{GS} = 4$ V) along with the maximum temperature in the channel. Excellent agreement between the measured and simulated J is obtained for $R_c = 700$ Ω and $\mu = 16000$ cm^2/V•s. (b) Contour plot of the lattice temperature and (c) line cut profile across the center of the channel starting at the source electrode ($x = 0$), obtained from 2D Silvaco-Atlas electrothermal simulations by considering the same device material stack as that of Figures 1 and 2.

mobility degradation by a factor of ~2 for carriers in InAs bulk with (100) surfaces.[24] Figure 3c shows a line cut of the temperature profile across the channel length of the device starting at the source electrode ($x = 0$) and ending at the drain electrode ($x = 3.6$ μm). The hottest regions in the channel where the temperature exceeds 500 K are located near the source electrode within a distance of ~250 nm. This distance is of the order of the electron mean free path in our InAs NW and is consistent with length scales over which a constant resistance in InAs NWs has been measured.[23] Following the ~250 nm region, over which ballistic transport have been observed,[25] onset of phonon scattering in the diffusive NW regions is expected to prevail. Electrothermal simulations at different V_{DS} biases show power-law increase of temperature as a function of current density as shown in Figure 3a with peak temperatures near the source electrode.

We have also used transmission electron microscopy (TEM) and scanning TEM (STEM) on two-terminal InAs

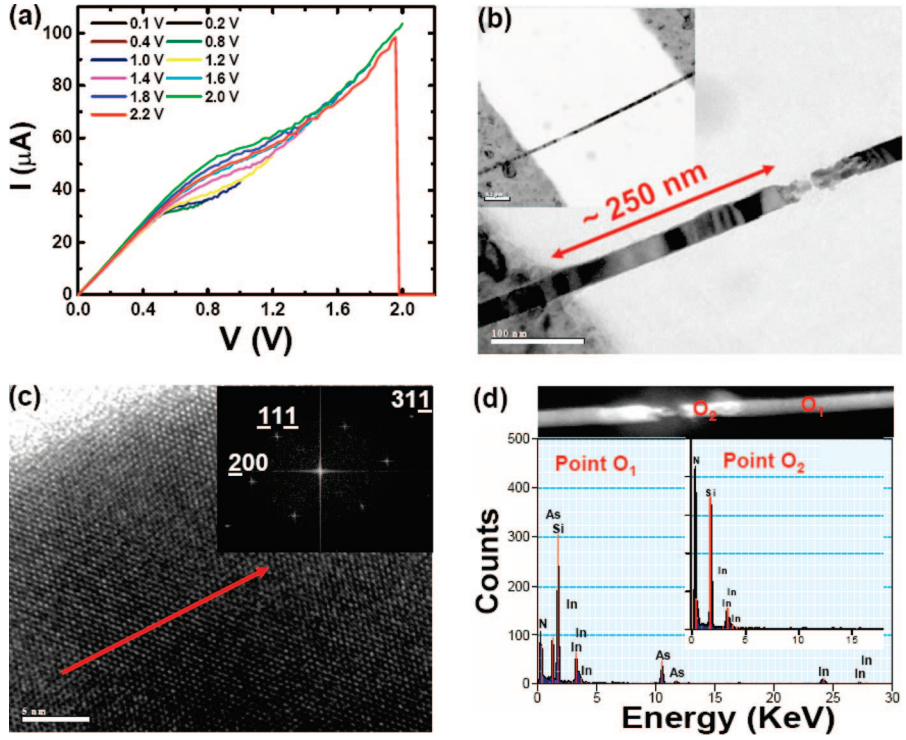

Figure 4. (a) Current−voltage characteristics of a two-terminal InAs NW device fabricated on a 100 nm Si_3N_4 TEM grid when biased up to different voltage biases. (b) TEM bright field image of the same device in (a) after performing the $I-V$ measurement. Scale bar is 100 nm. Inset scale bar is 200 nm. (c) HRTEM of the same NW away from the breakage region and inset is the correspondent diffraction pattern showing growth in the ⟨31$\underline{1}$⟩ orientation. Scale bar is 5 nm. (d) Dark field scanning TEM image of the same device in (b). EDX analysis shown below was obtained at point O_1 (away from the breakage region), and at point O_2 (directly at the breakage region), showing absence of As at the breakage region.

NW devices fabricated on a 100 nm Si_3N_4 suspended membrane, suitable for TEM study, to observe morphological changes to the InAs NWs when exposed to high current densities. Figure 4a shows $I-V$ characteristics of an InAs NW device (D = 33 nm, L_{SD} = 1.5 μm) up to different V_{DS} stresses. It can be noted from Figure 4a that for the last V_{DS} stress bias of 2.2 V, the current values are lower than those of the previous stress voltage of 2.0 V, after which the current drops to zero at 1.98 V. The current density at which the NW breaks is $\sim 10^7$ A/cm^2. It is noteworthy that when normalized to the NW diameter, the current capacity of this InAs NW device is 3 A/mm and exceeds that of the highest ever reported value in any III−V channel material including that of the recent InGaAs MOSFET (1.05 A/mm).[26] This is despite the unoptimized device geometry and the lower heat dissipation in our device that was fabricated on a 100 nm Si_3N_4 membrane suspended in air. Figure 4b shows TEM images of the two-terminal InAs NW device used for this TEM study. It can be seen clearly that the discontinuity in the InAs NW device occurs at ~250 nm distance from the source electrode, which is consistent with the simulations above and experimental measurements of the mean-free path in a similar InAs NW.[25] Figure 4c shows a high resolution TEM (HRTEM) image of a section of the InAs NW used for this measurement and the corresponding diffraction pattern of the image showing a single crystalline zincblende structure with a ⟨31$\underline{1}$⟩ growth orientation. Figure S4 of the Supporting Information shows HRTEM images of the InAs NW device under consideration taken at the discontinuity region and showing transition from polycrystalline to single crystalline regions as the distance from the discontinuous region toward the source electrode increases.

STEM analysis on the same two-terminal InAs NW device has been performed. Figure 4d shows a dark-field scanning image of the device with marked points (O_1 and O_2) from which energy dispersive X-ray (EDX) analysis spectra were obtained. Both In and As peaks appear in the EDX spectrum of the NW region at point O_1 away from the breakage area. However, only In (in addition to Si and N from the nitride membrane) was detected at point O_2 of the NW region in close proximity to the breakage region. This suggests that upon exposure of the NW to high current density, the local heating in the NW at ~250−300 nm away from the source region leads to As out-diffusion and vaporization from surface, leaving In behind. The molten In left behind, which has a melting temperature of ~156.6 °C and a lattice constant of 4.59 Å,[27] freezes and shrinks in size, forming a discontinuity in the NW at the decomposed region as can be seen in Figure 4b. The change of morphology at the breaking point is clearly seen from the HRTEM images in Figure S4, Supporting Information. Note that this situation represents the extreme scenario where physical breakdown in the NW occurs. At slightly lower current densities than are required for breakage, we anticipate that local heating causes similar decomposition or irreversible morphological changes to the NW leading to a total reduction in the NW current. This situation is observed in Figure 4a where the current−voltage characteristics show a lower slope (increased resistance)

when comparing the measurement up to 2.0 V (where the NW is exposed to high current density) to that of up to 2.2 V just before it breaks. Measurements on similar two-terminal devices have shown that these high current values cannot be recovered after such high current density exposure, consistent with permanent morphological changes to the NW and the irreversible negative differential conductance observed.

In summary, we have studied the dependence of transport properties of top-gate InAs NWFETs on vertical and lateral fields and discussed transconductance degradation as a function of both fields. Negative differential conductance was observed in the measured and the extracted output curves and velocity−field plots from top-gate NWFETs. High injection fields induce morphological degradation to the NW due to heating effects and irreversible mobility degradation that were illustrated using TEM and STEM analysis. 2D electrothermal simulations were used to highlight the temperature increase in the InAs NWFET devices that leads to enhanced phonon scattering and reduced mobilities. These results also suggest that thermal conductivity and thermal management are important issues in realizing the full potential of nanowire-based devices.

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Supporting Information Available: Model for extracting carrier velocity, device structure for electrothermal simulations, TEM structural analysis of the two-terminal InAs NW device, thermo-electric simulations of a two-terminal device structure. This material is available free of charge via the Internet at http://pubs.acs.org.

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