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TOPICAL REVIEW

Electron transport in indium arsenide nanowires

Shadi A Dayeh

Los Alamos National Laboratory, Center for Integrated Nanotechnologies, Los Alamos, NM 87545 USA

E-mail: shadi@lanl.gov

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Abstract

The vapor–liquid–solid growth of semiconductor nanowires led to the implementation of engineered electronic and optoelectronic one-dimensional nanostructures with outstanding promise for device applications. To realize this promise, detailed understanding and control over their growth, crystal structure, and transport properties and their combined impact on device performance is vital. Here, we review our work on electron transport in InAs nanowires in a variety of device schemes. First, we provide a brief introduction and historical perspective on growth and transport studies in InAs NWs. Second, we discuss and present experimental measurements of ballistic transport in InAs nanowires over ∼200 nm length scale, which indicates a large electron mean free path and correlates with the high electron mobility measured on similar nanowires. Third, we devise a device model that enables accurate estimation of transport coefficients from field-effect transistor measurements by taking into account patristic device components. We utilize this model to reveal the impact of surface states, diameter, lateral and vertical fields, as well as crystal structure, on electron transport and transport coefficient calculation. We show in these studies that electron transport in InAs nanowires is dominated by surface state effects that introduce measurement artifacts in parameter extraction, reduce electron mobility for smaller diameters, and degrade the subthreshold characteristics of transistors made of Zinc Blende InAs nanowires. This device model is also used for isolating vertical and lateral field effects on electron transport in nanowire transistor channels and explaining observed negative differential conductance and mobility degradation at high injection fields, which is supported by electro-thermal simulations and microstructure failure analysis. We adopt the concept of lack of inversion symmetry in polar III-V materials and the resultant spontaneous polarization charges perpendicular to the electron transport trajectory in twinned Wurtzite nanowires to explain compensation of surface charges for this type of nanowires and their enhanced subthreshold characteristics over transistors made of Zinc Blende ones. Fourth, we discuss the combined effects of surface states and field variations in InAs nanowire transistor channels to shed light on the local electrostatic behavior in 1D channels studied by scanning probe measurements. Fifth, we survey and benchmark results on nanowire transistor performance and demonstrate the superiority of InAs nanowires for high-on currents and high-speed applications. Finally, we implement a novel integration scheme for InAs nanowires on Si substrates that enables vertical alignment and electrical isolation between nanowires which is necessary for achieving multifunctional devices per single chip.

(Some figures in this article are in colour only in the electronic version)

1. Introduction and historical perspective

The rapid progress in vapor–liquid–solid (VLS) nanowire (NW) synthesis and device processing has allowed the realization of semiconductor NWs with diameters down to ∼3 nm [1] (less than ten atoms across the NW diameter) and field-effect transistor channel lengths down to 40 nm [2]. As these NWs shrink in dimensions, distinct behavior from that of bulk materials is expected. Even when NW dimensions are not small enough for significant quantum confinement, ballistic transport, surface-state effects, crystal structure and growth orientation effects can emerge and influence charge transport in NWs. The InAs material system is of particular interest for NW studies because of its high electron mobility and resulting potential for high performance devices. Bulk InAs is characterized by a small direct band-gap of ∼0.35 eV allowing a small effective mass $m^* = 0.023m_0$ (m_0 is the electron rest mass) and correspondingly high electron mobility in excess of 30 000 cm^2 $(V\ s)^{-1}$ at room temperature [3]. To exploit this high electron mobility, researchers have steadily increased the In content in the channels of high-speed heterojunction InGaAs/GaAs transistors [4] resulting in increasingly higher cut-off frequencies that are now in excess of 600 GHz [5, 6], and in lower power operation [7]. As a result of these advances, there have recently been extensive research efforts to compliment the bulk material properties of InAs with the 1D characteristics of NWs for further enhancement in high-speed performance and low power operation. In order to investigate electron transport in InAs NWs, control over the InAs NW synthesis is essential. The first report on 1D InAs synthesis dates back to 1959 when Antell and Effer observed the formation of InAs whiskers during the vapor growth of InAs crystals (from InI_3 and solid arsenic at a growth temperature of 840 °C) [8]. Antell and Effer state that 'The whiskers always seemed to grow from what appeared to have been a molten globule'. In 1966, Takahashi and Muriizumi synthesized InAs whiskers on Au- and Ag-coated glass substrates using a chemical vapor deposition (CVD) technique; however, the details of the growth mechanism were not discussed [9]. Koguchi *et al* [10] and Yazawa *et al* [11] synthesized InAs and GaAs whiskers on their respective substrates using organo-metallic vapor phase epitaxy (OMVPE) and attributed their growth to the VLS mechanism first proposed by Wagner and Ellis in 1964 for Si whisker growth [12]. The VLS growth mechanism, in which a liquid metal alloy (Au–In) initiates the growth of a solid whisker (InAs) from vapor reactants ($In(CH_3)_3$ and AsH_3), remains the generally accepted model for most InAs NW growth conditions [13–16]. As such, InAs NWs can be grown from a variety of vapor deposition techniques, the most established of which is OMVPE growth [17–19]. The growth of InAs NWs catalyzed by Au colloids requires In supersaturation in a liquid Au–In alloy. The supersaturation and consequent NW growth are determined by the input $In(CH_3)_3$ flow [20], growth time [21], temperature and the molar ratio of $AsH_3/In(CH_3)_3$ [14]. Morphology control of InAs NWs is also dependent on the proper tuning of these parameters. Figure 1 shows field emission scanning electron microscope (FE-SEM) images of InAs NWs grown on InAs (1 1 1)B surfaces from randomly dispersed Au colloids (figure 1(*a*)) and from electron-beam lithography patterned arrays of Au dots (figures 1(*b*)–(*d*)). A detailed discussion on the growth of InAs NWs can be found elsewhere [22].

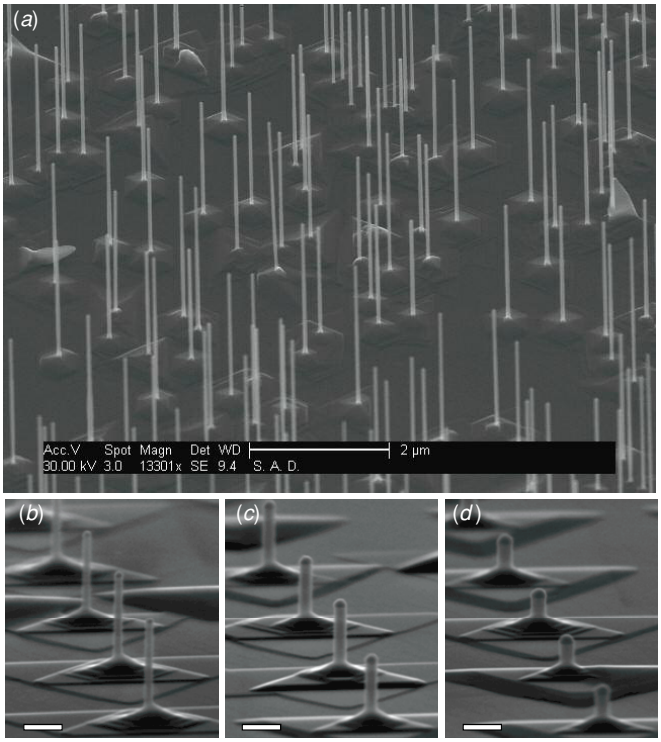

Figure 1. 45° angle view of InAs NWs grown on the InAs (1 1 1)B surface from (*a*) 40 nm diameter Au colloids dispersed from solution, and from (*b*)–(*d*) e-beam patterned Au colloids on the same substrate with 45 nm (*b*), 70 nm (*c*) and 90 nm (*d*) diameters. (Panels (*b*)–(*d*) reproduced from [21] with permission. © 2009 American Chemical Society).

The first transport studies on InAs and InAs/InP axial NW heterostructures were pioneered by Ohlsson, Björk, Thelander, Samuelson and co-workers at Lund University [23–25]. Field-effect transistor operation was demonstrated in their studies [23], band offsets [24] were calculated for InAs/InP NW heterostructures with which single-electron transistor [25] and resonant tunneling operation [26] were demonstrated at cryogenic temperatures. Reports on high electron mobility transistors from InAs NWs followed in 2005 [27, 28]. Since these early studies, there have been many reports on the transport properties of InAs NWs by various groups. In this paper, we overview our research on electron transport in InAs NWs and our studies of transport coefficient extraction from InAs NWs based on a variety of device schemes. In section 2, we demonstrate experimental observation of ballistic transport in InAs NWs over a length scale of ∼200 nm. Ballistic electron transport over such a distance indicates integrity of electron transport in InAs NWs and allows high-on current operation necessary for high-speed applications. In section 3, we introduce a device model that accounts for device parasitics in calculation of transport coefficients from NW field-effect transistors (NWFETs). While previous reports on parameter

extraction and transport coefficient calculation allow rough estimates and comparison of transport coefficients in NWs on a relative basis, accurate parameter extraction is necessary for detailed understanding and for fully exploiting the charge transport properties in NWs. Our model goes beyond what is frequently used in the literature and allows accurate parameter extraction from NWFET dc transport characterization. In sub-section 3.1, we illustrate the use of this model to quantify the effects of surface states on NWFET performance and on parameter extraction. We show that surface-state effects lead to artifacts in the measurements and consequent variations in the calculated transport coefficients on the same device. Our device model accounts for these variations and allows quantifying these effects. In sub-section 3.2, we discuss another aspect of NW scaling, the diameter-dependent transport behavior in InAs NWs. We show that smaller diameter NWs exhibit lower electron mobility and higher free carrier concentration due to the enhanced influence of surface states on the transport in smaller diameter NWs. In sub-section 3.3, we utilize our device model to evaluate the field-dependent transport properties and morphology degradation of NWFETs at high injection fields. The field-dependent analysis allows distinction between vertical and lateral field effects on transport properties in NWFETs. NW channel failure analysis helps assess the fields at which InAs NWs can operate at their maximal on-current tolerance, and how the failure point separation from the source relates to ballistic transport and electro-thermal simulations. In sub-section 3.4, we provide direct correlation between the InAs NW microstructure and transport properties. We discuss crystal structure and polymorphism in InAs NWs and discuss the transport properties of NWFETs made side-by-side of InAs NWs with different crystal structure. We use numerical device simulations to reproduce the experimental results and infer from these simulations that polarization charges at the facets of hexagonal crystal segments in InAs NWs greatly influence the transport behavior in such NWs. In section 4, we overview scanning probe microscopy studies on InAs NWs. These studies further advance our understanding of the interplay between surface states and electric fields in NWs and provide insights on the local nanoscale electrostatic behavior in 1D structures such as potential screening and its implications on device performance. In section 5, we survey results and compare performance of NWFETs made of different materials. We find that InAs NWs display the highest electron mobility, on-currents and transconductances, while improvements need to be made in surface-state passivation and device architecture for reduced short channel effects. In order for these NWs to be integrated with Si, the dominant low-cost material in the semiconductor industry, we introduce in section 6 a novel integration scheme for III–V NWs with Si substrates that allowed the realization of vertically aligned and electrically isolated InAs NWs on Si.

2. Ballistic transport in InAs nanowires

As device dimensions become of the order of the electron mean free path, ballistic electron transport in these devices governs their transport characteristics [29]. It is thus essential to determine the length scale over which ballistic transport emerges to assess the transport integrity and device dimensions for optimal high-on currents and high-speed performance. There are several methods to establish if the transport is ballistic in 1D structures. Ballistic transport in semiconducting single-wall carbon nanotubes (CNTs) was observed over length scales ~0.5 μm at room temperature, as deduced from the transmission line measurement technique [30]. Another procedure to obtain detailed information on the channel resistance in nanostrcutures is the use of conductive atomic force microscopy (cAFM), as demonstrated by Yaish *et al* who were able to isolate CNT-contact, CNT intrinsic and CNT-tip resistances [31]. Jo *et al* have used such a technique in 2007 to measure channel length-dependent resistances for In_2O_3 NWs for which the resistance kept on decreasing linearly with channel length down to ~20 nm, which is within the resolution of the nanoprobe [32]. Using a similar c-AFM approach, we have observed experimentally in 2005 ballistic transport in InAs NWs over a length scale of ~200 nm at room temperature [33].

The measurement setup shown in figure 2(*a*) comprises lithography defined Ti/Al contacts and a positionable probe constituting a diamond-coated AFM tip for two-terminal resistance measurements. Figure 2(*b*) shows the measured resistance as a function of L, the distance between the positionable c-AFM probe and the Ti/Al contact. The measured resistance is a combination of the length-independent wiring, length-independent contact series resistances and a length-dependent NW resistance in the drift-diffusion regime that becomes length independent in the ballistic regime. From this resistance combination, as the probe moves toward the fixed contact, the measured resistance should decrease if drift-diffusion electron transport is dominant and should become constant (value that sums the residual circuit series resistances) if ballistic electron transport is dominant. While the point-to-point scatter is substantial, by taking the average values in figure 2(*b*) we see a clear transition from a length-dependent to a length-independent resistance. The constant resistance region has a slope of -2.26×10^{-4} kΩ nm^{-1} with 3.6×10^{-3} kΩ nm^{-1} standard deviation while the linearly increasing resistance region has a slope of 2.24 kΩ nm^{-1} with 8.65×10^{-4} kΩ nm^{-1} standard deviation. The length-independent resistance region is indicative of ballistic transport in the NW over ~200 nm length scale and corresponds to few mean free paths as we discuss below [34]. This ballistic length is indicative of the potential of InAs NWs for high-speed electronics applications. Other materials with lower electron mobility than InAs including Si and ZnO will have lower ballistic transport lengths that are well below the resolution of the measurement technique which is dominated by the probe-tip diameter. This has led to the persistent length-dependent resistance for ZnO NWs which are not expected to have ballistic transport in nm scale [32]. To estimate the lengths over which ballistic transport is expected, one needs to calculate the average electron mean free path, $L_m = v_f \tau$, where v_f is the Fermi velocity and τ is the momentum relaxation time. v_f can be determined by calculating the energy sub-band structure of the NW under consideration, and τ can

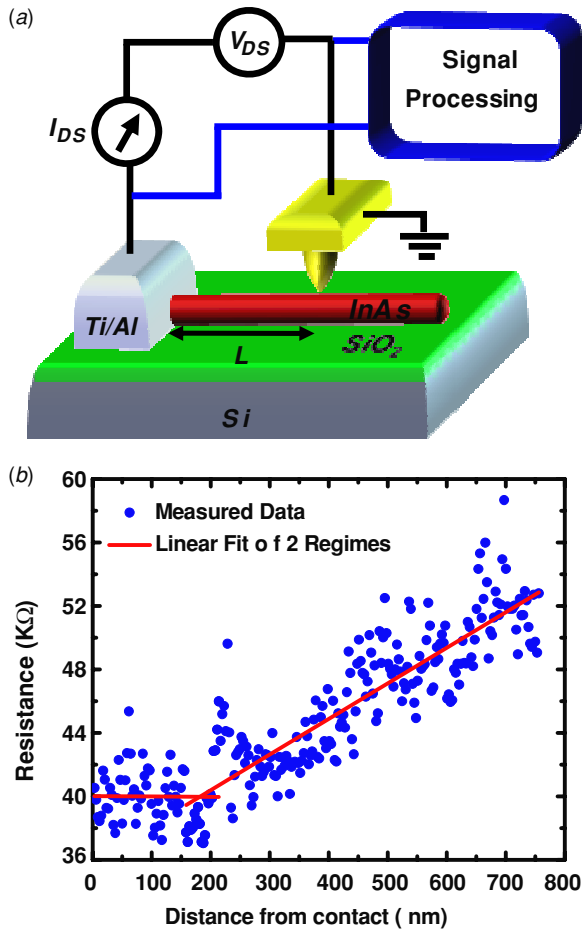

Figure 2. (*a*) Schematic drawing showing the experimental setup for measuring ballistic transport in InAs NWs. Current is injected through a positionable c-AFM tip and the overall resistance is measured as a function of NW length. (*b*) Plot of the overall measured resistance as a function of length. A constant resistance is observed over a NW length of ∼200 nm where transition from drift-diffusion into ballistic transport is observed. The constant resistance region has a slope of -2.26×10^{-4} kΩ nm^{-1} with 3.6×10^{-3} kΩ nm^{-1} standard deviation while the linearly increasing resistance region has a slope of 2.24 kΩ nm^{-1} with 8.65×10^{-4} kΩ nm^{-1} standard deviation. (Panel *b* is reproduced from [33] with permission. © American Institute of Physics.)

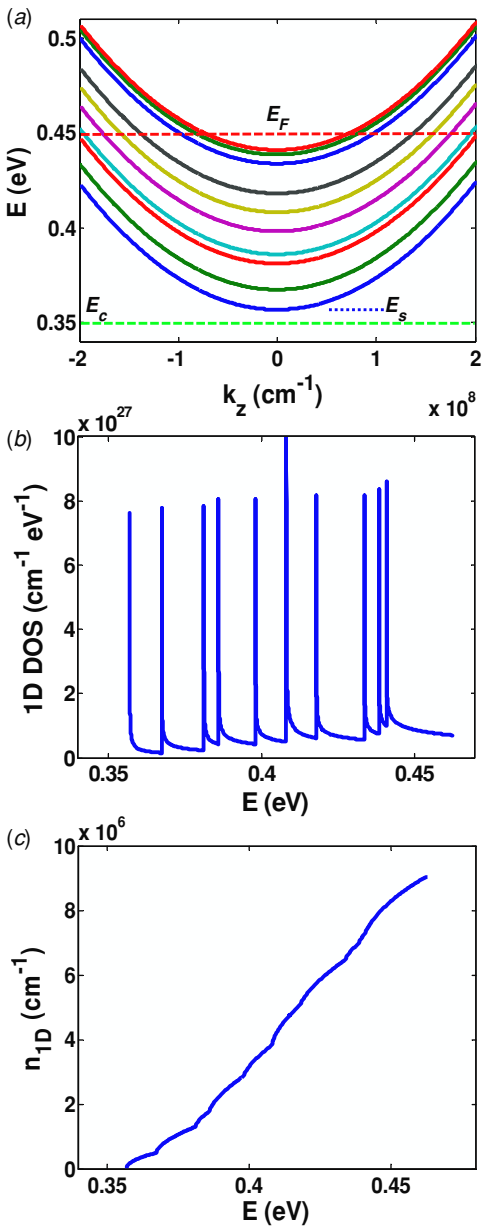

Figure 3. (*a*) Energy subband structure for a 75 nm InAs NW. E_s is the ground-state energy ($E_s(k_z = 0) - E_c \sim 6.8$ meV). Ten confined modes for this NW can lead to $n_{1D} \sim 9 \times 10^6$ cm^{-1}. (*b*) Plot of the 1D density of states (DOS) for the modes confined in (*a*). (*c*) n_{1D} resulting from the integration in (3) over the sub-band energies in (*a*) and DOS in (*b*).

be calculated from the extracted electron mobility, $\mu = \frac{q\tau}{m^*}$, where q is the fundamental charge constant. By solving Schrödinger's equation in cylindrical coordinates using the effective mass approximation—which is valid at low fields for electron energies in the vicinity of the conduction band-edge minimum—and by assuming an infinite confining potential for simplicity, one can determine the discrete energy sub-bands, $E_{m,n}$, confined in the NW using

$$E_{m,n} = \frac{\hbar^2}{2m^*}\left(\frac{\rho_{m,n}^2}{r^2} + k_z^2\right), \tag{1}$$

where $\rho_{m,n}$ is the nth root of the mth-order Bessel function J_m, $\hbar$ is the reduced Planck's constant, r is the NW radius and k_z is the wave vector in the unconfined direction along the NW axis. For a more rigorous band-structure calculation and analytical Schrödinger–Poisson solutions for charge-carrier density distribution in an InAs NW, the reader can refer to the work of Lind *et al* [35] and Wang *et al* [36]; figure 3(*a*) shows the sub-band energies for a rather large InAs NW diameter of 75 nm, similar to that used in our experiments. The number of confined modes or sub-band energies can be found by integrating over the 1D density of states from the first confined energy up to an energy over which the integrated 1D free-electron charge density, n_{1D}, is equal to that measured from experiment ($n_{1D} \sim 9 \times 10^6$ cm^{-1}). This is done using

$$n_{1D} = \left(\frac{2m^*}{\hbar^2}\right)^{1/2} \int_{E_c}^{\infty} \frac{\sum_{m,n} H(E - E_{m,n})}{\sqrt{E - E_{m,n}}} \cdot \frac{1}{1 + e^{(E-E_F)/k_bT}}\, dE, \tag{2}$$

where $H(E-E_{m,n})$ is the Heaviside function that is equal to unity when $E > E_{m,n}$ and is zero otherwise, k_b is Boltzmann's constant and E_F is the Fermi energy. Figures 2(*b*) and (*c*) show plots of the 1D density of states and n_{1D} for the 75 nm diameter InAs NW. This results in $E_F - E_c \sim 100$ meV and ~10 confined modes whose energies are shown in figure 2(*a*) according to equations (1) and (2) and without a self-consistent Schrödinger–Poisson solution. Using a lower bound mobility value of 3000 cm^2 (V s)$^{-1}$ (average mobility calculated from devices made from similar NWs), and invoking $E_f - E_{gr} = \hbar^2 k_f^2/2m^*$ with $v_f = \hbar k_f/m^*$ and E_{gr} being the ground-state energy, we estimate an electron mean free path $L_m \sim 55$ nm, a substantial value that led to the observation of ballistic transport over significant channel lengths as demonstrated experimentally and discussed above.

3. InAs nanowire FET for transport coefficient extraction

Traditionally, the extracted transconductance from measured transfer curves is used to calculate the field-effect mobility and carrier concentration in semiconductor NWs with the back-gate [37], top-gate [38] and surround-gate [27] configurations. While such calculations provide useful information about current transport in NWs on a relative basis, influence of the parasitic components on these measurements and calculations can be significant for nanostructures. To account for the influence of these parasitic factors and obtain more accurate transport coefficient extraction, we developed a simple circuit model that takes into account parasitic contact, series and leakage resistances as well as the interface state capacitance and the 2D geometry-defined gate capacitance [39].

For the experiments discussed in this section, we used OMVPE grown InAs NWs on SiO_2 surfaces. These NWs are typically ~30–100 nm in diameter and 20–30 μm in length (both depend on the growth time), and are unintentionally n-doped with the zinc blende crystal structure and [1 1 0] growth orientation [39]. The as-grown NWs are released from their growth substrates by a brief ultrasound sonication in ethanol solution, and transferred by drop-casting onto a SiO_2/n^+–Si substrate with a pre-defined grid for defining the NW position. After locating the NW on the substrate using an optical microscope, the coordinates of the NW with respect to the pre-defined grid are calculated. E-beam lithography is subsequently used to pattern electrode contacts. For source and drain electrodes, e-beam evaporation of 15 nm/85 nm Ti/Al is used followed by lift-off. For gate dielectric and top-gate electrodes, RF sputtering of SiO_2 or ZrO_2/Y_2O_3 and Al are used, respectively, followed by lift-off. The resulting top-gate NWFET device is shown in figure 4. Using the transmission line method, we extract a low contact resistance ~1.5 kΩ. This value is primarily due to the surface Fermi level pinning in the conduction band of InAs [40] that leads to surface accumulation of electrons [41] and allows formation of low resistance ohmic contacts [42]. The relative dielectric constant, ε_r, for the sputtered dielectrics was measured separately by quasi-static capacitance measurements on planar capacitor structures that were fabricated together

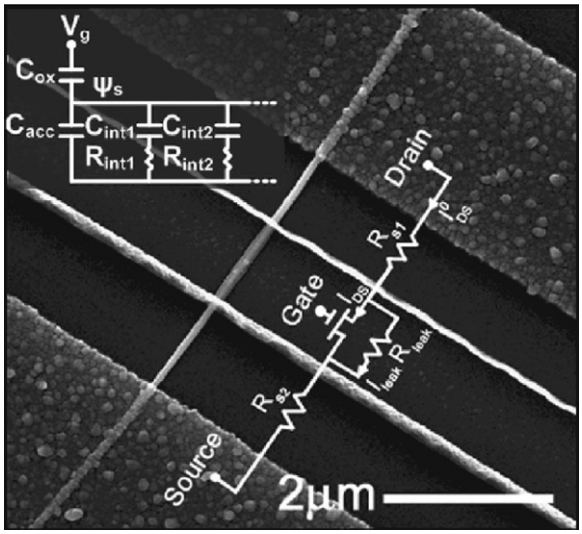

Figure 4. Field-emission scanning electron microscope (FE-SEM) of a top-gate InAs NWFET device. Top corner inset is the equivalent capacitance diagram for the depletion mode device including interface state capacitances. Bottom corner inset is the equivalent dc circuit diagram accounting for series and leakage resistance. The active portion of the device is the one directly underneath the gate and is resembled by the FET symbol in the circuit diagram. (Reproduced from [46] with permission. © 2007 American Institute of Physics.)

with the NWFETs. The resulting values were found to be 3.1 for sputtered SiO_2 and 12 for sputtered ZrO_2/Y_2O_3.

In the device shown in figure 4(*a*), we introduce an underlap (gap) region between the gate-source and gate-drain electrodes to reduce their overlap capacitance and prevent modulation of the source and drain potentials. The resistance of the underlap region and that of the contact resistance introduce a fixed drain series resistance, R_{s1}, and fixed source series resistance, R_{s2}. In addition, the presence of surface states will influence the extent of depletion across the body of the InAs NWFETs. This effect will be discussed in detail in the following sub-section (3.1). At the source-drain current, I^0_{DS}, maintains a constant finite value which constitutes sufficiently negative applied gate-source voltages, V^0_{GS}, the source–drain leakage current and can be accounted for with the introduction of a channel leakage resistance, R_{leak}. The dc equivalent circuit for the top-gate NWFET is also shown in figure 4. Using elementary circuit analysis on this dc equivalent circuit, and invoking the extrinsic measured transconductance $g^0_m = \partial I^0_{DS}/\partial V^0_{GS}$ together with current component of the active portion of the NWFET device $I_{DS} = \mu_{FE} C_{gate}(V_{GS} - V_t)V_{DS}/L^2_G$, where the absence of the superscript '0' indicates internal node voltages and currents as labeled in figure 4, one can arrive at a field-effect mobility equation [39]

$$\mu_{FE} = \frac{L^2_G V^0_{DS}(1+C_{int}/C_{acc})/C}{\left[\left(V^0_{DS}-I^0_{DS}R_s\right)^2/g^0_m - \left(I^0_{DS}\right)^2 R^2_s R_{s2} - V^0_{DS}R_{s2}\left(V^0_{DS}-2I^0_{DS}R_s\right)\right]}, \quad (3)$$

which allows mobility extraction from measured and applied voltages and currents at the outer contact electrodes, and

takes into account the parasitic resistances and interface state capacitance. Here, L_G is the physical gate length; $C_{\rm int}$, $C_{\rm acc}$ and C are the interface state capacitance, electron accumulation capacitance and gate dielectric capacitance respectively; and $R_s = R_{s1}+R_{s2}$ is the total series resistance. We note here that for the NW lengths we used ($L_{\rm SD} > 3.41$ μm, $L_G > 1.3$ μm) [28], ballistic effects are negligible. Further, with the thick oxide layer thickness (100 nm for devices utilizing SiO_2 and 73 nm for devices utilizing ZrO_2/Y_2O_3), and with the diameters used ($D > 47$ nm), quantum capacitance effects are also negligible. For each individual device subject to our study, we determine the device dimensions from SEM. With the contact resistance being determined from the transmission line model, and from the measured low-field NW resistance value, we then calculate the values of individual source and drain series resistances and channel leakage resistances. From equation (3), we can note that (i) the gate capacitance is reduced from the dielectric capacitance by $1/(1 + C_{\rm int}/C_{\rm acc})$ if $C_{\rm int}$ is non-negligible compared to $C_{\rm acc}$ and as a result, not accounting for this reduction leads to an underestimate of the mobility values; (ii) the series resistances reduce the applied source–drain bias, and not accounting for these resistances also leads to an underestimate of the mobility values. Indeed, if one neglects these parasitics, equation (3) folds down to the known field-effect mobility equation, $\mu_{\rm FE} = g_m L_G^2 / C V_{\rm DS}$.

The gate dielectric capacitance C is typically calculated using the well-known equation for a degenerately doped wire separated from a conductive plane by a dielectric material with permittivity ε and thickness $t_{\rm ox}$, using $C = 2\pi\varepsilon L_G/\ln((t_{\rm ox} + r + \sqrt{(t_{\rm ox} + r)^2 - r^2})/r)$, where r is the NW radius. This equation simplifies to $C = 2\pi\varepsilon L_G / \ln\left(\frac{2t_{\rm ox}}{r}\right)$ for $t_{\rm ox} \gg r$. For the non-planar geometry of the top-gate devices, one would need to use a 2D electrostatic simulator to calculate the device-specific capacitance. We have used Silvaco Atlas [43] and deduced gate dielectric capacitance values that are 10–14% smaller than those obtained from the capacitance equation above. Field-effect mobility values calculated using the capacitance equation above are therefore over-estimated. With all these corrections introduced into the mobility equation (3)—except for the interface state capacitance—we have calculated low-field (1.5 kV cm^{-1}) field-effect mobility values with an average of 3400 cm^2 (V s)$^{-1}$ and a peak mobility of 6580 cm^2 (V s)$^{-1}$ [39]. These mobility values from InAs NWs are still to date the highest among homogenous semiconductor nanowires and the model presented above allows us to isolate different device parameter effects on the transport coefficients as discussed below.

3.1. Surface-state effects

Surface effects play important and perhaps dominant role in the transport properties of nanoscale devices. For instance, the surface area to volume ratio scales as $2/r$, such that this ratio increases by a factor of 1000 while going from a 1 μm diameter NW to a 1 nm diameter NW, implying a significant increase in their effects. These surface and interface effects can be desirable for achieving highly sensitive sensors [44] and photodetectors [45]—at the cost of operation speed and sampling frequency—but they have adverse effects on the transport properties of FETs, some of which include (i) reduction of the gate capacitance, and therefore the gate coupling to the channel leading to lower transconductance [46] and lower switching speeds [47]; (ii) introduction of coulomb scattering centers that reduce $\mu_{\rm FE}$, and therefore the overall performance of the FET [48]; (iii) poor sub-threshold characteristics, i.e. non-steep current turn-on characteristics; (iv) inaccuracies in field-effect mobility and carrier concentration estimation [49]; (v) hysteresis in the FET transfer curves. While all these effects are inherently present in our InAs NWFET devices, we focus below on the effect of surface states on transport coefficient extraction.

The interface state capacitance is a differential capacitance that is a function of surface potential, Ψ_s, which is in turn a function of axial and radial potential drops across the NW channel. This capacitance is expressed as $C_{\rm int} = \frac{{\rm d}Q_{\rm int}}{{\rm d}\Psi_s} = q\frac{{\rm d}N_{\rm int}}{{\rm d}E_s}$, where $Q_{\rm int}$, $N_{\rm int}$ and E_s are the modulated interface state areal charge, areal density and energy, respectively. As a result, $C_{\rm int}$ can change while measuring the output and transfer curves of an FET, which are typically used in extracting the transport coefficients, and these changes need to be accounted for. In InAs, interface states are known to have donor-type characteristics [50] that are charge neutral when occupied by an electron and are positively charged otherwise [51]. These donor-type interface states accumulate electrons at the surface, and the electron accumulation layer forms a conduction channel that is hard to deplete and that leads to high-off currents.

One can assess the effects of surface states on transport coefficient extraction by varying the gate-voltage sweep-rate. Here, we mean by varying the gate-voltage sweep-rate changing the hold-time at which the gate voltage was applied for measuring each data point. Due to slow surface-state trapping and de-trapping, the surface-state charge density can be modulated by varying the gate-voltage sweep-rate, which in turn modulates the free carrier concentration in the channel. A gate-voltage sweep-rate-dependent extrinsic transconductance is thus expected. Figure 5(*a*) shows the extrinsic $I^0_{\rm DS} - V^0_{\rm GS}$ characteristics for different gate-voltage sweep rates from 100 V s^{-1} to 1.7 mV s^{-1} with negative to positive sweep direction of $-4{\rm V} < V^0_{\rm GS} < 4{\rm V}$. The gate leakage current is six orders of magnitude lower than those $I^0_{\rm DS}$ values shown in figure 5(*a*), and thus does not contribute to the observed decay 'tails' in $I^0_{\rm DS}$ at negative gate voltages. These current tails can be attributed to the long trapping and de-trapping time constants in the InAs NWs that lead to current decay times of the order of 45 s [46], as well as to ambipolar hole conduction where at sufficiently negative gate bias, hole inversion at the surface facing the gate can be achieved with the concurrent presence of a conduction channel at the other pinned surface away from the gate. It can be readily seen from figure 5(*a*) that the off-current decreases, on-current increases and the extrinsic transconductance increases (from $\sim$1 μS to $\sim$12 μS) with slow gate-voltage sweep-rates. Using equation (3), and setting $C_{\rm int}/C_{\rm acc}$ to zero—as this effect is virtually included in equation (3) by varying the sweep rate which readily modulates

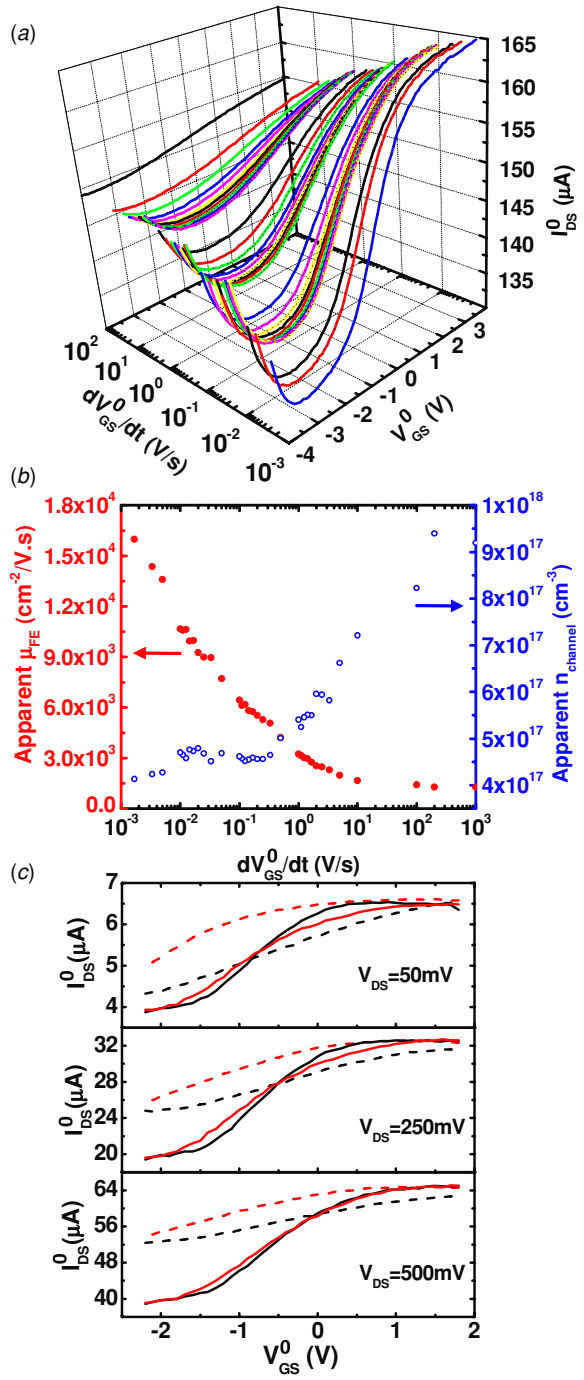

Figure 5. Effect of surface states on extrinsic (*a*) transfer curves of an InAs NWFET with $L_{SD} = 3.5\ \mu$m, $L_G = 0.78\ \mu$m, $D = 110$ nm, plotted for different gate-voltage sweep-rates, (*b*) computed μ_{FE} and $n_{channel}$ from the transfer curves in (*a*) and (*c*) hysteresis in transfer curves at different V^0_{DS}. Dashed lines represent a sweep rate $>$ 10 V s^{-1} and solid lines represent a sweep rate of 6.7 mV s^{-1}. (Reproduced from 46 with permission. © 2007 American Institute of Physics.)

C_{int}—one can extract mobility values of ∼1000 cm^2 (V s)$^{-1}$ at fast V_{GS} sweep rates, which is in agreement with those reported for similar InAs NW devices [52, 53] and ∼16 000 cm^2 (V s)$^{-1}$ at slow gate-voltage sweep-rates. A slow gate-voltage sweep-rate is expected to allow a charge balance between carrier capture and emission such that the inherent NW carrier mobility and concentration can be extracted. This high mobility value highlights the potential of InAs NWs for high-speed electronic devices provided adequate passivation of surface states can be achieved. One can also infer the effects of varying the gate-voltage sweep-rate on free carrier electron charge modulation in the channel. A more charge-neutral surface will lead to a lower electron density in the channel, which is indeed observed with slow gate-voltage sweep-rates as illustrated in figure 5(*b*). Hysteresis in the transfer curves arises due to time lags in charge capture and emission from interface states [54, 55]. We have observed a reduction in the hysteresis in the transfer curves with slower gate-voltage sweep-rates at different V^0_{DS} values, as shown in figure 5(*c*). This also indicates that a more charge-neutral surface is attained at slow gate-voltage sweep-rates and that the extracted transport coefficients at these sweep rates reflect on the inherent transport behavior in the NW channel. These characterization techniques to quantify the effects of surface states from easily accessible dc *I–V* characterization have been subsequently applied to other NW materials such as ZnO [56] and GaN [57].

3.2. *Diameter effects*

From the discussion above, surface effects are also expected to emerge with scaling the NW diameter. Earlier studies have attributed the diameter-dependent transport behavior due to either (i) only changes in carrier concentration, such as in Si NWs [58, 59], where surface depletion modulates the free carrier density in the channel as the diameter changes or (ii) only changes in carrier mobility such as in GaN NWs [60]. Using the dc circuit model discussed above, we are able to extract the intrinsic NW *I–V* characteristics and compute the diameter-dependent carrier mobility and carrier concentration [61]. With the intrinsic output and transfer curves, one can isolate the diameter dependence from the field dependence by extracting the transport coefficients at the same gate-source and source-drain fields.

Figure 6(*a*) shows the extracted transfer curves for a set of NWs with different diameters and similar gate lengths. It can be seen that smaller diameter NWs exhibit lower currents. When normalized to the NW diameter and length, the conductivity of these wires decreases with decreasing NW diameter [61]. This behavior is expected in the drift-diffusion transport regime which is dominated by transport near the surface of the NW channel where electrons encounter enhanced surface roughness (coulomb) scattering. Figure 6(*b*) shows computed energy band-edge diagrams, electron density and the first five confined states from a self-consistent Schrödinger–Poisson solver in the radial direction of a 75 nm diameter InAs NW. A fixed surface-state charge density of $Q_f/q = 2.7 \times 10^{12}$ cm^{-2} and a donor doping density of 5×10^{16} cm^{-3} were assumed in these solutions. Strong electron accumulation at the NW surface can be deduced from the downward band bending of the conduction band below the Fermi energy, and the electron density peaks within 5 nm from the NW surface. These surface electrons are

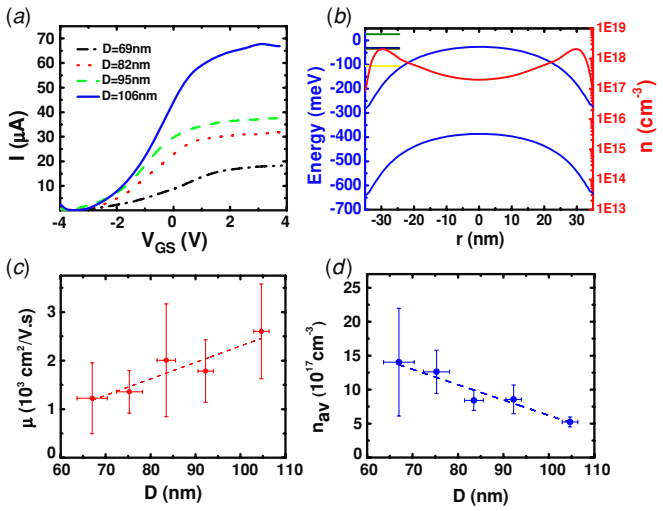

Figure 6. (*a*) Plot of the extracted transfer curves for different diameter NWFETs. (*b*) Band-edge diagram, the first five confined energies (top left; E_2, E_3 and E_4, E_5 are too close and overlap on this energy scale) and electron concentration profile across a NW diameter of 70 nm. A surface-state density of $Q_f/q = 2.7 \times 10^{12}$ cm^{-2} and a donor doping density of 5×10^{16} cm^{-3} were used in these self-consistent numerical simulations. (*c*)–(*d*) Plot of the average NW field-effect mobility (*c*) and free carrier concentration (*d*) as a function of NW diameter. (Reproduced from [61] with permission. © Wiley-VCH.)

dominated by surface roughness scattering, and the electron field-effect mobility is thus reduced as the NW diameter decreases. This was experimentally observed as can be seen in figure 6(*c*) where the average mobility of 26 devices with different diameters has been calculated at $V_{GS} = 0$ V and $V_{DS} = 0.15$ V, in the low-field drift regime. As the NW diameter decreases, the contribution of these surface electrons to the total electron density in the channel increases and the integrated free-electron charge density increases as the NW diameter decreases, as observed in figure 6(*d*). Numerical simulations using Silvaco have validated this trend of charge carrier density with NW diameter. A surface-state density of $Q_f/q = 2.7 \times 10^{12}$ cm^{-2} and a donor doping density of 5×10^{16} cm^{-3} were found to produce similar electron densities to those calculated from experiment [61]. Ford *et al* have also reported reduction in carrier mobility in InAs NWs as the NW diameter decreases for diameters in the range 14–40 nm [62].

3.3. Field dependence

Variation of vertical (gate-channel) and lateral (drain-source) fields in the channel modulates the electron's transport trajectory and energy, yielding field-dependent transport behavior. While all previous works discuss mobility reduction as a function of gate voltage due to enhanced surface scattering in the accumulation or depletion regimes, mobility degradation with source–drain voltage due to enhanced phonon scattering/thermal heating is rarely discussed in detail. In this section, we discuss field effects on electron mobility by previewing the vertical field dependence, discussing the lateral field dependence, and the effects of high injection fields on electron transport and NW morphology. We support our conclusions on device failure with scanning tunneling electron microscopy (STEM) analyses and electro-thermal simulations [63].

The measured output characteristics of a back-gate twinned wurtzite (WZ) InAs NWFET (figure 7(*a*)) and the extracted output characteristics of a top-gate zinc blende (ZB) InAs NWFET (figure 7(*b*)) show reduction of output current with increased source–drain bias, indicative of mobility degradation in these regimes. Following the negative differential conductance (NDC) regime in figure 7(*a*), avalanche multiplication in the narrow band-gap InAs ($E_g = 0.35$ eV) takes over leading to onset of breakdown characteristics for $V_{DS}^0 \geqslant 1.2$ V (full breakdown characteristics have been observed and are not shown here). For the InAs ZB NWFET, the series resistances prevent observation of NDC in the measured output curves and extraction of output curves for the active portions of the NWFET device, such as in figure 7(*b*), is necessary. With the aid of extracted transfer curve such as that in figure 7(*c*), one can compute the field-effect mobility using the simplified version of equation (3), $\mu_{FE} = g_m L_G^2 / C V_{DS}$. To reveal the vertical and lateral effects on the transport behavior in the NW channel, we constructed in figure 7(*d*) a 2D contour plot of the extrinsic transconductance obtained from several $I_{DS}^0 - V_{GS}^0$ transfer curves measured for V_{DS}^0 in the range of 0–2.5 V. In figure 7(*d*), we can observe that with both V_{DS}^0 and V_{GS}^0, the extrinsic transconductance increases and then decreases with applied bias. To discuss these effects individually, let us consider first the vertical gate-channel transconductance and mobility behavior (figure 7(*e*)). In the linear operating regime ($V_{GS} \geqslant 1.9$ V), one can use the simplified version of equation (3) to compute the field-effect mobility as a function of gate bias. The field-effect mobility is low at negative gate voltages due to Coulomb scattering from fixed oxide charges, interface state charges and ionized impurity charges [48], which are dominant at low carrier densities that cannot screen the potential of these charged scattering centers. As the gate voltage approaches the flat-band voltage (typically negative due to donor surface charges), the mobility peaks, and then reduces as V_{GS} increases in the accumulation region near the surface due to interface roughness scattering [64, 65]. The symmetric behavior of μ_{FE}–V_{GS} observed here is due to the poor sub-threshold characteristics (non-steep turn-on characteristics) of the InAs NWFETs and should be typically more steep in the absence of surface states for voltages below the flat-band voltage [64, 66].

Using the dc circuit model for the top-gate NWFET, we can calculate the lateral electric field across the active portion of the NWFET device and compute the electron drift velocity in the channel according to

$$v = \frac{I_{DS}^0(1 + (R_{s1} + R_{s2})/R_{leak}) - V_{DS}^0/R_{leak}}{C(V_{GS}^0 - V_T)/L_G - C I_{DS}^0 R_{s2}/L_G} \tag{4}$$

which simplifies to $v = \frac{I_{DS}^0}{C(V_{GS}^0 - V_T)/L_G}$ if the device parasitics are neglected, from which the popular mobility equation $\mu_{FE} = g_m^0 L_G^2 / C V_{DS}$ derives, assuming $v = \mu_{FE} E$, with $E = V_{DS}/L_G$. We calculate the device parasitics from the output and transfer curves of each V_{DS}^0 bias point and the

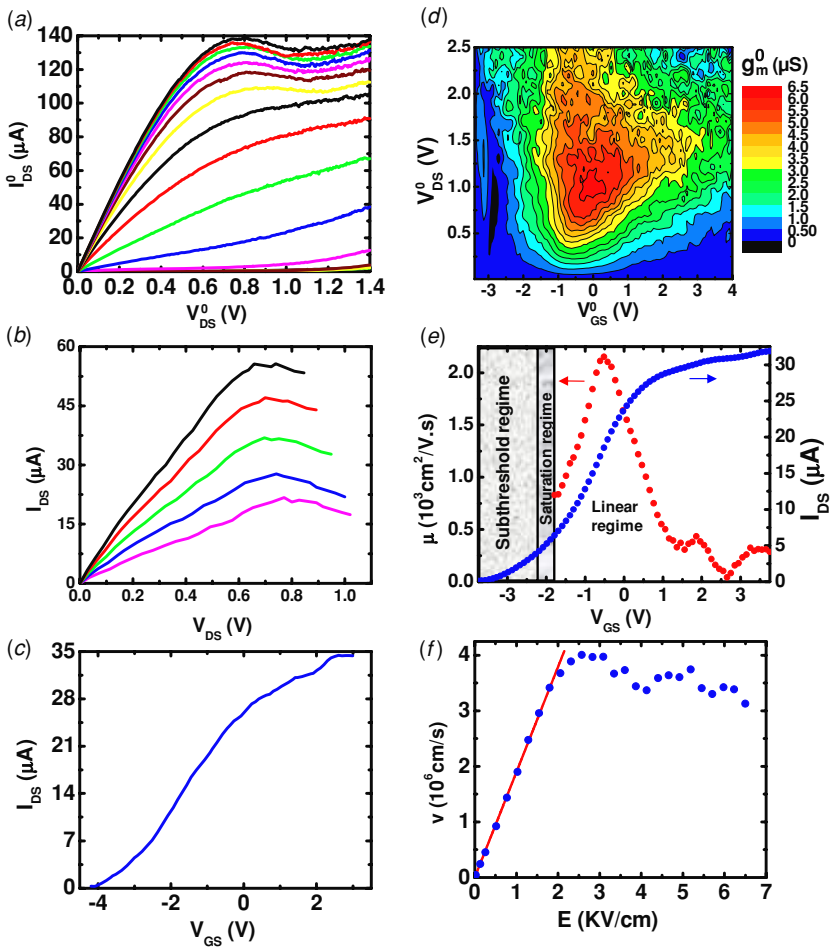

Figure 7. (*a*) Plot of the extrinsic output curves of a back-gated WZ InAs NW (D = 243 nm) showing NDC at high current values followed by onset of breakdown characteristics. $V^0_{GS} = -40$ V to +40 V with 5 V steps. (*b*) Plot of the extracted output curve for a top-gate ZB NWFET device ($D = 90$ nm, $L_G = 0.97$ μm, $L_{SD} = 3.57$ μm) showing also the NDC signature. $V^0_{GS} = -4$ V to +4 V with 2 V steps. (*c*) Transfer curve of the wire in (*b*) with $V^0_{DS} = 0.5$ V. (*d*) Contour plot of the extrinsic transconductance for the same device in (*b*) and (*c*) as a function of V^0_{DS} and V^0_{GS}. (*e*) Plot of the extracted field-effect mobility and current as a function of extracted gate voltage. (*f*) Velocity-field plot extracted as a function of the source–drain field for the same device in (*b*)–(*d*) extracted from several output and transfer curves. (Panels (*b*)–(*f*) are reproduced from [63] with permission. ©2008 American Chemical Society.)

drift velocity is calculated near $V^0_{GS} = 0$ V using equation (4) and is plotted in figure 7(*f*). For $0 \leqslant E \leqslant 1.5$ kV cm^{-1}, the slope of the $v(E)$ plot is the low-field effective electron mobility, μ_{eff} (calculated from the conductance rather than the transconductance typically used to calculate the field-effect mobility), which is ∼1900 cm^2 (V s)$^{-1}$. The drift velocity peaks at $\sim 4 \times 10^6$ cm s^{-1} and decreases for $E \geqslant 2.7$ kV cm^{-1}. This velocity value is smaller than that in bulk InAs ($\sim 3 \times 10^7$ cm s^{-1}) [67], likely due to dominant surface scattering in the InAs NWFETs.

Numerous effects can lead to NDC in FETs. We examine the applicability of these various effects to InAs NWFETs and show that phonon scattering is what causes NDC in these devices. First, it may be appealing to explain NDC behavior due to non-parabolicity in the energy–momentum band structure for a small band-gap material such as InAs, where high-energy electrons exhibit high effective masses and reduced momentum relaxation times [68, 69]. This has been used to explain NDC in CNTs [70]. Second, intravalley or inter-sub-band scattering where electrons scatter from high energy sub-bands to equivalent energy sub-bands but with lower momentum may also be important in 1D nanostructures and lead to NDC. Third, intervalley scattering ($\Gamma \rightarrow X$ or $\Gamma \rightarrow L$) is less likely for InAs due to the relatively large energy separations for these band-gap minima ($E_{\Gamma L} = 0.73$ eV and $E_{\Gamma X} = 1.02$ eV). Fourth, phonon scattering and momentum relaxation to the lattice may also lead to NDC. Hot phonon distribution was suggested to dominate NDC in CNTs [71]. We have performed electrothermal simulations and STEM studies on InAs NWs stressed under high electric fields to show that thermal heating is the dominant process in the observed NDC behavior.

Electro-thermal simulations were performed using Silvaco Atlas for a material stack (including the 350 μm thick Si substrate and long Al contact leads) and device dimensions similar to those used in experiment. The carrier mobility and contact resistance were varied to fit the experimentally measured current density to the numerically calculated one from the 2D simulations. A constant fixed surface charge and donor doping densities similar to those of section 3.1 were assumed. Figure 8(*a*) shows excellent fit between the simulated and measured current densities for a mobility

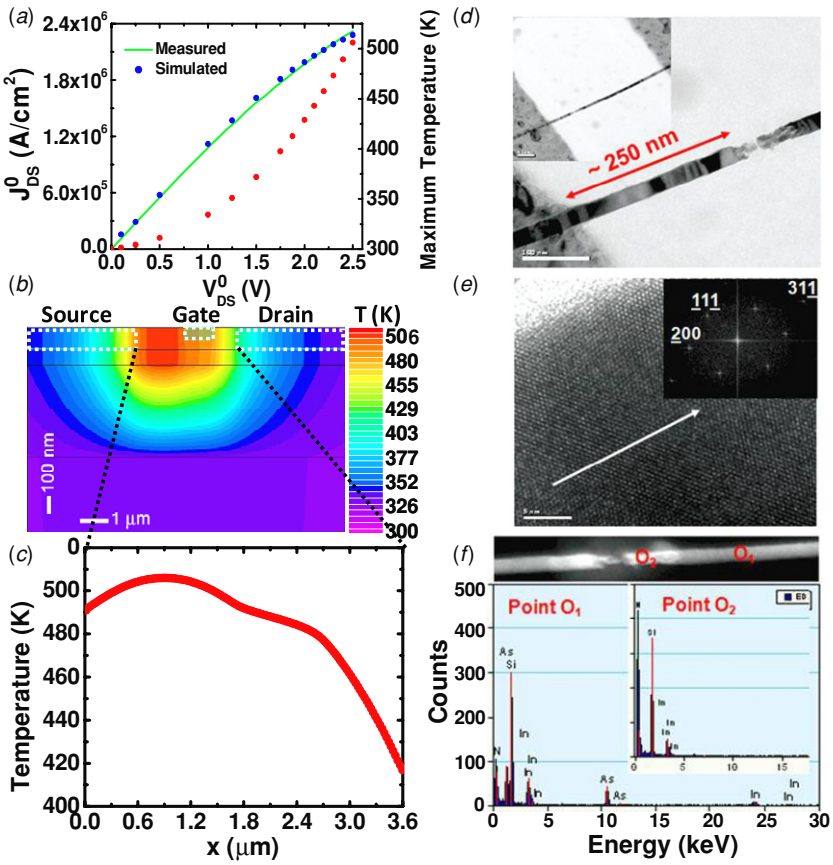

Figure 8. (*a*) Plot of the measured and simulated current density and channel temperature peak as a function of applied voltage in an InAs NW with device architecture similar to that of figure 7(*b*). (*b*) Contour plot of temperature across the NW device and (*c*) line cut across the center of the NW channel of a temperature profile from the source ($x = 0$) to the drain ($x = 3.6$ μm). (*d*) TEM images of the InAs NW device on the Si_3N_4 TEM grid subject to voltage stress and breakdown. (*e*) HR-TEM image of the same device away from the break region showing the single crystal ZB NW growing in the ⟨3 1 1 1⟩ orientation. (*e*) Dark field TEM image and EDS spectra collected near (O_2) and away (O_1) from the break region. (Reproduced from [63] with permission. ©2008 American Chemical Society.)

value of 16 000 cm^2 (V s)$^{-1}$, and a contact resistance of 350 Ω/electrode. These values are in good agreement with those extracted from experiment in section 3.1. Figure 8(*b*) shows a contour plot of the temperature across the NWFET device with a line cut across the center of the channel from the source ($x = 0$) to the drain ($x = 3.6$ μm). The region over which the temperature in the channel exceeds 500 K is ∼250 nm from the source electrode. This is in agreement with the distance over which ballistic transport has been estimated in a similar InAs NW, beyond which diffusive transport and phonon scattering dominate. With a 200 K increase above room temperature, an electron mobility reduction by a factor of 2 has been observed in bulk InAs (1 0 0) surfaces [72].

To assess the effect of thermal heating on the NW morphology, we used TEM and STEM analyses on two-terminal InAs NW devices fabricated on a 100 nm Si_3N_4 membrane. The InAs NWs were stressed with different V_{DS} biases until breakdown is observed. For the NW shown in figure 8(*d*) ($D = 33$ nm, $L_{SD} = 1.5$ μm), the InAs NW breaks down (current drops to zero) at a current density of ∼10^7 A cm^{-2} (at $V^0_{DS} = 1.98$ V). When normalized to the NW perimeter, we obtain ∼1 A mm^{-1}, similar to the record value in InGaAs MOSFET 1.05 A mm^{-1} [73], despite the lower heat dissipation in the case of the InAs NW over the air-suspended nitride membrane. It is also noteworthy that the distance at which the NW discontinuity appears is ∼250 nm away from the source side, in agreement with electro-thermal simulations showing highest temperatures in this region and the approximate measured ballistic length in InAs NWs. Away from the discontinuity region, the NW is a single crystal with ZB crystal structure and ⟨3 1 1⟩ growth orientation as illustrated in figure 8(*e*). Figure 8(*f*) shows a dark field scanning TEM image of the wire with brighter regions near the break. Point EDS spectra at the broken region show only the In peak in addition to the Si and N peaks, whereas those taken away from the broken region show both In and As peaks. This suggests that local heating beyond the ballistic transport length leads to As out-diffusion and vaporization leaving only In behind, which upon NW breakage and current cessation, freezes and shrinks in size leaving a discontinuity in the NW. With bias stress leading to high current densities in excess of 10^6 A cm^{-2} but lower than 10^7 A cm^{-2}, permanent morphology changes are induced to the NW channel and the current densities cannot be recovered upon remeasurement. These results also affirm that thermal management in nanoscale FETs is another challenging problem among other electrostatic ones.

3.4. Correlation of transport behavior with crystal structure

Most III–V materials crystallize in the ZB crystal structure. However, III–V NWs often show ZB/WZ polymorphism under different growth conditions and techniques, as discussed below, which has direct consequences on their electronic and optical properties. Such polymorphism was observed in our InAs NWs grown on InAs (1 1 1)B substrates [74]. In this section, we discuss polymorphism in InAs NWs and correlate the transport properties of pure ZB and twinned WZ NWs to their crystal structure. We utilize numerical simulations to infer about the role of polarization charges in compensating surface-state charge accumulation in twinned WZ NWs which in turn lead to better sub-threshold characteristics for these twinned NWs.

Takahashi's and Muriizumi's XRD analyses on CVD grown InAs whiskers (at 400 °C) have shown that these whiskers exhibit the WZ crystal structure, which converts fully to ZB when annealed at 800 °C [9]. Koguchi *et al* [10] and Yazawa *et al* [11] have shown through cross-sectional TEM, XRD and high-resolution TEM studies that InAs NWs grown at temperatures greater than 400 °C assume the WZ crystal structure with numerous planar defects perpendicular to their growth direction. These NWs generally grow in the ⟨0 0 0 1⟩ direction, equivalent to ⟨1 1 1⟩ ZB. This is the case because the surface free energy of the (1 1 1) plane is the lowest among all other planes in the lattice [75]. ZB and WZ crystals are based on face-centered cubic and hexagonal close-packed, respectively, and both are most densely packed in the ⟨1 1 1⟩ orientation with very similar bond lengths and system energies [76]. Twinning in their bulk or nanostructure forms is thus possible. Glas *et al* have suggested in 2007 that the surface energies of the NW facets may lead to preferential nucleation at triple phase interfaces (vapor–liquid–solid, i.e. edge of the growth seed) rather than at the liquid–solid interface [77]. Lower WZ facet energies and high nanoparticle supersaturations would then favor the formation of WZ NWs of III–V semiconductors. A simple rotation of the third nearest neighbors in the (1 1 1) planes by a quarter of the body diagonal of ZB crystal with ABCA layer stacking leads to ABAB layer stacking and to the formation of WZ InAs. This is illustrated in figures 9(*a*)–(*c*) where a planar view of the crystal structure of ZB, WZ and a mixture of WZ/ZB/WZ is shown.

Twinning and polymorphism may be clearly identified under TEM, however, at only certain pole axes. Figure 9(*d*) shows a TEM image of an InAs NW taken near its tip where the NW is imaged from the [0 $\bar{1}$ 1 0] pole orientation, and the NW appears to be defect free. Figure 9(*e*) shows a TEM image of the same NW shown in figure 9(*d*), however imaged form the [2 $\bar{1}$ $\bar{1}$ 0] pole axis where the difference in layer stacking between WZ and ZB can be identified such that twin planes are visible. The density of these twin planes did not seem to vary from the tip of the NW toward its base. A HR-TEM image near the center of the InAs NW is shown in figure 9(*f*) where stacking faults and a small ZB segment are clearly visible. On the other hand, NWs grown on SiO_2 substrates at ∼350 °C do not maintain an epitaxial relationship with the substrate and generally grow in the [1 1 0] orientation, where the probability of forming WZ crystal structure in this growth direction is low. It was observed however that these NWs with diameters >40 nm exhibit a twin along the axis of the NW between two equivalent [1 1 0] orientations as shown in figure 9(*g*).

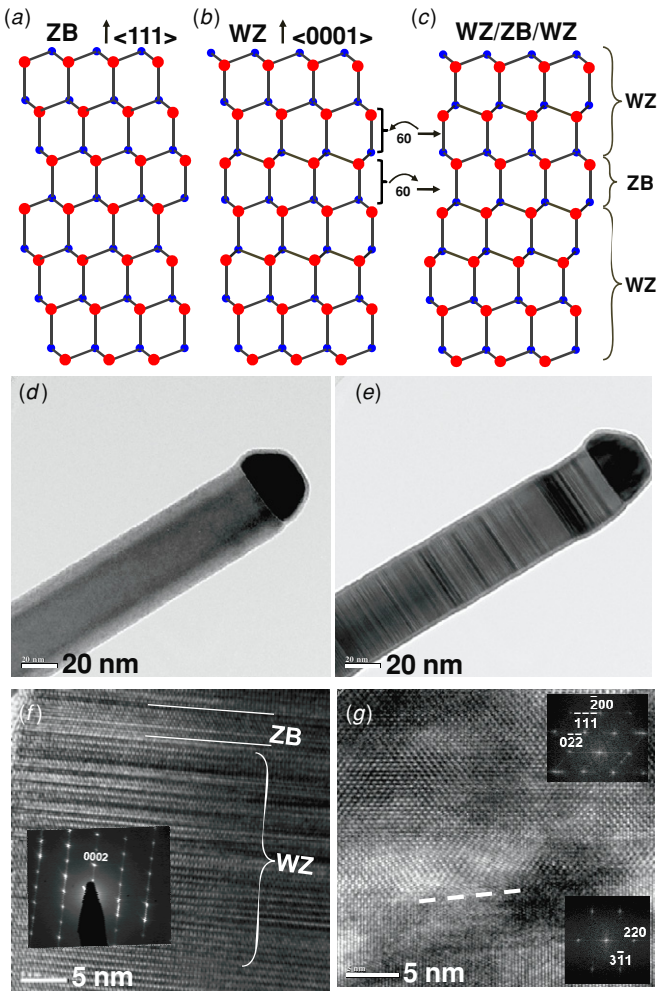

Figure 9. Crystal structure for a (*a*) ZB, (*b*) WZ and (*c*) WZ InAs NW with a ZB twin. (*d*) TEM image of an InAs NW grown on an InAs (1 1 1)B surface with an electron beam direction (pole) of [0 $\bar{1}$ 1 0]. TEM image of the same segment in (*d*) rotated to a pole axis of [2 $\bar{1}$ $\bar{1}$ 0] where stacking faults become visible. (*f*) HR-TEM image showing lattice fringes, stacking faults and a small ZB segment highlighted with two white lines. Inset is the corresponding diffraction pattern indicating the WZ crystal structure with a [0 0 0 2] growth direction. Stacking faults are clearly visible and a small ZB segment is highlighted by two white lines. (*g*) Lattice fringes of an InAs NW grown on the SiO_2 surface with inset FFT patterns of the top and bottom portions showing [0 1 1] and [−1 1 4] pole orientations and indicating ZB crystal structure. (Panels (*f*) and (*g*) are reproduced from [74] with permission. © 2009 Wiley-VCH.)

Despite the clear differences in crystal structure, the effect of polymorphism and the correlation of crystal structure with electronic and optoelectronic properties of NWs have received little attention [78–80]. Concurrently, we have observed distinct sub-threshold characteristics of NWFETs made of twinned WZ and pure ZB InAs NWs. We attribute these effects to the presence of spontaneous polarization charges at the WZ/ZB heterointerface as we discuss below.

Back-gate InAs NWFETs have been fabricated on the same chip from both types of NWs (ZB and twinned WZ)

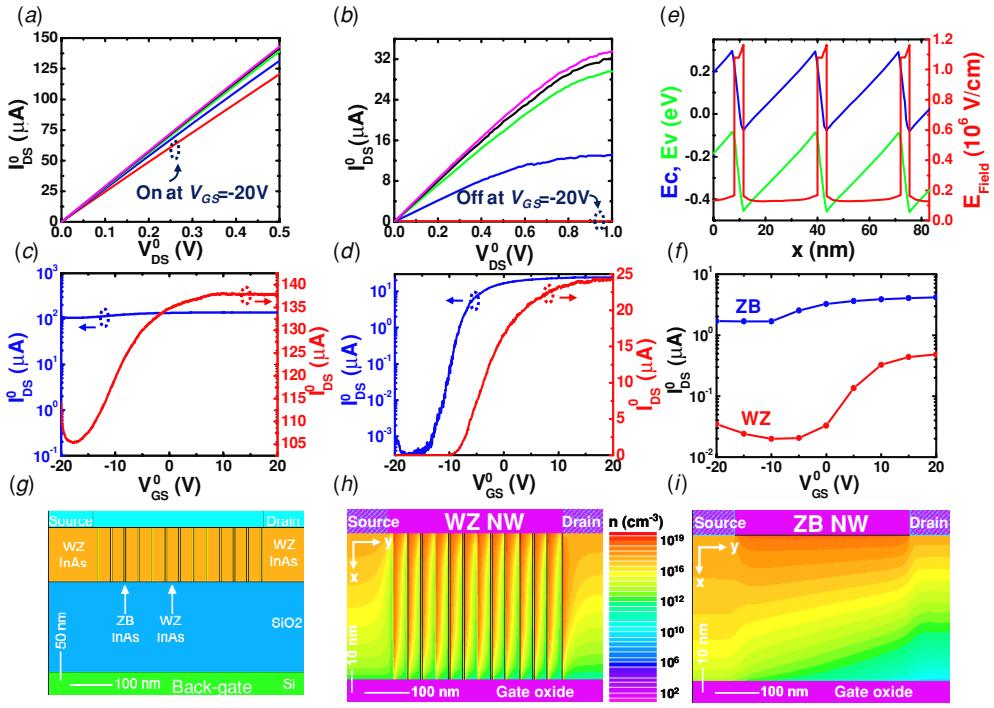

Figure 10. Experimental output curves of (*a*) ZB and (*b*) twinned WZ back-gate InAs NWFETs. Transfer curves of (*c*) ZB and (*d*) twinned WZ for the same InAs NW FETs shown in (*a*) and (*b*). (*e*) Simulated energy band-edge diagram and electric field across the transport direction in the channel of a WZ InAs NW with ZB segments. (*f*) Simulated transfer curves of ZB and WZ InAs NWFETs with device architecture shown in (*g*) with the pure ZB channel when referring to the ZB case. Contour plots of the free carrier concentration in WZ (*h*) and ZB (*i*) NWFETs. The simulations in (*e*)–(*i*) assumed a 2×10^{12} cm^{-2} surface-state density and 10^{13} cm^{-2} spontaneous polarization charge density. Contour plots in (*h*)–(*i*) were extracted at $V_{DS} = 0.5$ V and $V_{GS} = -20$ V. Channel length of both devices is 400 nm. (Reproduced with permission from [74]. © 2009 Wiley-VCH.)

and their dc characterization was carried out under the same sweep rate conditions. Figures 10(*a*) and (*b*) show the output characteristics of a ZB and a twinned WZ InAs NWFET, respectively, with similar channel length of ∼3.4 μm where the ZB NWFET cannot be pinched off at $V_{GS}^0 = -20$ V, while the twinned WZ NWFET was pinched off for the same V_{GS}^0. The current modulation is further evident in the transfer curves of these NWs shown in figures 10(*b*) and (*c*) where the ZB NWFETs show poor sub-threshold characteristics with $I_{on}/I_{off} < 2$ when compared to the twinned WZ NWFETs which show better sub-threshold characteristics with $I_{on}/I_{off} \sim 10^4$. The current density in the ZB NWFETs is about one order of magnitude larger than that in WZ NWFETs. This is due to differences in the contact resistances with the two types of wires, where ZB NWs show a contact resistance of ∼1.5 kΩ whereas the twinned WZ NWs show a contact resistance of ∼11.3 kΩ, both extracted through the transmission line method. These sub-threshold trends are observed for the 17 devices subject of this study. We note that for $L_{SD} < 1$ μm, these devices with a 100 nm SiO_2 dielectric layer show strong short channel effects where the I_{on}/I_{off} ratio for twinned WZ NWs approaches 10. The transport coefficients of these devices were calculated according to the model discussed earlier, and the average values of the free carrier concentration and mobility are $n_{av}(ZB) = 6.4 \times 10^{17}$ cm^{-3}, $n_{av}(WZ) = 8.5 \times 10^{17}$ cm^{-3}, $\mu_{av}(ZB) = 2200$ cm^2 (V s)$^{-1}$ and $\mu_{av}(WZ) = 1700$ cm^2 (V s)$^{-1}$. This slight difference in the transport coefficients is not sufficient to induce the large difference in the sub-threshold characteristics in the two types of NWs.

The band offsets for bulk WZ InAs with respect to ZB InAs are $\Delta E_c = 86$ meV for the conduction band and $\Delta E_v = 46$ meV for the valence band with staggered band-edge alignment at the WZ/ZB heterointerface [81]. If one assumes the periodicity of the ZB segments in the mostly WZ NW to be 3.5 nm every 28.5 nm based on figure 9(*f*) over a 400 nm channel length, and with an InAs surface-state density of 10^{12} cm^{-2} in a material layer stack similar to that used in experiment (figure 10(*g*)), Silvaco Atlas simulations resulted in poor sub-threshold characteristics for both twinned WZ and ZB NWFETs. This indicates that band offsets alone do not explain the distinct sub-threshold behavior. Due to the lack of inversion symmetry in hexagonal crystals, it is known that the {0 0 0 1} facets have spontaneous polarization charges [82]. Since the current flow is in the [0 0 0 1] direction of the twinned WZ NWs, these spontaneous polarization charges lead to field modulation in the channel and compensation of the surface states' field as indicated by the energy band-edge diagrams of figure 10(*e*) (simulated under thermal equilibrium conditions). With a spontaneous polarization charge density of 10^{13} cm^{-2}, the gate field penetrates deeper into the channel of a twinned WZ NW with ZB segments (figure 10(*h*)) when compared to the pure ZB NW where depletion is restricted near the surface closest to the gate. The transfer curves from these two structures show better sub-threshold characteristics of the twinned WZ NW compared to the ZB NW (figure 10(*f*)). The

I_{on}/I_{off} ratio here is dominated by short channel effects for the 400 nm channel length device with the 100 nm SiO_2 thick dielectric layer. Simulations various surface-state densities and polarization charges with indicated that a spontaneous polarization charge density of 10^{13} cm^{-2} is required to induce the observed experimental sub-threshold trends with the periodicity of ZB/WZ segments used [74]. This density is comparable or is lower than spontaneous polarization charge densities well known for other polar material systems such as GaN, AlN, InN and ZnO [83]. Our HR-TEM analysis indicated little difference in the lattice spacing of the $\{1\,1\,1\}$ and $\{0\,0\,0\,1\}$ planes of the ZB and WZ segments leading to a piezoelectric polarization charge density $\sim 5 \times 10^{11}$ cm^{-2}, lower than that needed to pinch off the twinned WZ NWs and than the expected spontaneous polarization charge density [74]. These results suggest that spontaneous polarization charge effects in polymorph NWs need to be accounted for in the design of InAs and other III–V NW devices.

4. Scanning probe measurements on InAs nanowires

In section 3, we isolated the effects of surface states, diameter, field and crystal structure on transport behavior in InAs NWs. The interrelationship between surface states and device vertical and lateral fields and the local nanoscale electrostatic behavior can be revealed by scanning gate microscopy (SGM) and scanning capacitance spectroscopy (SCS) measurements performed by Zhou *et al* [84], and Law *et al* [85] on these NWs. Specifically, we show by SGM that local modulation of current in the NWFET channel is maximal near the injecting/extracting electrodes and we probe by SCS the contact potential screening in the 1D NW which extends over several μm across the NW length.

SGM has been successfully used in earlier studies on single-wall CNTs to identify individual scattering sites and transport barriers along the CNT length [86], and on Si NWs to probe conductance variations in a doping-modulated NW [87]. The measurement setup is similar to that of figure 2(*a*), however, with V_{DS} applied across two Ti/Al metal electrodes, and a V_G applied to a metal coated AFM tip that is used as a local positionable gate electrode. Figure 11(*a*) (top panel) shows an AFM topograph of the 1 μm channel, 45 nm diameter InAs NW, subject of this study coated with 20 nm SiO_2 dielectric layer. Figure 11(*a*) (bottom panels) shows SGM current images at different V_G biases of -4, -2, 0, 2 and 4 V taken at a V_{DS} bias of 0.3 V. The measurements were performed in tapping mode where the AFM tip is kept at $\sim$5 nm above the device structure and scans over all the area shown in figure 11(*a*). Dark regions in the SGM images indicate a low current (electron depletion) and bright regions indicate a high current (electron accumulation). These regions appear to be evident near the edges of the NW where the coupling of the AFM tip (gate) to the NW channel is maximal due to the geometry of the tapered tip and the thin oxide at the edges of the NW [88]. To gain a more straight-forward understanding of these data, the transconductance measured with the AFM tip step of 6 nm in the channel is averaged over 100 nm periods, and is plotted in figure 11(*b*) at $V_{DS} =$ 0.045 V and $V_{DS} = 0.3$ V. One can observe in figure 11(*b*) the following: (i) g_m^0 is generally higher at $V_{DS} = 0.3$ V than that at $V_{DS} = 0.045$ V, as expected ($g_m = \mu C V_{DS}/L^2$); (ii) g_m^0 assumes approximately the same value near the source contact ($V_S = 0$ V) for both biases and is smaller near the drain contact for the larger V_{DS} bias of 0.3 V, due to a stronger drain field leading to less gate modulation in that region; (iii) g_m^0 is low just in the vicinity of the metal contacts, maximizes within 100 nm from either contact and then drops to the minimum toward the center of the channel. This latter effect is counter-intuitive, as one would anticipate that g_m^0 would be maximal near the source contact and decreases steadily as the source underlap length increases or the tip approaches the drain contact. A greater source underlap length reduces C_{GS} and increases R_{s2} both leading to reduction in g_m^0, the latter according to $g_m^0 = g_m/(1 + g_m R_{s2})$ with g_m being the intrinsic transconducatance.

Strong electron accumulation at the surface of InAs creates a thin tunnel barrier when InAs is contacted with most metals leading to ohmic contact behavior. Surface states however prevent strong modulation of free carriers in the channel. At the contact-NW interface, the conduction energy band edge is fixed at the metal contact and can be modulated (weakly due to surface states) in the semiconductor NW. When the AFM tip is within 50 nm from either metal contact, modulation of the conduction band edge is effective but cannot extend spatially far enough into the channel to form a wide enough energy barrier for injected/collected electrons. Potential screening from the bulk metal contact cannot be ruled out just in the vicinity of the metal contact. When the AFM tip is $\sim$100 nm away from either metal contact, modulation of the conduction band edge is the strongest and a spatially thick energy barrier can be formed in the vicinity of the injection/collection electrodes (see the energy band-edge insets at the left and right of figure 11(*b*)). Close to the center of the NW, modulation is the weakest as the conduction band edge is not fixed at 0 eV or $-qV_D$, similar to the situation at the device electrodes, and a strong energy barrier cannot be created (see the energy band-edge inset at the center of figure 11(*b*)). Indeed, 3D numerical simulations using the integrated system engineering (ISE) package [89] for a similar device architecture to that used in experiment have also shown moderately strong current modulation close to the NW contact, strongest modulation within 100 nm from the contact and weakest modulation near the center of the channel (figure 11(*c*)). We emphasize that this is the case here due to the strong presence of surface states in InAs NWs preventing strong gate modulation in the channel. A more passivated surface should result in a similar behavior to that described in point (iii) above. These SGM results are analogous to what have been obtained from CNTs due to Schottky barrier modulation in the latter [90]. These results suggest that placing the gate near the source electrode is most effective for a material such as InAs with high surface-state density.

The effect of potential screening (or fringing fields) from the metal contact to the NW is less likely to be revealed by SGM measurements because these measurements utilize dc

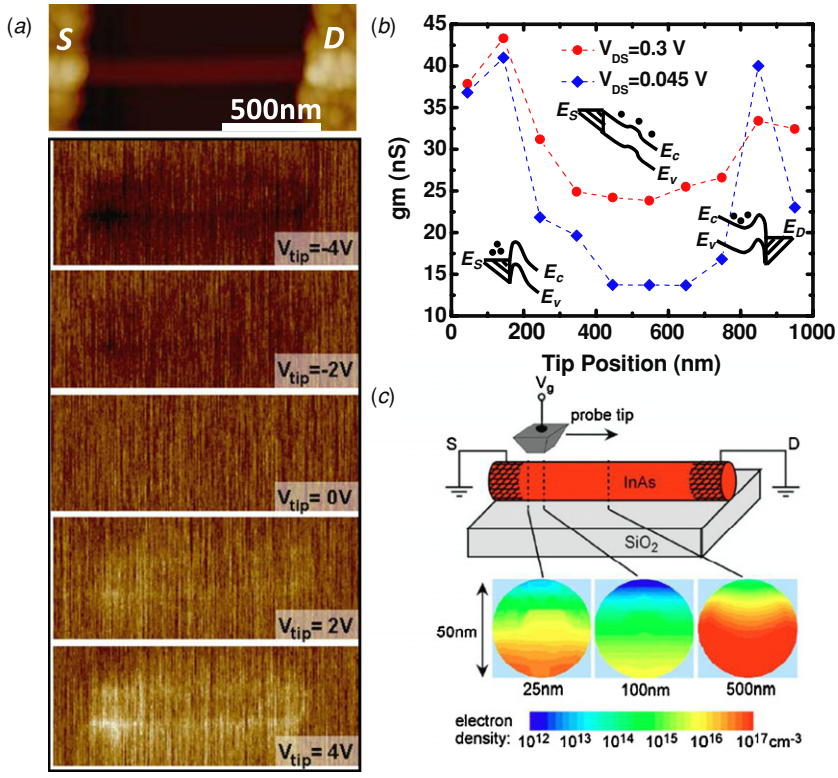

Figure 11. (*a*) Top panel is the AFM topograph of a 1 μm long and 45 nm diameter InAs NW channel utilized for the SGM measurements. Bottom five panels are SGM images of the NW current for tip voltages of -4, -2, 0, 2 and 4 V, obtained at a source-drain bias of $V_{DS} =$ 0.3 V. The dark and bright spots correspond to currents of 4.12 μA and 4.47 μA, respectively. The tip was scanned over all the areas shown here. (*b*) Plot of the transconductance measured from the current images at different locations along the channel of the NW at low (45 mV) and high (0.3 V) V_{DS} biasing. Small insets are energy-band diagrams illustrating injecting/collecting barrier modulation near source/drain and lower band-edge modulation near the center of the channel. (*c*) 3D numerical simulations of a material stack similar to that used in experiment presenting contour plots of the free-electron density in the NW channel at three different locations along its length. (Reproduced with permission from [84]. © 2007 American Institute of Physics.)

currents that are dependent on the barrier height and width in the vicinity of the metal contacts, which by themselves can be modulated by the probe tip potential as discussed above. Scanning capacitance spectroscopy (SCS), on the other hand, utilizes displacement currents and is typically used for profiling dopant distributions and field gradients at the nanoscale [91–93], and is more suitable for understanding the local electrostatic environment of a NW device. Law *et al* have used SCS to study fringing field effects of a metal contact to an InAs NW [85]. In the SCS experiment performed here, a dc bias is swept at the sample electrode with a superimposed sine wave (2 V, 45 kHz) for measuring the capacitance using the system's capacitance sensor. Since the sample capacitance is very small (∼aF range), a saw-tooth modulation voltage (0.5 Hz, 6–12 V varying amplitude) is superimposed onto the sine wave in order to measure small capacitance variations rather than the capacitance itself; $\partial C/\partial V$ spectra are then collected as the tip scans over the surface [94]. Similar to traditional MOS capacitor behavior, a non-zero $\partial C/\partial V$ signal indicates carrier modulation in the depletion regime, and a zero $\partial C/\partial V$ signal indicates no carrier modulation when the tip-sample system is biased in the accumulation or inversion regimes. Figure 12(*a*) shows an AFM topograph of the InAs NW subject of this study, and figure 12(*b*) shows a density plot of the SCS signal as a function of tip voltage and length separation between the tip and the metal contact. For these SCS spectra, the probe tip was positioned at the apex of the NW/oxide and full spectra of $\mathrm{d}C/\mathrm{d}V$ were measured. The probe was then moved 100 nm and repositioned over the apex of the NW/oxide and other spectra were taken. A bright region in figure 12(*b*) indicates carrier modulation in the InAs NW. It is evident from figure 12(*b*) that carrier modulation in the NW occurs at more negative voltages as the AFM tip departs from the metal contact, indicating a threshold voltage shift with distance from the contact.

To gain more quantitative understanding of capacitance variations with distance from the contact, the SCS signal is plotted in figure 12(*c*). In figure 12(*c*), one can observe the following: (i) in the vicinity of the contact up to 1 μm, no $\partial C/\partial V$ signal is observed with the experimentally assessable voltage range and correspondingly no carrier modulation occurs due to electrostatic potential screening from the contact; (ii) for the 1–3 μm separation from the contact, a negative shift in the peak of the SCS signal is observed as the distance from the contact increases indicating effective but less contact potential screening and slightly enhanced carrier modulation due to the applied dc bias; (iii) for the 3–6 μm separation, a weaker shift in the SCS signal and a sharper signal spectrum is observed indicating decreased contact potential screening effects. The tip voltage

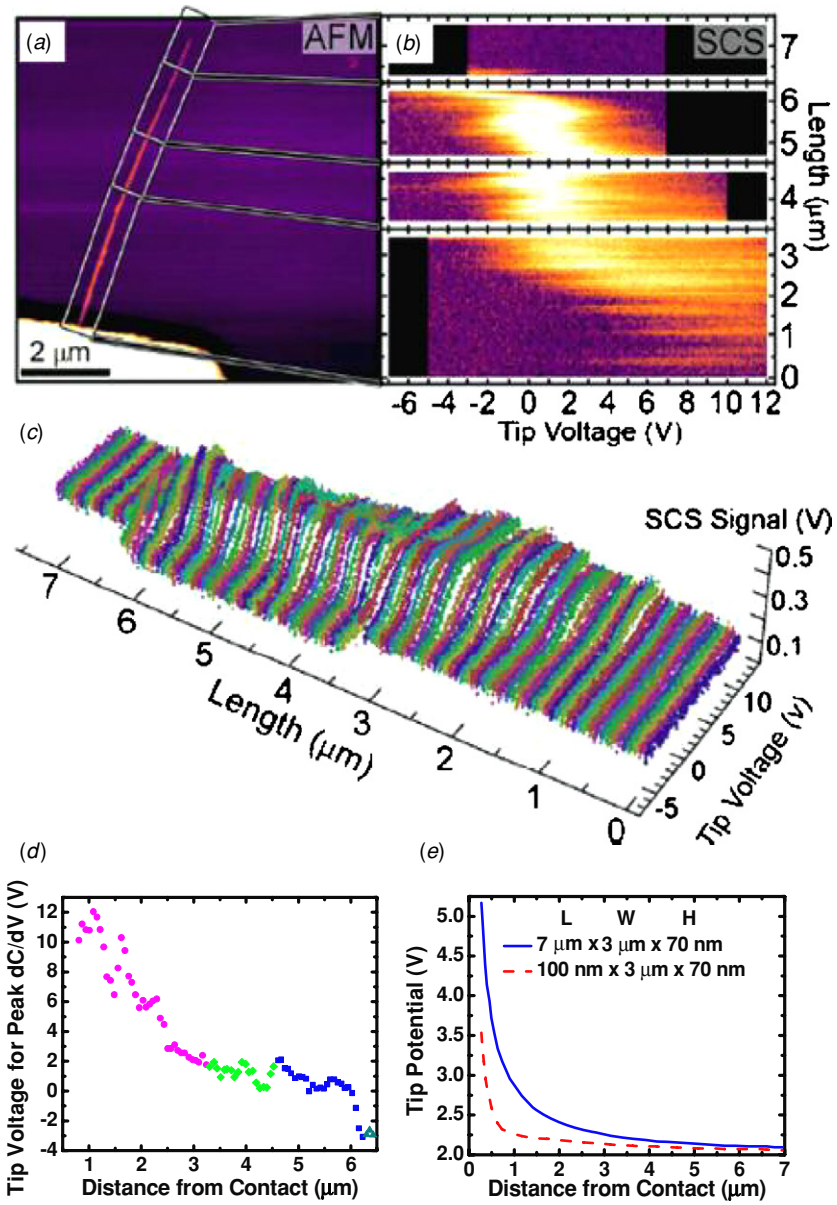

Figure 12. (*a*) AFM topograph of the NW device used in this SCS study. (*b*) Plot of the SCS signal as a function of tip voltage and separation from the metal contact. (*c*) Line cut profiles of the SCS spectra in (*b*) taken at 100 nm period. (*d*) Plot of the tip voltage at which a peak in the SCS spectra is observed. Different symbols correspond to the different regions in (*b*). (*e*) Simulated tip voltage required to produce a 2 V constant surface potential at the NW plotted as a function of distance from the metal contact for the case of two contact sizes where the lengths of the contact perpendicular to the wire axis were 7 μm and 100 nm. (Reproduced with permission from [85]. © American Institute of Physics.)

at which the peak in the SCS signal was observed is plotted in figure 12(*d*) showing a rapid decrease of the required tip voltage to produce an SCS signal peak with distance from the contact. This figure conveys that electrostatic screening from the metal contact can lead to a threshold voltage shift in the NW, as has been suggested by Guo *et al* [95]. Law's finite element numerical simulations for a similar device architecture using COSMOL MULTIPHYSICS simulation package confirm these experimental results. Figure 12(*e*) shows a plot of the required tip voltage to produce a constant surface potential of 2 V with distance from the metal contact. The contact bias is kept at 0 V. It is evident from figure 12(*e*) that the required tip potential to produce the 2 V surface potential on the NW exhibits a rapid increase with $e^{1/x}$ dependence as the tip approaches the metal contact with 7 μm $\times$ 3 μm $\times$ 70 nm dimensions. With a smaller contact of 100 nm $\times$ 3 μm $\times$ 70 nm, potential screening from the metal contact has the same functional dependence whose magnitude is greatly reduced as indicated by the dashed line in figure 2(*e*). These results compliment Guo *et al*'s predictions on the parasitic effects of microscopic contacts to 1D NWs and reveal that such effects extend several microns across the NW length which highlights the importance of reducing the metal contact size to reduce screening effects while maintaining a reasonable contact resistance which starts to increase for a

contact width, W, below the contact transfer length, L_T, with $\coth(W/L_T)$ dependence [96].

5. Performance assessment of InAs nanowire FETs

The results discussed in section 3 confirm that InAs NWs possess high electron mobility and are capable of delivering high current densities. To assess the performance of InAs NWFET devices among other NWFETs, we discuss a number of the most significant results in VLS-synthesized NWFETs and compare them to top-down processed NWFETs and planar CMOS FETs. Even though our devices were fabricated for basic transport measurements, nonetheless, we include their results in this performance assessment. To do so, we utilize a number of the benchmarking metrics introduced by Chau *et al* [97], and by Cohen *et al* [98]. In particular, we use the method of Chau *et al* for calculating the I_{on}/I_{off} ratio (when not stated in the original paper) by considering the I_{on} current at $V_T + 2/3\ V_{DD}$ and I_{off} at $V_T - 1/3\ V_{DD}$. When comparing the NW to planar CMOS performance, several researchers have normalized the on-state currents and transconductances to either the NW diameter or the NW perimeter. In addition to the error introduced to the gate width by doing so, this method does not account for oxide-equivalent-thickness differences between devices under comparison and their channel lengths. Cohen *et al* have used a new metric for this comparison, namely $I_{on-norm} = I_{on}L_g/C(\mathrm{A}\cdot\mathrm{cm}^2/\mathrm{F})$ which takes into account geometrical and material differences in device comparison, where C is the NW capacitance per unit length.

Table 1 shows a summary of various FET figures of merit for devices and materials under consideration. This includes NWFETs fabricated from bottom-up synthesized Si NWs [98], Ge–Si core-shell NWs [99], Ge–Si core-shell NWs with silicided nano contacts [100], InAs NWs [101], top-down processed Si NWs [102] and planar CMOS FET [98]. The device materials and physical dimensions are also included in table 1 and the figures of merit compare as follows.

(a) *Mobility*: for p-type FETs, Ge cores with ∼25 nm diameter and ∼2 nm Si shells have shown hole mobility values of ∼640 $\mathrm{cm}^2\ (\mathrm{V\ s})^{-1}$. This high hole mobility value was attributed to the formation of a hole gas at the Ge–Si interface [103]. This, however, is still lower than CVD grown strained Ge on $Si_{0.5}Ge_{0.5}$ which have shown hole mobility values of ∼1700 $\mathrm{cm}^2\ (\mathrm{V\ s})^{-1}$ for 12 nm Ge epitaxial layers [104]. For n-type FETs, InAs NWs have shown room temperature mobility values in excess of 10 000 $\mathrm{cm}^2\ (\mathrm{V\ s})^{-1}$, estimated through simulation [101]. Mobility values in InAs NWs in excess of 10 000 $\mathrm{cm}^2\ (\mathrm{V\ s})^{-1}$ have been measured by us as discussed in the previous sections.

(b) *Normalized on-current ($I_{on-norm}$)*: our back-gate twinned WZ InAs NWFET (figure 10(*d*)) exhibits the highest $I_{on-norm}$ when compared to all other devices. Our ZB NWFET (figure 10(*c*)) even exhibits a higher $I_{on-norm}$ value of $2.67 \times 10^4\ \mathrm{A\ cm}^2\ \mathrm{F}^{-1}$. For the InAs surround gate NWFET fabricated at Lund University, $I_{on-norm}$ does not account for the underlap regions of the channel length, i.e. the ungated NW regions between the source and the drain, which are several times larger than L_G. These underlap regions contribute to a significant series resistance. The bottom-up synthesized Si NWs have shown a remarkably high $I_{on-norm}$ when compared to Ge–Si core-shell devices, as well as when compared to bulk n-FET fabricated at IBM with similar gate length and dielectric thickness [98]. It is worth to note that p-type Si NWFETs have shown the best p-type performance. Cohen *et al* attributed this high performance to the low ohmic contact resistance obtained in these NWs by ion-implantating the source and drain regions.

(c) *Normalized transconductance (g_{m-norm})*: our back-gate twinned WZ InAs NWFET also exhibits the highest g_{m-norm} among all other devices. P-type Ge–Si core-shell NWs also show high g_{m-norm} partly due to the use of the thin high-k HfO_2 dielectric, and due to the passivated Ge core surface by the crystalline Si shell. g_{m-norm} of Lund's InAs NWFET lags behind all other devices due to the presence of the underlap regions that reduce the transconductance as discussed in earlier sections (2 and 4).

(d) *Inverse sub-threshold slope (SS^{-1})*: Near-ideal inverse subthreshold slope (60 mV/decade) was obtained from VLS and top-down Si NWFETs (for both p-type and n-type) and decent ones were obtained from Ge-Si and Lund's InAs NWFETs. Our back-gate twinned WZ NWFET shows the poorest SS^{-1} due the use of the Si carrier as back-gate with a thick 100 nm SiO_2 dielectric layer. The decent SS^{-1} in top-down Si NWFETs is not surprising because of the superior quality of the SiO_2/Si interface compared to all others. The inverse subthreshold slope of Lund's InAs NWFETs is comparable to that obtained for Ge-Si core-shell NWs and is encouraging provided the surface-state bottle-neck problem for III-V FETs. One can improve over these inverse subthreshold slopes by exploiting band-to-band tunneling in tunnel or impact ionization FETs that allow subthreshold slopes that are substantially less than 60 mV/decade. Recently, Björk *et al* have demonstrated a 6 mV/decade inverse subthreshold slope in vertical Si NWFETs at room temperature [105]. However, the presence of tunnel barriers in such devices leads to reduction of on-state currents when compared to conventional FETs.

(e) *Drain-induced barrier lowering (DIBL):* DIBL that accounts for short channel effects is superior for Si NWFETs when compared to all other devices, particularly for the Si VLS NWFET when compared to Ge–Si. Lund's surround gate InAs NWFET with extension regions has shown a decent DIBL but at the expense of transconductance and on-currents as indicated above.

(f) *I_{on}/I_{off} ratio*: Si NWFETs have shown the highest I_{on}/I_{off} ratios when compared to other devices in table 1 due to the larger band-gap of Si (1.12 eV) when compared to Ge (0.64 eV) and InAs (0.35 eV) with poor performance for the back-gate InAs and Ge–Si core-shell wires. It is likely that Lund's InAs NWFET showed better turn-off characteristics due to their surround gate geometry when compared to the Ge–Si NWFETs with top or omega-gate

Table 1. Comparison of FET device performance for a sample of bottom-up NWs (a–e), a Si top-down NW (f) and a planar CMOS n-FET (a).

	Si[a] bottom-up (top-gate)	Ge–Si[b] bottom-up (top-gate)	Ge–Si[c] bottom-up (top-gate)	InAs[d] bottom-up (surround-gate)	InAs[e] bottom-up (back-gate)	Si[f] top-down (surround-gate)	Si[a] planar
Orientation	⟨1 1 2⟩	⟨1 1 0⟩	⟨1 1 0⟩	⟨0 0 0 1⟩	⟨0 0 0 1⟩	–	–
Polarity	n	p	p	n	n	n	n
D (nm)	17	27	16	50 ± 10	61	10	–
L_G (nm)	515	190	40	50	3380	130	515
Oxide	SiO_2	HfO_2	HfO_2	HfO_2	SiO_2	SiO_2	SiO_2
t_{ox} (nm)	7.4	4	4	10	100	5	7.4
V_{DS} (V)	1	1	0.5	0.5	0.5	1.5	–
μ_{FE} (cm^{-2} $(V\ s)^{-1}$)	>300	640	–	>10 000	2000	600	–
$I_{on-norm}$ ($A\ cm^{-2}\ F^{-1}$)	>200	88	75.5	6.45	420	43	∼90
g_{m-norm} ($S\ cm^{-2}\ F^{-1}$)	–	143	45.5	8.34	645	–	–
S.S. mV/decade	63–75	100	140	100 ± 8	7.6×10^3	72–74	–
DIBL (mV/V)	<10	1450	1000	60	–	4–12	–
I_{on}/I_{off}	$\sim 10^5$	∼10	$<10^2$	10^3	∼2	$>10^8$	–

[a] [98]
[b] [99]
[c] [100]
[d] [101]
[e] Calculated for the back-gate twinned WZ device of figure 10(*d*).
[f] [102]

geometry (not fully conformal). Our back-gate twinned WZ InAs NWFET also showed a poor I_{on}/I_{off} ratio due to the back-gate geometry. The approximate five orders of magnitude current modulation in figure 10(*d*) occurs over a large back-gate voltage range compared to those used in the assessment metrics here (I_{on} at $V_T + 2/3\ V_{DD}$ and I_{off} at $V_T - 1/3\ V_{DD}$).

This comparison indicates great potential for InAs NWs for high mobility and high on-current devices suitable for high-speed nanoelectronics applications; however, their potential is not yet fully exploited. The key remaining challenges for attaining optimal FET performance from InAs NWFETs include optimization of the device geometry for high-performance FET operation, surface-state passivation and elimination of polymorphism in n-type InAs NWs.

6. Integration to Si technology

In the previous sections, we discussed detailed characterization techniques to assess charge transport and FET performance for InAs NWs. In order to make use of the novel properties of InAs NWs, one needs to consider their integration into useful circuits and systems in addition to the challenges outlined above for obtaining enhanced FET performance for InAs NWs. An integration scheme that makes use of advancements in Si technology is preferred, thereby allowing direct integration of InAs with Si. We discuss here our approach in integrating vertical arrays of electrically isolated InAs NWs with Si.

Despite the numerous proposed integration schemes in the literature [106–114], the most interesting are those which utilize epitaxial NW growth to exploit dense vertical integration of NWs into 3D device architectures. This is traditionally accomplished by the epitaxial growth of NWs on their respective substrates with e-beam or nano-imprint patterning techniques [115]. Aimed at integrating III–V NWs to Si, researchers have successfully grown vertically aligned III–V NWs directly on Si substrates [116–119]. These approaches however do not provide electrical isolation between NW devices which is required for multi-device operation on a single chip. Further, the nature of energy band-edge alignment at the Si/III–V interface is not well understood, and its implications on charge transport are still under investigation [120]. We took a different approach to bring together the potential of vertical isolated 3D device architectures with the integration to Si substrates by using the smart-cut® technique to transfer thin III–V layers to SiO_2/Si surfaces and perform ordered vertical growth afterward (figure 13(*a*)) [121]. Details on the smart-cut® technique can be found elsewhere [122]. In brief, a donor InAs substrate is implanted with hydrogen ions at a predetermined projected depth. The donor substrate is then thermally bonded to a SiO_2/Si surface at moderate temperatures, and the temperature is further increased to allow H_2 bubble formation at the projected depth in the donor InAs wafer causing exfoliation from the bonded structure. With wet etching and thin film regrowth for planarization of the bonded InAs surface, NW growth from Au colloids becomes feasible (figure 13(*a*)) [121].

For ordered growth, we used e-beam lithography to pattern Au dot arrays with 4 μm pitch on the transferred and planarized InAs layer on SiO_2/Si. OMVPE growth of InAs NWs resulted in vertical ordered NW growth similar to that on the InAs(1 1 1)B bulk surface. When followed by another e-beam lithography step to mask disks with 2 μm diameter centered around the InAs NW, wet chemical etching resulted in isolating these NWs as shown in figure 13(*b*). A zoom-in to the cross-section of one of these NWs shows an InAs NW atop an InAs island on the SiO_2 surface (figure 13(*c*)). The InAs island can serve as an ohmic bottom contact to the NW structure and processing of a vertical NWFET would then

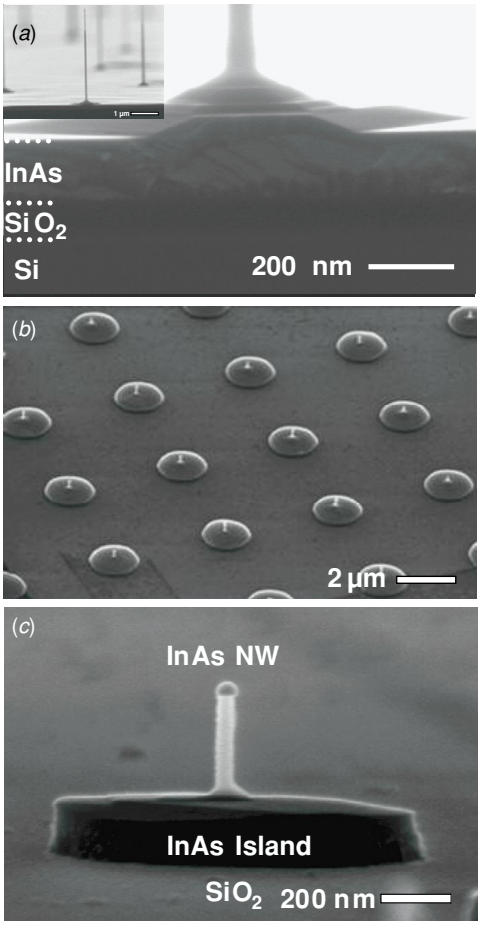

Figure 13. (*a*) 85° cross-sectional FE-SEM at the base of an InAs NW grown on $InAs/SiO_2/Si$ showing different contrast from the different layers. Inset is a larger field of view FE-SEM image. (*b*) 45° angle-view FE-SEM images of vertical and electrically isolated InAs NWs on SiO_2/Si. (*c*) Zoom-in FE-SEM image of an InAs NW with an InAs island at its base, sitting on a SiO_2 substrate and electrically isolated from other NWs suitable for individual NW addressing. (Reprinted with permission from [121]. © 2009 American Institute of Physics.)

proceed in a process similar to that of Thelander *et al* [101] While this novel approach allowed the vertical integration and electrical isolation of InAs NWs to Si, the requirements on the quality of the donor substrate surface are very stringent (less than 0.5 nm rms surface roughness for donor and acceptor surfaces). Transfer of patterned donor layers is feasible and perhaps can help in enabling the transfer of layers with lower surface quality [123].

7. Conclusions

In this paper, we overviewed our work on electron transport studies in InAs NWs obtained from characterization of NWs in a variety of device schemes. Direct observation of ballistic transport in InAs NWs over a length scale of the order of ∼200 nm was demonstrated, highlighting the potential of InAs NWs for high-speed applications. A simple model that accounts for parasitic device components in transport coefficient extraction was introduced, and high field-effect electron mobility in InAs NWs was computed. This model allows accurate extraction of free carrier mobility and concentration in semiconductor nanowires. Surface-state effects on current transport and parameter extraction from NW FETs were discussed and quantified. We showed that surface states have detrimental effects on electron transport in NWs which when measured with different sweep rates may lead to artifacts in parameter extraction. Scaling effects of the NW diameter on transport behavior and transport coefficients were explored and the implications of Fermi-energy pinning at the NW surface were highlighted. We showed by experiment and numerical simulations that reduction in nanowire diameter leads to reduced electron mobility and increased free-electron density for the case of InAs where the Fermi energy is pinned in the conduction band. The field effects on transport properties were isolated and discussed and the effects of high injection fields on mobility reduction and morphology changes were overviewed. We highlighted the effects of lateral fields on mobility degradation and used *ex situ* TEM measurements to study morphological changes to NWs exposed to high injection fields. The failure length in these NWs showed to be in agreement with estimated ballistic length and with highest temperature spots in the NW channel from electro-thermal simulations. The correlation of a crystal structure with NW transport properties and the impact of spontaneous polarization charges in WZ crystals on charge transport in III–V NWs were introduced. By utilizing numerical simulations, we inferred that these spontaneous polarization charges in twinned WZ NWs are responsible for enhancing the sub-threshold characteristics of NWFETs made of these NWs. Scanning probe studies on nanoscale transport behavior in InAs NWs were overviewed. Local transconductance and electrostatic variations in typical device configurations were presented highlighting the importance of injection/collection barrier modulation as well as potential screening in 1D structures. The current status and performance of NWFETs were analyzed and compared for different material NWFETs. While InAs NWs show great promise in terms of mobility, on-currents and transconductances, optimization of short channel effects and surface passivation for lower off currents is needed. Finally, a novel integration scheme of vertical, yet electrically isolated III–V NWs to Si substrates was introduced. It is our hope that these studies have enabled better understanding of electron transport in InAs NWs, provided a fair assessment of their performance, and presented the forthcoming challenges for this technology.

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