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High Electron Mobility InAs Nanowire Field-Effect Transistors

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Single-crystal InAs nanowires (NWs) are synthesized using metal–organic chemical vapor deposition (MOCVD) and fabricated into NW field-effect transistors (NWFETs) on a SiO_2/n^+-Si substrate with a global n^+-Si back-gate and sputtered SiO_x/Au underlap top-gate. For top-gate NWFETs, we have developed a model that allows accurate estimation of characteristic NW parameters, including carrier field-effect mobility and carrier concentration by taking into account series and leakage resistances, interface state capacitance, and top-gate geometry. Both the back-gate and the top-gate NWFETs exhibit room-temperature field-effect mobility as high as 6580 $cm^2 V^{-1} s^{-1}$, which is the lower-bound value without interface-capacitance correction, and is the highest mobility reported to date in any semiconductor NW.

Keywords:
- electron mobility
- field-effect transistors
- nanoelectronics
- nanowires

1. Introduction

Semiconductor nanowires are very attractive and versatile building blocks for future electronic systems because of the unique possibilities they offer for the rational control of fundamental properties such as dimension, composition, and doping during growth.[1,2] A wide range of nanowire (NW)-based devices and systems, including transistors and circuits,[3–5] light emitters,[6–9] and sensors,[10] have been explored. Nanowire field-effect transistors (NWFETs) have been of particular interest recently, both as vehicles for the investigation of basic carrier-transport behavior and as potential future high-performance electronic devices. NWFETs fabricated from group IV,[11–13] III–V,[3,14–16] and II–VI[17,18] semiconductors and conductive oxides[19] have demonstrated promising FET characteristics in top-gate,[11,12,15] back-gate,[3,14,15] and surround-gate[16,18] FET geometries. InAs in particular is an attractive candidate for NW-based electronic devices because of its very high electron mobility at room temperature[20] and its surface Fermi-level pinning in the conduction band,[21] which lead to the formation of an electron surface accumulation layer[22] and allow straightforward formation of low-resistance ohmic contacts.[23] Indeed, resonant tunneling diodes,[24] single-electron transistors,[25] and Josephson junctions[26] have been implemented using InAs NWs and InAs/InP NW heterostructures with carrier mobilities in the range of 200–3000 $cm^2 V^{-1} s^{-1}$.[16,25]

Herein, we report room-temperature studies of depletion-mode InAs-based NWFETs with both global back-gate and underlap (i.e. nonzero spacing to source/drain electrodes) top-gate geometries. We also present a circuit model for top-gate FETs that takes into account the contact, series and leakage resistances, interface-state capacitance, and top-gate geometry-defined capacitance to assure accurate parameter extraction for such structures from device measurements. We have analyzed the InAs NWFETs using this new model and the conventional back-gate NWFET model. In

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both cases, we obtained field-effect electron mobility values significantly higher than those reported to date for other semiconductor NWs.

2. Results and Discussion

The as-grown InAs nanowires on a SiO_2/n^+-Si substrate were 30–75 nm in diameter and 20–30 μm long, as shown in the representative scanning electron microscopy (SEM) image (Figure 1 a). The InAs NWs were single-crystal Wurzite with the growth axis in the [110] direction, as shown in the high-resolution transmission electron microscopy (HRTEM) image (Figure 1 b).

The InAs NWFET devices were then fabricated using electron-beam lithography (EBL) with Ti/Al source and drain electrodes and a SiO_x/Au top-gate electrode. The n^+-Si substrate served as a global back gate. Figure 2 a shows the schematic of an underlap top-gate NWFET device. Careful consideration of the device geometry of this structure suggests the need for an analysis that extends beyond those employed previously[3,12–14,16,18] in order to extract key characteristic nanowire parameters, such as mobility and carrier concentration. Specifically, we have taken into account the contact resistance, the resistance of the ungated NW regions between the source/drain and gate electrodes, and the unmodulated NW volume underneath the gate, which are important factors that have not been accounted for in prior reported studies. Because the Fermi level is pinned in the conduction band at the InAs surface, the ungated portions of the NW remain conducting with no band bending under top-gate bias, as illustrated in Figure 2 b; the resistance of each NW section should therefore be calculated separately to analyze device current–voltage characteristics. We thus define two series resistances R_{s1} and R_{s2}, each of which includes the contact resistance and the resistance of the corresponding ungated NW segments. The unmodulated portion of the nanowire underneath the gate gives rise to a current-leakage path that is constant for a wide range of negative gate voltages and can be described by a leakage resistance, R_{leak}, which can be obtained from the lowest measured current in the device, I_{leak}. The gate-leakage current through the thick oxide is negligible so that the gate-leakage resistance is not included in this model. Figure 2 c shows the resulting equivalent circuit model employed in our analysis; V_{DS}^0 and V_{GS}^0 are the applied source–drain and gate–source voltages, respectively, and I_{DS}^0 is the measured source–drain current. V_{DS}, V_{GS} and I_{DS} are related to the active transistor portion of the device.

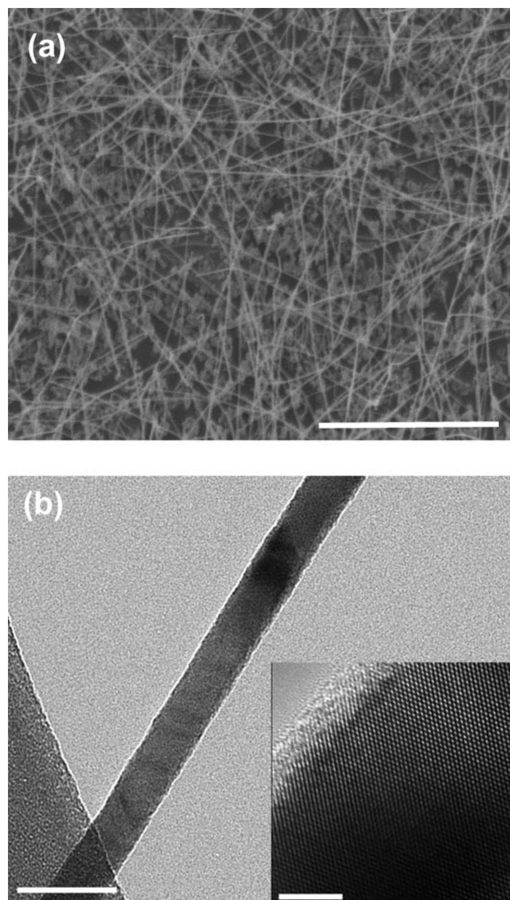

Figure 1. a) SEM image of InAs nanowires on a SiO_2 substrate. Scale bar is 20 μm. b) TEM image of an InAs nanowire. Scale bar is 50 nm. The inset is a HRTEM image of the same single-crystal InAs nanowire. Scale bar is 5 nm.

The resistances of the InAs NWs were measured from devices fabricated with source–drain separations that varied from 0.5 to 4 μm in the same processing run, and without a top gate, the extrapolation to a source–drain separation of zero yielded an ohmic contact resistance in the range of 1–10 kΩ (see Supporting Information). As a conservative estimate in the computation of the mobility, a contact resistance of 1 kΩ has been used; this assumes the highest possible NW-resistance values. Numerical calculation to determine the number of confined modes in the InAs nanowires by solving Schrödinger's equation in cylindrical coordinates[27] yields the occupation of 10 modes for the carrier densities calculated in these wires (as discussed later), which in turn results in a contact resistance of 1.3 kΩ due to the mismatch in the one-dimensional (1D, NW) and 3D (metal contact) density of states.[28] This result suggests, as expected, the absence of a significant Schottky barrier at the Al-Ti/InAs interface.

In the linear operating region,[19] the accumulation charge is given by $Q_{acc}=C(V_{GS}-V_t)$, where C is the gate capacitance and V_t is the threshold voltage. The source–drain current, I_{DS}, can then be derived as:

$$I_{DS} = \int qnvdA = \mu_{FE} Q_{acc} V_{DS}/L_G^2 = \mu_{FE} C(V_{GS} - V_t) V_{DS}/L_G^2 \quad (1)$$

where q is the electron charge, n is the electron concentration, v is the drift velocity, μ_{FE} is the field-effect mobility, L_G is the gate length, and A is the cross-sectional area of the NW. Ballistic effects are expected to be negligible for the lengths of nanowire reported in this paper; numerical computations indicate a mean free path of ≈50 nm and scanning

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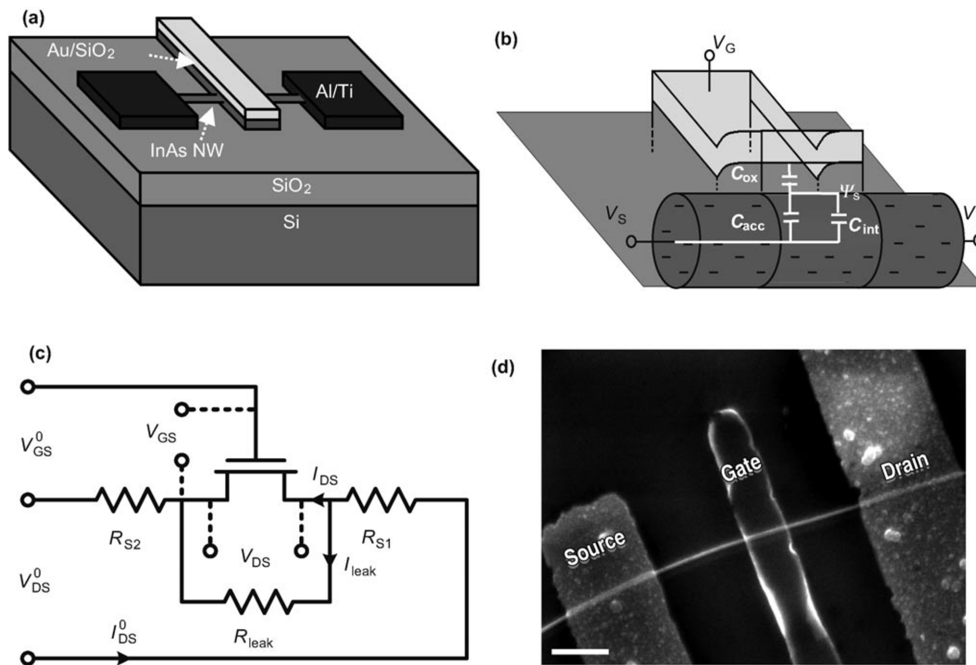

Figure 2. a) Schematic of the underlap NWFET fabricated on an oxidized Si substrate with 85/15 nm Al/Ti as the source and drain contacts, respectively, and 100/100 nm Au/SiO_x as the top-gate electrode and dielectric, respectively. b) Schematic of the underlap top-gate NWFET and its equivalent capacitance circuit. c) DC circuit model of the underlap top-gate NWFETs. d) SEM image showing the "ungated" regions between the source and the drain that contribute to series resistances. Scale bar is 1 μm.

probe microscopy (SPM) measurements on NWs grown and fabricated together with the devices we report in this paper have demonstrated ballistic or nearly ballistic transport only over distances of up to 200 nm, much shorter than the gate lengths employed here.[27,29]

The gate capacitance, C, is critical in obtaining the field-effect mobility. The dielectric capacitance of a top-gate NWFET is difficult to determine precisely because of the curved gate geometry and the dependence of the curvature on the oxide thickness, and the wire-to-plate capacitance model used for back-gate NWFETs is not applicable. For back-gate NWFETs and nanotube FETs, the general form of capacitance is:

$$C = 2\pi\varepsilon L_G / \ln\left[\left(t_{ox} + a + \sqrt{(t_{ox}+a)^2 - a^2}\right)/a\right] \quad (2)$$

where L_G is the gate length, ε is the insulator dielectric constant, t_{ox} is the gate insulator thickness, and a is the nanowire radius; this can be reduced to $C = 2\pi\varepsilon L_G/\ln\left(\frac{2t_{ox}}{a}\right)$, when $t_{ox} \gg a$. These equations are applicable to degenerately doped NWs and have been used extensively elsewhere[3,14,16–18]. For top-gated NWFETs employed in this work, a 2D device simulator[30] was used to compute the capacitance between the metal gate and the InAs NW, and it was found that the capacitance calculated using Equation (2) is underestimated by ≈10–14% when compared to the numerically computed capacitance; for an oxide thickness of 100 nm used in our devices, the error in using Equation (2), or its approximation, is ≈13%. Use of the wire-to-plate capacitance model would therefore lead to an overestimate of ≈10–14% compared to the values calculated using the numerically simulated capacitance of μ_{FE}.

An additional contribution to C may arise due to the unavoidable presence of surface states in InAs.[31] To take surface and interface states into account, in analogy with a conventional metal oxide semiconductor field-effect transistor (MOSFET),[32] an interface capacitance, C_{int}, is introduced in parallel with the accumulation capacitance, C_{acc}, for the depletion mode InAs NWFET, as shown in Figure 2b.. The modulated electron-charge density will then be:

$$\Delta Q_{acc}/A = \Delta\Psi_s C_{acc} = \Delta V_{GS} C_{ox}/(1 + C_{int}/C_{acc} + C_{ox}/C_{acc}) \quad (3)$$

where Ψ_s is the surface potential at the InAs/SiO_2 interface, A is the area, and all capacitances are in F cm^{-2}. $C_{ox}/C_{acc} = (\varepsilon_{ox}/\varepsilon_{InAs})(t_{acc}/t_{ox})$ is negligible in the planar approximation due to the dielectric constant difference and the large oxide thickness. A value of $\varepsilon_{ox} = 3.31$ was determined experimentally for a sputtered SiO_2 layer from the same target; $\varepsilon_{InAs} = 15.1$[20] and t_{acc} and $t_{ox} = 100$ nm are the accumulation layer and oxide thicknesses, respectively, with $t_{acc} \ll t_{ox}$. The accumulation capacitance can be expressed as $C_{acc} = Q_{acc}/bV_t$, where $b = 2$ for planar-enhancement-mode MOSFETs,[32] and can be approximated as $C_{acc} = \varepsilon_{InAs}/t_{acc}$ where t_{acc} is the separation of the accumulation charges from the surface of the nanowire due to quantum-mechanical confinement. The interface-state capacitance can be expressed as $C_{int} = qD_{it}$ where D_{it} is the interface-state density

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small

in units of $cm^{-2}eV^{-1}$, distributed over an energy range within the energy bandgap of InAs. The interface-state density and its energy distribution have not yet been studied for NWs in general nor for InAs NWs in particular. If a surface-state density of $5\times10^{12}\,cm^{-2}eV^{-1}$ (eg., $10^{12}\,cm^{-2}$ for an energy range of 0.2 eV) and even a very small value t_{acc} of 3 nm are assumed, then $C_{int}/C_{acc} = 0.2$. Thus, the term C_{int}/C_{acc} may not be negligible and has to be taken into account for accurate nanowire field-effect mobility calculations. However, the mobility values reported in this paper do not take into account the interface-charge-capacitance correction and are thus the lower-bound mobility values.

Straightforward circuit analysis is employed in Figure 2c to relate the quantities appearing in Equation (1) to the quantities applied at the physical electrodes of the nanowire device. Using the accumulation capacitance from Equation (3), a field-effect mobility equation can then be derived from Equation (1) as:

$$\mu_{FE} = \frac{L_G^2 V_{DS}^0 (1 + C_{int}/C_{acc})/C}{[(V_{DS}^0 - I_{DS}^0 R_s)^2/g_m^0 - (I_{DS}^0)^2 R_s^2 R_{s2} - V_{DS}^0 R_{s2}(V_{DS}^0 - 2I_{DS}^0 R_s)]} \quad (4)$$

where $g_m^0 = \partial I_{DS}^0 \partial V_{GS}^0$ is the extrinsic transconductance. If the series resistances and effects of interface states are neglected, Equation (4) simplifies to:

$$\mu_{FE} = g_m L_G^2 / C V_{DS} \quad (5)$$

which is the usual expression employed to determine carrier mobility in nanowires.

Representative I_{DS}^0 versus V_{DS}^0 plots are shown in Figure 3a for gate voltages $V_{DS}^0 = -2$, 0, and +2 V, which reveals that the InAs nanowires are highly conductive with low ohmic contact resistance. The extrinsic transconductance, g_m^0, obtained from the slope of I_{DS}^0 versus V_{GS}^0 in the linear region (Figure 3b), is 3 μS, from which the field-effect mobility can be calculated, using Equation (4), to be 6580 $cm^2V^{-1}s^{-1}$, which is the highest room-temperature field-effect mobility reported to date in any semiconductor NWFET. It should be noted that these NWFET devices exhibit hysteresis in their I_{DS}–V_{GS} characteristics (Figure 3b) that could alter the obtained extrinsic transconductance by a considerable amount (6 to 50%). We have used the lowest obtained transconductance in the mobility values reported in this paper. A detailed analysis of the hysteresis and measurement time-delay effects will be reported elsewhere.

One can also extract the current voltage characteristics, I_{DS}–V_{GS}, intrinsic to the InAs NWFET device using circuit analysis, as shown in Figure 2c. This is shown in Figure 3c and d with the applied voltages corresponding to those in Figure 3a and b, respectively. The potential drop across the series resistances lowers V_{DS} across the active portion of the NWFET device. As the source–drain current I_{DS} increases with applied V_{GS}^0, the measured current I_{DS}^0 increases, causing more potential drop across the series resistances. Hence, V_{DS} decreases with increasing V_{GS}^0, unlike the fixed V_{DS}^0 applied to the physical electrodes of the device, and causes a decrease in I_{leak}. The intrinsic transconductance is calculated to be $g_m = \partial I_{DS}/\partial V_{GS} = 7.7$ μS. The differential transconductance can be incorporated along with V_{DS} into $\mu_{FE} = g_m L_G^2/CV_{DS}$ to yield mobility values of (6200±1900) $cm^2V^{-1}s^{-1}$ for the same device discussed above. These mobility values extracted using this conventional technique are quite consistent with those extracted using Equation (4).

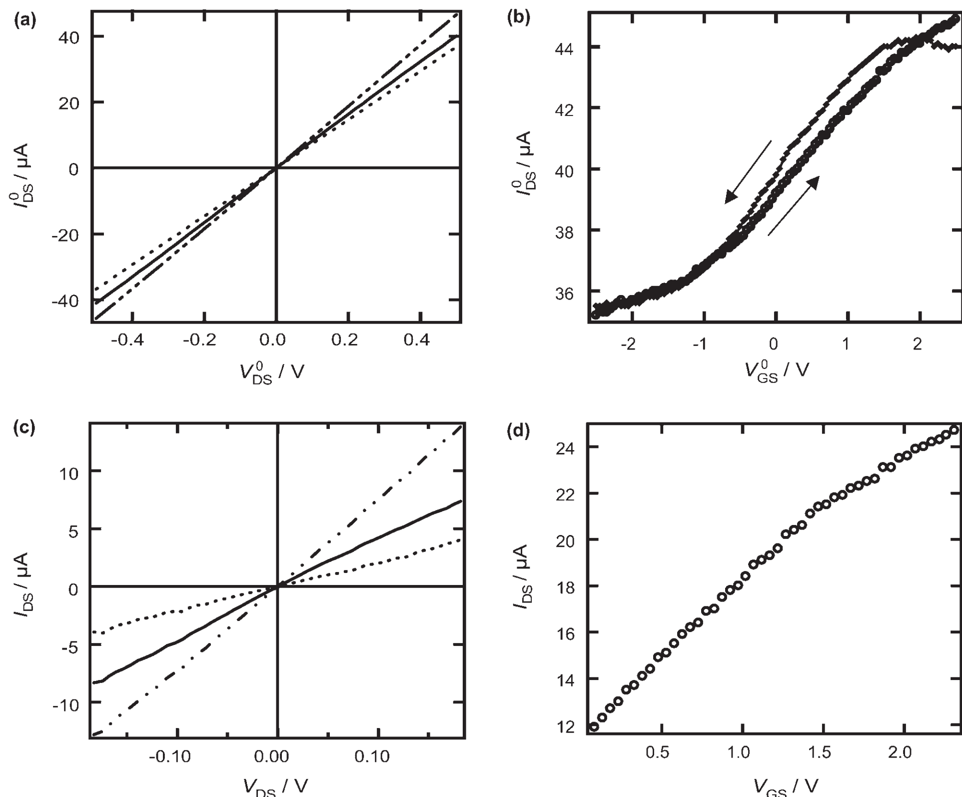

Figure 3. a) Graph of I_{DS}^0 versus V_{DS}^0 for $V_{GS}^0 = -2$ V (----), 0 V (——), and +2 V (———----) of a representative top-gate InAs NWFET. b) Graph of I_{DS}^0 versus V_{GS}^0 at $V_{DS}^0 = 0.5$ V of the same InAs NWFET. The arrows indicate the direction of the gate sweep with a sweeping rate of 2.7 Vs^{-1}. c) Graph of I_{DS} versus V_{DS} for the active portion of the NWFET device, extracted from (a). $V_{GS}^0 = -2$ V (----), 0 V (——), and +2 V (–•–•). d) Graph of I_{DS} versus V_{GS} for the top-gate NWFET, extracted at $V_{DS}^0 = 0.5$ V for the same device. Device dimensions correspond to device F in Table 1.

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Table 1. Summary of some representative InAs NWFET parameters and calculated field-effect mobility.

NWFET	D [nm]	L_{SD} [μm]	L_G [μm]	L_{SG} [μm]	R_T [kΩ]	R_s [kΩ]	R_{s2} [kΩ]	g_m [μS]	I_{meas} [μA]	C^+ [fF]	C^* [fF]	μ^+ [cm^{2}V^{-1} s^{-1}]	μ^* [cm^{2}V^{-1} s^{-1}]
A	73	3.87	1.62	1.75	21.9	13.14	9.93	1.18	22.8	0.419	0.174	2630	2260
B	49	3.72	1.69	0.986	20.9	11.9	5.78	9.06	23.9	0.134	0.124	2070	1800
C	74	3.72	1.42	1.07	12.6	8.15	3.81	1.93	39.7	0.132	0.153	4800	4160
D	63	3.66	1.52	1.15	11.9	7.36	3.9	1.67	42.4	0.132	0.154	4070	3500
E	65	3.41	1.45	1.21	16	9.64	5.85	0.88	31.2	0.128	0.147	1830	1590
F	68	3.48	1.30	1.04	13.2	8.63	4.31	3.04	38	0.116	0.133	7500	6580
G	47	3.64	1.61	1.25	25.5	14.6	8.87	1.88	19.6	0.127	0.145	4320	3770

Table 1 summarizes the extracted field-effect mobilities of seven representative devices; the NW diameters (D), source–drain lengths (L_{SD}), gate lengths (L_G), and gate–source lengths (L_{SG}) were measured using SEM. R_T is the total device resistance and is equal to the sum of the NW resistance (R_{NW}) and the contact resistance (R_c). The total series resistance R_s can be calculated using $R_s = (R_T - R_c)(L_{SD} - L_G)/L_{SD} + R_c$. The source series resistance R_{s2} can be calculated using $R_{s2} = (R_s - R_c)L_{SG}/(L_{SD} - L_G) + R_c/2$. The measured current I_{meas} is that measured at $V^0_{DS} = 0.5$ V; C^+ is the capacitance calculated using Equation (2), μ^+ is the mobility calculated using C^+ and Equation (4); C^* is the numerically computed capacitance using Silvaco software, and μ^* is the mobility calculated using C^* and Equation (4). The field-effect mobility in these InAs nanowires is much lower than the bulk InAs mobility (33 000 cm^{2}V^{-1}s^{-1}) due to surface scattering but higher than that typically measured for the accumulated free-electron gas on the InAs surface (2000–3000 cm^{2}V^{-1}s^{-1}).[33,34] Such an intermediate value is expected, given the combination of surface and bulk electron transport likely to be present in these NWs. We anticipate that carrier mobility can be increased by surface passivation[13,35] or in heterostructure core/shell NWs.[15] Table 1 also lists the mobilities calculated using the capacitance given by the wire-to-plate model, which quantifies the discrepancy compared to those obtained using the numerical simulated capacitance.

The modulated carrier concentration in the NWFET channel underneath the gate can be calculated from Equation (1) and is given by:

$$\Delta n_{\mathrm{channel}} = \frac{I_{DS} L_G}{q \mu_{FE} V_{DS} A} \tag{6}$$

The typical calculated $\Delta n_{\mathrm{channel}}$ values are $\approx 10^{17}$–10^{18} cm^{-3} with a leakage carrier concentration $n_{\mathrm{leak}} \approx 10^{16}$–$10^{17}$ cm^{-3}. The entire carrier concentration n is expected to be the sum of these two quantities.

Finally, back-gate InAs NWFETs were also fabricated and back-gate measurements performed (Figure 4) to compare our top-gate model with the back-gate model and to enable a fair comparison of our results with carrier mobilities reported in other NW studies. A field-effect mobility of $\mu_{FE} = 2740$ cm^{2}V^{-1}s^{-1} was obtained using Equation (5) and the wire-to-plate capacitance model, and corresponds to a transconductance of 2 μS. This value is significantly higher than the mobility values reported for other NWs listed in Table 2 and is comparable to that of the free-electron gas on the InAs surface, which suggests an increased influence of surface states due to poor physical contact between the nanowire and the SiO_2 substrate compared to the top-gate NWFETs, and substantial gate coupling to the source and drain electrodes.

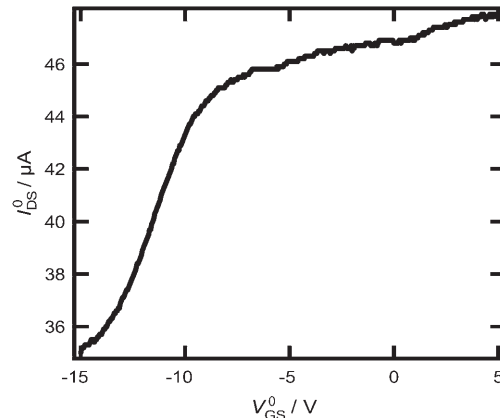

Figure 4. Graph of back-gate I_{DS}–V_{GS} at $V_{DS} = 0.5$ V for the same device shown in Figure 3.

Table 2. Comparison of different semiconductor NWFETs (nonpassivated nanowires).

NW	Carrier	μ [cm^{2}V^{-1}s^{-1}]	n [cm^{-3}]	J_{DS}[a] [A cm^{-2}]	I_{on}/I_{off}	Reference
Ge	h	600	3×10^{18}	$\approx 10^4$	10^3	11
Si	h	560		1.41×10^5	10^4	13
GaN	e	650	10^{18}–10^{19}	2.88×10^5		14
ZnO	e	13 ± 5	5×10^{17}	3.74×10^3	10^5–10^7	16
InAs	e	6200 ± 1900	10^{17}–10^{18}	10^6–10^7	2–100	This work

[a] At $V_{DS} = 0.5$ V and $V_{GS} = 0$ V, or the maximum available values.

3. Conclusions

In summary, we have fabricated and characterized underlap top-gate and global back-gate InAs NWFETs, and demonstrated the highest semiconductor nanowire electron mobility reported to date. For top-gate NWFETs, we have developed a model that allows a more accurate estimation of field-effect mobility and carrier concentration in semiconductor nanowires by taking into account series and leakage resistances, interface-state capacitance, and top-gate geometry for oxide-capacitance calculation. In particular, we have

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derived a new mobility equation for the analysis of the underlap gate NWFET device. A peak mobility value of $6580\,cm^2V^{-1}s^{-1}$ at low drift fields of $\approx 1.5\,kV\,cm^{-1}$ was measured in a top-gate InAs NWFET, and measurements on several devices yielded a representative average mobility value of $\approx 3400\,cm^2V^{-1}s^{-1}$. Both values represent lower bounds on the calculated mobility, which are conservative estimates because 1) the lowest possible ohmic contact resistance was used; 2) the lower extracted transconductance from the hysteretic NWFET measurements was employed for mobility calculation, and 3) the effect of surface states has not been taken into account. These results demonstrate the promising potential of using InAs nanowires for high-speed nanoelectronics.

4. Experimental Section

The InAs NWs were grown in a horizontal growth tube on 600-nm SiO_2-n^+-Si substrates by metal–organic chemical vapor deposition. Au colloids (40-nm diameter, Ted Pella) were dispersed from solution on cleaned substrates pretreated with Poly-L-Lysine. The substrates were then loaded into the growth chamber and the temperature was ramped to the final growth temperature (350 °C) in a H_2 atmosphere. Arsine (148 $\mu mol\,min^{-1}$, 10% AsH_3 in H_2) and Trimethylindium (TMIn, 6 $\mu mol\,min^{-1}$) precursors were then introduced into 1.2 $L\,min^{-1}$ H_2 carrier gas with an input V:III ratio of 25 and a chamber pressure maintained at 100 Torr. The samples were then cooled to room temperature in an AsH_3 atmosphere. The single-crystal InAs NWs were 30–75 nm in diameter and 20–30 μm long after a 15-min growth time.

A sonication of 7 s in ethanol solution was used to suspend the nanowires in the solution; they were then transferred to a 600-nm SiO_2-n^+Si substrate with a prepatterned indexed grid with alignment marks. Optical microscopy was used to determine the locations of the randomly dispersed nanowires on this grid structure. Patterning of contacts by EBL followed by 15-nm Ti/85-nm Al metallization and a standard liftoff process were used to create ohmic contacts to the nanowires. Gate-pattern definition by EBL, sputtering of 100 nm SiO_2/100 nm Au, and subsequent lift-off were used to form top-gate structures. Current–voltage characteristics were then obtained with an HP4155 semiconductor parameter analyzer in air at room temperature. The device dimensions were measured after electrical measurements under the highest magnification (× 300 000) using a FEI XL 30 Environmental SEM operating at an acceleration voltage of 10 kV.

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