Carbon nanotube based nonvolatile memory

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We propose the use of carbon-nanotube based vacuum microelectronics for a nonvolatile memory core. A design that can be implemented with state-of-the art nanotube fabrication techniques is presented and nonvolatile memory operation, up to 0.25 GHz, is shown to be feasible through circuit simulations. When integrated with flip-chip technology, this type of memory offers a possible solution to the problem of flash memory scaling coupled with the advantages of high density integrated circuitry and a faster speed of operation. © *2005 American Institute of Physics*. [DOI: 10.1063/1.2139847]

Planar flash memory technology based on silicon field effect transistors faces obstacles to further miniaturization. Scaling of the tunneling oxide used in these memory cells is complicated by the incompatible requirements of high programming current and minimal leakage current.[1] The increased voltage needed for hot electron injection is an additional problem. Although the basic tunneling mechanism is attractive, it is widely recognized that alternative materials and new device architectures are imperative for further advances in nonvolatile memory technology. In this letter, we propose a carbon nanotube (CNT) based memory core, which circumvents the issues of transistor scaling and hot electron effects and uses the enhanced field emission[2] that can be obtained from nanometer sized CNTs. The specific advantages of the proposed design include lower power levels due to the higher efficiency of field emission from nanostructures, greater circuit density, a faster speed of operation as the electrons travel in vacuum, greater reliability due to the absence of tunneling through oxide, and immunity to ionizing radiation.

CNTs display exceptional mechanical, chemical and thermal stability and extensive research is being carried out to probe their electrical properties. The controlled growth of metallic carbon nanostructures, in various morphologies, i.e., fibers, cones, etc., with a range of diameters (1–100 nm) and lengths (1–100 μm), through chemical vapor deposition (CVD) techniques, has been well established.[3–5] For example, an electric field can be used to orient the nanotubes perpendicular to the substrate.[6] One can obtain regulated field emission[3,7–9] from the tips of these vertical nanotubes, arranged in a triode like arrangement, with the CNT as the cathode. The emission current (I) is determined by the Fowler-Nordheim (FN) relationship: $I=aV^2\exp(-b\varphi^{3/2}/\beta V)$, where V is the applied voltage, φ the work function of the surface and β is the field enhancement factor due to the radius of curvature of the emitting tip (a and b are phenomenological constants). In CNTs, β, the field enhancement factors[2,9] can be as high as 3400 due to the nanometer radius of curvature, which translates to a higher emission current at a given voltage. A gate electrode can be used to construct an active field emission device and avoid the performance trade-offs that plague flash memory tunneling oxide design.[10] A vacuum based field emission system can then replace the hot carrier mechanism used in current technology, allowing a memory cell to be programmed and erased solely via tunneling. There is an added advantage that the active transistors in the memory core can be dispensed with. A higher device speed and a larger current drive are also ensured by operation in vacuum.

It was experimentally observed[9] that field emission from nanotubes can be obtained for up to 1500 h at reasonable vacuum levels of 1 Torr. In current flash memory technology, a field effect transistor within the memory cell and an external sense amplifier are both needed to sense the limited charge that passes through the tunneling oxide. However, the high current capacity of the CNTs—up to 0.2 mA per single nanotube[9]—could eliminate the need for an amplifier within the memory cell. The use of common fabrication techniques and advanced packaging ("flip-chip") technologies,[11] incorporating three-dimensional circuit integration, allow the implementation of the proposed CNT based circuitry.

The cross section of the proposed memory cell is shown in Fig. 1(a) and can be constructed through conventional micro- and nano-fabrication techniques. Note that the memory cell is comprised of both the upper and lower portions of the figure which depict two separate silicon substrates. The substrate-I is ion implanted to create (i) a lightly doped region, which serves as a current limiting resistor [R_B in Fig. 1(b)], and (ii) an adjacent highly doped region which acts as the Word Line (WL) for the memory cell. A relatively thick ($\geqslant 1$ μm) silicon oxide (gate oxide) layer is required to accommodate the vertical CNTs and reduce the gate capacitance, and can be deposited on top through CVD. Subsequently, an overlayer of metal is deposited on the gate oxide and patterned via photolithography to form a Bit Line (BL). Electron beam lithography can then define a gate aperture, through which the oxide and the BL metal layers are etched vertically. A suitable diffusion barrier (e.g., TiN) and catalyst (e.g., Ni, Co, or Fe) are deposited through the gate aperture and a vertical CNT grown by CVD.[3,12] The grown CNT is the field emission tip (*cathode*) of the nanotube based triode N_1. The BL acts as the *gate* of triode N_1 and the *anode* of triode N_2 (Fig. 1).

The nanotube triode-N_2 is fabricated on substrate-II, and constitutes the second half of the memory cell. Initially, a thin silicon oxide layer (~20 nm) is grown on substrate-II. Metal is deposited onto the oxide and etched into isolated

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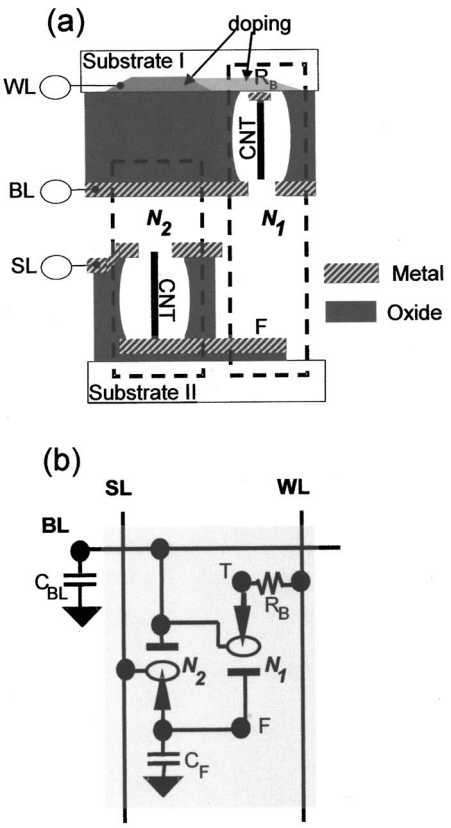

FIG. 1. (a) Schematic cross section of the proposed carbon nanotube based nonvolatile read-write memory cell. The cell is constituted of two triodes N_1 and N_2 (outlined) separately assembled on two substrates, and which can be aligned using flip-chip technology. (b) A schematic circuit diagram of the memory cell, placed along with the write line (WL), bit line (BL), and sense line (SL) architecture. Along with the triodes N_1 and N_2, the storage capacitor C_F, a current limiting ballast resistor R_B and the parasitic capacitance C_{BL} are also shown.

islands using photolithography, forming a floating node capacitor [C_F, Fig. 1(b)]. This metal also serves as the *anode* of N_1. A thick oxide layer is laid down, followed by metal deposition. This metal is patterned into the sense line (SL) by photolithography, and the gate oxide is etched away to allow the electron beam of N_1 to reach the floating conductor. Electron beam lithography is then used to define the gate aperture and place the catalyst for nanotube (*cathode*) growth for triode N_2.

It is to be noted that the fabrication is done separately on substrates-I and II. The substrates are then aligned, for dense integration, using established flip-chip technologies.[11] Alternatively, one can design a sensor system for active registration of the two substrates. In this scheme, the current from a nanotube field emitter on one substrate is sensed by an array of anodes on the other substrate akin to a four-quadrant detection scheme.

A SPICE circuit simulation model, developed for a field emission triode,[13] on the MULTISIM® software platform was used to simulate the proposed memory cell, as shown schematically in Fig. 1(b). The FN parameters are estimated from previous work,[11] where field emission from a gated CNT structure, using a 1.1 μm tip-to-gate spacing was reported. While previous work used photolithography to fabricate the structures, we propose the use of electron-beam lithography, which can give a reduced CNT to gate [Fig. 1(a)] spacing, for even higher field emission performance. With a spacing

TABLE I. An overview of the read-write operation of the proposed nonvolatile memory cell. The voltages on the control lines (SL, BL, and WL) are varied to read, write and store logic values of 0 and 1 in the cell.

Control Lines/Operation	Write 0 (V)	Read 0 (V)	Write 1 (V)	Read 1 (V)
Sense line (SL)	0	3	0	3
Bit line (BL)	1.5	1.5	−2	1.5
Write line (WL/T)	−1.5	2	−1.5	2

of 100 nm, we extrapolate FN coefficients of $a=0.75$ A/V^2 and the factor $(b\phi^{3/2}/\beta)=50.7$ V. We estimate the bit line capacitance [C_{BL}, Fig. 1(b)] as 46.1 fF, from previous studies on vacuum microelectronic devices.[14] Based on the geometry of devices, the storage node capacitance (C_F, Fig. 1) was taken to be 850 aF. The ballast resistor (R_B, Fig. 1), used to limit emitter tip current, was given a value of 50 kΩ.

Two representative cycles of operation (Table I) of the nonvolatile CNT based memory cell at 0.25 GHz are shown in Fig. 2. The voltage across the storage node capacitance (C_F) is initially positive—corresponding to a logical value of 1, as it would be after being erased by a read cycle.

(a) Write 0: At 0 ns (Fig. 2), the SL is brought to 0 V so that triode N_2 is turned off during the write cycle. The BL is set to 1.5 V in order to write a 0 to the memory cell (The input to BL is the complement of the data to be written). The WL is brought to ~ -1.5 V, as shown by the voltage at node T [Fig. 1(b)]. The potential difference between T and BL causes current flow through N_1 and charges C_F to a negative value, giving the memory cell a logical value of zero. Note that this voltage, at F, is not low enough to induce any significant current from N_2. The ballast resistor (R_B) serves to limit the current to 4 μA. We note that if the sense line remains at ground (i.e., the circuit remains idle) for one year, N_2 will increase the voltage of T by only 0.2 V, reducing the charge available during the next read cycle by less than 7 %.

(b) Read 0: To read the memory cell, the SL is asserted at 2.6 ns. The BL remains at 1.5 V. The triode N_2 (Fig. 1) turns on in response to the potential difference between its gate (SL) and tip (F), allowing the charge to flow out of C_F

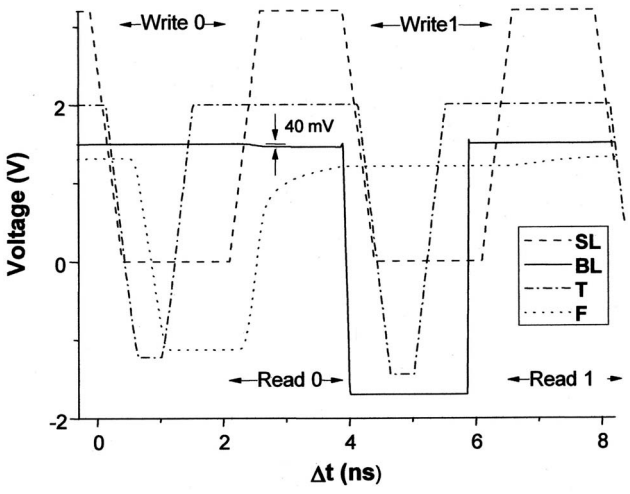

FIG. 2. Circuit simulations, at 0.25 GHz, for two read/write cycles of the proposed CNT based nonvolatile memory cell. The voltage of the sense line (SL), bit line (BL), write tip (T) are systematically asserted to write and read logical values of 0 and 1 onto the floating conductor (F).

through triode N_2 into C_{BL}, decreasing its voltage by ~40 mV. In a real circuit this value would be reduced somewhat by gate current, which has been found to be <1% of the total current in similar devices,[12] and has been neglected in our preliminary model. A sense amplifier could be used to detect this voltage swing.

The voltage of node F tracks the upswing in SL initially, but the tip-gate voltage gradually decreases as SL is held constant, causing N_2 to turn off. This self-limiting behavior protects the tip from over-current damage. During the read cycle, the WL is held high so that N_1 is turned off. Note that this Read process resets the memory cell to a logical value of 1, by charging C_F to a positive voltage.

(c) Write 1: In order to write a value of 1 to the memory cell, the BL is brought to −2 V, and the SL returned to ground. At 3.9 ns, the WL (node *T*) is then brought to ~−1.5 V. Since BL is at a lower potential than *T*, triode N_1 does not turn on and the memory cell retains a logical value of 1.

(d) Read 1: At 6.1 ns, the SL is asserted to a positive voltage, to carry out a second read cycle. The voltage across C_F is positive and the potential difference between *F* and SL is not adequate to turn on N_2, as was the case at the end of the previous read cycle. Only a negligible amount of charge is transferred from the memory cell and we find that the BL swings by only 0.6 mV, much less than the 40 mV voltage swing encountered in the previous Read cycle. There is no leakage current from N_1 as its emission is shielded by its gate [BL in Fig. 1(b)]. This mode of operation coupled with the rectifying behavior of triode N_2 functions allows the memory cell to retain its value until N_1 is activated. Since the memory cell can retain either logical value without any external power input, the memory is nonvolatile. The most energy intensive operations in the cycle are reading and writing a value of 0. It should also be pointed out that the Read cycle must always be followed by a Write cycle to replace data that is lost by the destructive Read processes.

The CNT based architecture for a nonvolatile memory core presented in this paper is easily scalable to lower operating voltages and sizes. The additional advantages include the possibilities of higher operating speeds and radiation tolerance. It is hoped that the dual characteristics of tunneling and vacuum based operation in the present design can offer one possible solution to the problems of flash memory scaling and make nanotube based electronics a reality.

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