24.5 A 4.5nW Wake-Up Radio with -69dBm Sensitivity

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Wake-up receivers (WuRXs) are low-power radios that continuously monitor the RF environment to wake up a higher-power radio upon detection of a pre-determined RF signature. Prior-art WuRXs have 100s of kHz of bandwidth [1] with low signature-to-wake-up-signal latency to help synchronize communication amongst nominally asynchronous wireless devices. However, applications such as unattended ground sensors and smart home appliances wake-up infrequently in an event-driven manner, and thus WuRX bandwidth and latency are less critical; instead, the most important metrics are power consumption and sensitivity. Unfortunately, current state-of-the-art WuRXs utilizing direct envelope-detecting [2] and IF/uncertain-IF [1,3] architectures (Fig. 24.5.1) achieve only modest sensitivity at low-power (e.g., -39dBm at 104nW [2]), or achieve excellent sensitivity at higher-power (e.g., -97dBm at 99μW [3]) via active IF gain elements. Neither approach meets the needs of next-generation event-driven sensing networks.

This paper presents a 0.4V 113.5MHz OOK-modulated WuRX that achieves -69dBm sensitivity with only 4.5nW of power by: 1) reducing the baseband signal bandwidth to 300Hz, suitable for many event-driven applications, to aggressively filter noise; 2) employing a high-*Q* transformer and filter that passively amplifies the voltage of the incoming RF waveform by 25dB and filters adjacent channel noise and interferers; 3) simultaneously demodulating and amplifying the wake-up signal via a high-impedance dynamic threshold MOS (DTMOS) envelope detector (ED) with subthreshold active-inductor biasing; 4) digitizing the ED output via a regenerative comparator with kickback elimination; 5) generating the baseband clock via a 0.9pJ/cycle 1.1nW relaxation oscillator; 6) decoding the received OOK signal modulated with a custom 16b codeword using a high-V_t subthreshold digital baseband correlator; and 7) operating all circuits at 0.4V to minimize static and dynamic power. A block diagram of the architecture is shown in Fig. 24.5.1.

The RF input voltage is amplified at no power cost by an off-chip high-*Q* transformer that also filters out-of-band noise and interference with a 1.9MHz BW. The voltage gain is limited by the impedance ratio between the secondary and primary sides; achieving a gain of 25dB from a 50Ω source requires the secondary load impedance to be >17kΩ. This large impedance transformation requires reactive values that are over an order of magnitude apart, making them difficult to realize while precisely controlling the coupling coefficient, *k*. This issue is addressed by utilizing a combination of lumped and distributed inductive elements as illustrated by discrete inductors and meandering striplines on an RO4003 substrate, respectively, in Fig. 24.5.2. The combination of lumped and distributed elements results in a design that is easily manufactured and highly reproducible (σ=0.34%, 0.4%, and 0.09% for the center frequency, bandwidth, and gain respectively, for typical component tolerances). The measured S_{11} and voltage gain are shown in Fig. 24.5.2. Since the required load impedance of the transformer is too large to measure the voltage gain directly, it was measured at the ED output after de-embedding.

Because the input impedance of the ED must be high to support high passive RF gain, an active ED is implemented via a common-source amplifier. The ED utilizes a DTMOS transistor biased in subthreshold to maximize the 2nd-order non-linearity, and therefore RF-to-BB conversion gain (Fig. 24.5.3). With a 0.4V supply, conventional biasing schemes such as active diodes offer too low conversion gain, while resistive loading is fixed by current levels and limits gain. Instead, the ED is self-biased by a MOS-bipolar-pseudoresistor feedback circuit, R_{FB}, that acts as an active inductor and increases R_{out} at low bias currents, improving the gain by 2.5× and 20×, and SNR by upwards of 3dB and 21dB over resistive and active diode-based biasing techniques, respectively. Since sub-V_t circuits can suffer from significant process variation, both M_N and M_P have 8b of tunability, while R_{FB} has 5b. The tunable feedback network also adjusts the lowpass corner to tune the baseband bandwidth. All critical transistors are sized to trade-off the contributions of 1/*f* noise while minimizing parasitic capacitance, the latter of which ultimately limits the achievable R_{out} of the active inductor (~100MΩ in this design). An inverting voltage doubler provides -0.4V to bias unused transistors in super-cutoff, saving 3nA of leakage current.

The comparator is implemented with a g_m-C integrator followed by a regenerative latch (Fig. 24.5.4). The integrator uses a DTMOS input pair to increase the effective transconductance (g_m+g_{mb}) by 51%, resulting in higher gain and lower noise. Two 5b CDACs tune the comparator threshold voltage (200μV steps) in conjunction with a diode-connected reference ladder for coarse tuning (6.25mV steps). Due to the unbalanced and high output impedances of the ED (~100MΩ) and reference ladder (~2GΩ), directly connecting the comparator would result in differential kickback errors. The time constants of these nodes are sufficiently large that this perturbation would not settle by the next comparison, so an S/H circuit is added to provide balanced impedances and temporarily store the kickback charge. An added reset transistor to the integrator ensures that the same amount of charge injected on the sampling capacitors is removed at the end of each cycle, resulting in zero net kickback charge. The comparator power is reduced via an early-reset scheme where the preamplifier turns off once the latch has regenerated, saving 33% power at -69dBm in simulation.

Coding is a commonly used approach to reduce the required SNR in communication systems while also providing robustness. Since power requirements prohibit symbol- or sequence-level synchronization, a custom 16b codeword is designed to achieve low autocorrelation. Received signals are 2× oversampled and fed via a shift register into a digital correlator that computes the Hamming distance between the received and locally-stored codewords (Fig. 24.5.4). When the Hamming distance is below a programmable threshold, a two-stage voltage doubler generates a >1V wake-up signal. All digital baseband circuitry operates in sub-V_t using custom-designed logic gates with stacked FETs to minimize leakage current. The comparator and correlator are clocked by an integrated 1.1nW 600Hz relaxation RC oscillator.

The circuit was fabricated using a 0.18μm CMOS SOI process and consumes 4.5nW (Fig. 24.5.5). Measured transient waveforms are shown for each block when the OOK modulated signal with the correct codeword is received. The measured BER curve is plotted using the data taken from the comparator output under the assumption of perfect synchronization between clock and input data, yielding a sensitivity of -65dBm at a BER of 0.1%. Figure 24.5.5 also shows missed-detection-rate curves after correlation, where a 0.1% missed detection rate was achieved with random (i.e., not synchronized) transmission at -67.5dBm while maintaining a false alarm rate <<1/hr. When the thresholds are optimized towards detection and away from false alarm prevention, the system achieves a sensitivity of -69dBm while maintaining a false alarm rate <1/hr. Figure 24.5.6 summarizes the proposed design and compares it to other state-of-the-art WuRXs. A die and PCB photo are shown in Fig. 24.5.7.

Acknowledgements:
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References:

[1] N. M. Pletcher, et al., "A 2GHz 52μW Wake-Up Receiver with -72dBm Sensitivity Using Uncertain-IF Architecture," *ISSCC,* pp. 524-525, Feb. 2008.
[2] N. E. Roberts, et al., "A 236nW -56.5dBm-Sensitivity Bluetooth Low-Energy Wakeup Receiver with Energy Harvesting in 65nm CMOS," *ISSCC,* pp. 450-451, Feb. 2016.
[3] C. Salazar, et al., "A –97dBm-Sensitivity Interferer-Resilient 2.4GHz Wake-Up Receiver Using Dual-IF Multi-N-Path Architecture in 65nm CMOS," *ISSCC,* pp. 1-3, Feb. 2015.

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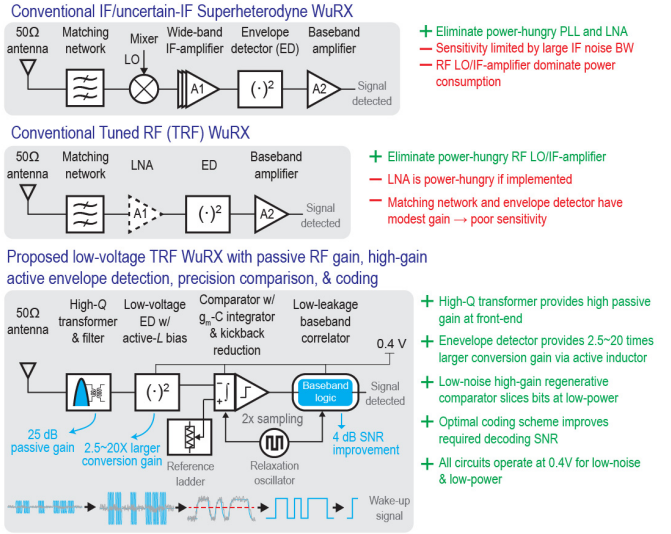


Figure 24.5.1: Block diagram of conventional WuRX approaches and the proposed WuRX.

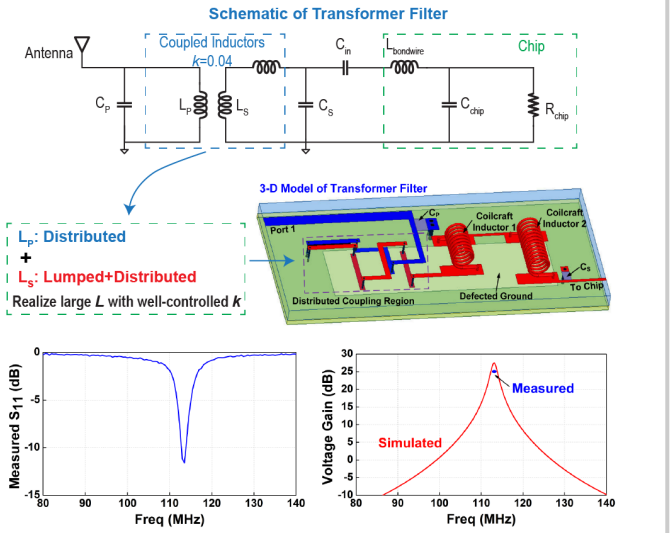


Figure 24.5.2: Schematic and 3-D model of the transformer; measured S_{11} and voltage gain.

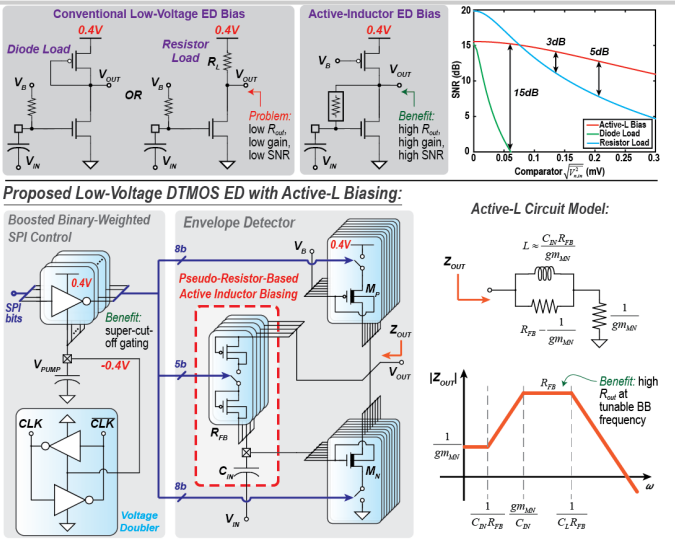


Figure 24.5.3: SNR comparison between three ED biasing schemes (top); active-inductor ED and equivalent output impedance (bottom).

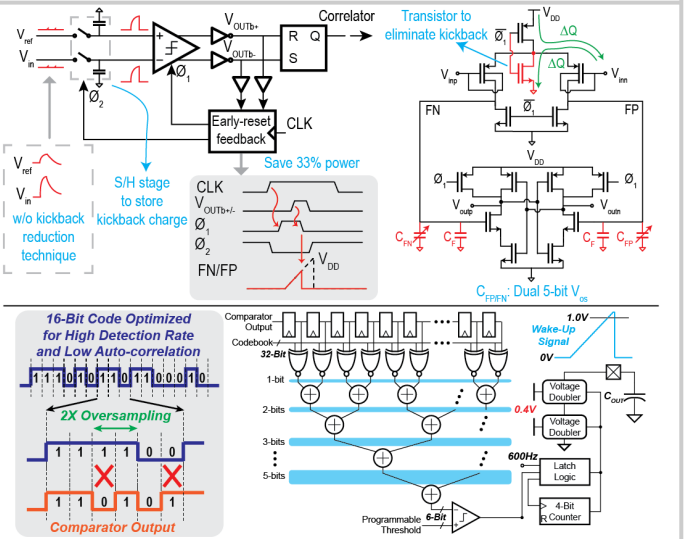


Figure 24.5.4: Dynamic comparator and S/H stage to eliminate kickback (top); 16b coding and digital correlator with output driver (bottom).

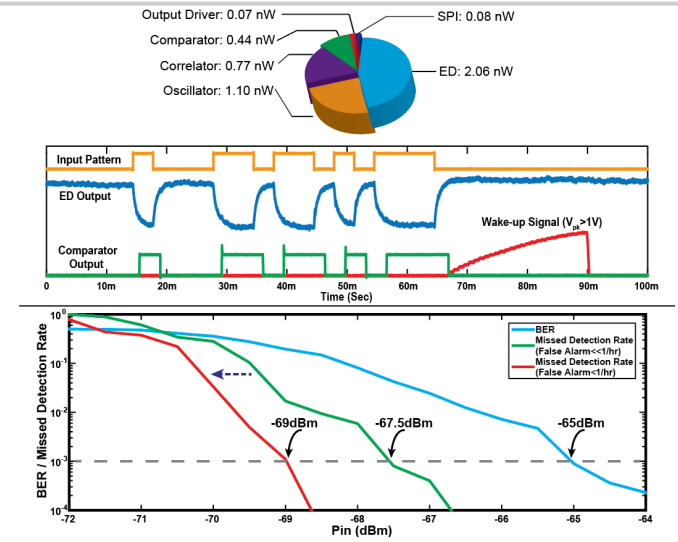
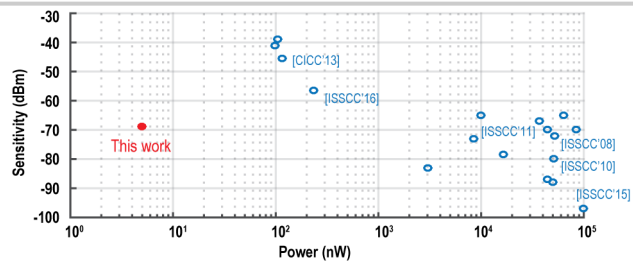


Figure 24.5.5: Measured power breakdown and waveforms with a correct pattern (top); BER & Missed-Detection-Rate curves (bottom).



	Plectcher ISSCC'08	Huang ISSCC'10	Pandey ISSCC'11	Oh CICC'13	Salazar ISSCC'15	Robert ISSCC'16		This Work
Technology	90nm	90nm	130nm	130nm	65nm	65nm		180nm
Carrier Frequency	2GHz	915MHz	402MHz	402MHz	2.4GHz	2.4GHz		113.5MHz
Modulation	OOK	OOK	FSK	OOK	OOK	OOK		OOK
Power Supply	0.5V	1V	1V	1.2/0.5V	0.5V	1/0.5V		0.4V
Digital Correlator?	No	No	No	31-bit	No	31-bit		32-bit[1]
Oscillator?	Ring osc.	No	Inj.-locked ring osc.	XTAL osc.	LC DCO	XTAL osc.		Relaxation osc.
Gain Stage(s)	IF[2]	RF/BB[2]	IF[2]	ED[2]	IF/BB[2]	ED[2]	ED/BB[2]	TF/ED/BB
Data Rate	100kbps	10kbps	200kbps	12.5kbps	10kbps	8.192kbps		0.3kbps
Energy/bit	520pJ	5100pJ	220pJ	9.3pJ	9900pJ	12.7pJ	28.8pJ	15.0pJ[1]
Sensitivity	-72dBm	-80dBm	-70dBm	-45dBm	-97dBm	-39dBm	-56.5dBm	-69dBm[3]
Normalized Sensitivity[4]	-84.6dBm	-87.6dBm	-98.2dBm	-53.1dBm	-112dBm	-46dBm	-63.7dBm	-69dBm
Power	52μW	51μW	44μW	116nW	99μW	104nW	236nW	4.5nW

[1] 16-bit code sequence with 2x oversampling.
[2] The front-end matching network also has modest passive gain.
[3] Defined with less than 10^{-3} miss detection rate.
[4] Calculated by normalizing the data rate to 0.3kbps.

Figure 24.5.6: Measurement results of the WuRX (top); performance comparison with state of the art (bottom).

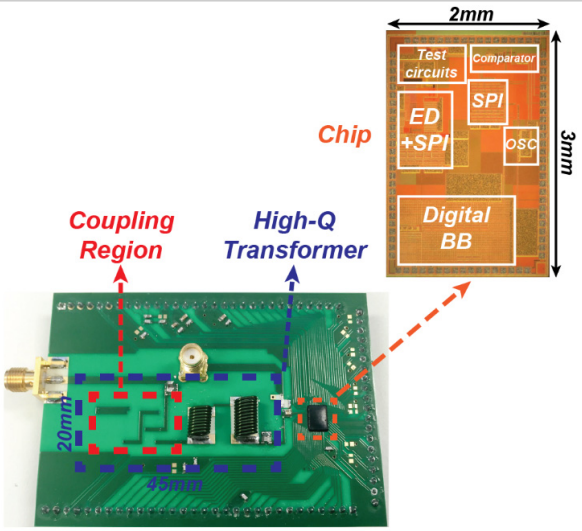


Figure 24.5.7: Die micrograph (top); photograph of the entire wake-up radio (bottom).

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